Мультимедиа процессор AIT8328

CPU AIT8328

Datatshee
Описание

Notice

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1 Overview

The AIT8328 is a highly integrated multi-media system-on-chip (SOC) for Sports-cam, Car-cam, and IP-cam devices.

The AIT8328 includes dual 32-bit RISC processors, AIT's advanced ISP engine, and high definition MJPEG/H264 video codec up to 1080P30.

The powerful on-chip ISP (image signal processor) implements the most advanced algorithm to deliver high-quality image and precision control for AF/AE/AWB. The hardwired WDR engine and rolling-shutter compensation also enhance image/video quality in consumer applications.

The MJPEG/H.264 video codec supports up to 30 frames per second with 1920x1080 resolution. Pure hardwired architecture achieves low power operation and extends battery time. MCTF (motion -compensated temporal filter) is integrated to enhance image quality and reduce video bit-rate under dark environment.

The AIT8328, powered by Alpha Imaging Technology, will provide complete development environment for customer. "Time-to-Market" is possible.

Applications

- Sports Camera
- Car Camera
- IP Camera

2 Function List

☐ **Dual Core High Performance CPU**

- Dual 600MHz 32-bit RISC processors

☐ **Memory Interface**

- 16-bit 800MHz data rate DDR2/DDR3 interface up to 4Gb
- Optional stacked 32-bit 400MHz data rate LPDDR
- Optional stacked 16-bit 800MHz data rate DDR3

☐ **Camera**

- Support up to 64M pixel sensor with Bayer, YUV format in parallel or MIPI interface
- High performance image pipeline to support high speed continuous shot up to 13M@30fps
- Full resolution still image capture during video recoding without frame loss (ex. 8M JPEG capture during 1080p30 video recoding)
- Support dual sensor interface (one parallel + one MIPI or two MIPI)
- MIPI CSI (one 4-lane and one 2-lane) interface
- Multiple stream support 1080p + 720p + MJPEG or 2x1080p @ different bit-rate etc. for local storage and network application
- 3D still and video capture

☐ **Image Processing**

- Rolling shutter compensation
- 3D motion compensated temporal filtering (MCTF) for temporal noise reduction
- Advance spatial noise reduction
- Electronic and Digital image stabilization
- Calibrated and advanced Automatic Defect Pixel Compensation
- Lens shading correction
- Advanced Interpolation (Demosaic) algorithm
- Advanced chroma shading
- Space Color non-Uniformity Compensation
- Advanced False Color Reduction
- Color space conversion
- Enhanced Gamma table
- High Dynamic Range
- Edge Enhancement
- High performance Anti-crosstalk
- 3D LUT color correction
- Histogram Equalization or Modification
- Blue edge reduction
- Anti-flare
- Brightness/Contrast enhancement
- Hue/Saturation enhancement

  Advanced Auto-Exposure/ Auto-White-Balance / Auto Focus

  Black Level Compensation

  Multiple special effect like sepia, binary, emboss, negative, sketch, oil, crayon, blackboard

  Flexible flash strobe function (IGBT and LED)
- Linear digital zoom up to 1024x

☐ **LCD / TV / HDMI Display**

- HDMI 1.4
- Simultaneously LCD and HDMI/TV display output
- Support LCD panel up to Full HD with 16M colors
- Support 8/12/16 bit CPU and RGB interface
- 4 layers OSD with alpha-blending, rotation, mirror, flip and scaling function
- Embedded TV DAC to output 480/576 interlace or progressive composite output

☐ **Video**

- Optimized video engine for low power requirement
- Baseline, Main and High profiles H.264 Level 4.1 codec up to 1920x1080@30fps
- Supports both CAVLC & CABAC entropy encoding
- Adjustable motion search complexity
- Flexible bit rate control and frame rate adjustment
- Adjustable motion search complexity to improve video quality under the same bit rate
- Support temporal SVC, multiple ROI, and slice mode
- Support multi-stream output with YUY2, MJPEG, and H.264
- Support Microsoft Lync UCConfig Modie0/1

☐ **JPEG**

- High performance JPEG engine up to 240Mpixel/s
- Compliant with JPEG baseline standard (ISO/IEC 10918) with JFIF.
- Hardware JPEG engine supports up to 64M resolution

☐ **Voice / Audio**

- On-chip audio codec for voice / audio recording with 8K~192KHz sampling rate
- Dual synchronous dual digital audio interface (I2S) for external ADC/DAC support
- High performance audio stereo ADC with SNR up to 106dB
- Support microphone input PGA 0~30dB with 1dB step
- Optimized power performance for audio core
- Support digital MIC interface
- Support single-ended mono playback with SNR up to 95dB
- Support advanced voice processing algorithm for Skype audio certification

☐ **Graphic DMA Engine**

- BitBLT
- Line draw
- Color expansion
- Data Copy/Paste
- Raster Operation
- Pattern / Solid Fill
- Transparent overlay
- Hardware cursor
- Hardware image rotate, flip, mirror, scaling and color format transform

Storage controller

- Support 3 x SD / SDIO / mini-SD / T-Flash / MMC / RS-MMC
- Support 512 / 2K bytes page SLC / MLC NAND flash
- Support chip boot up from ROM, SD, or NAND flash

☐ **USB**

- USB 2.0 High Speed device controller and PHY
- Support Microsoft Lync, UVC1.1, UVC1.5 and Skype specification
- Support USB LPM-L1 fast suspend/resume mode

☐ **Peripheral**

- SPI master (x3)
- SPI slave
- I2C master (x3)
- I2C slave
- UART (x4)
- PWM (x18)
- GPIO

- 32K RTC
- Watchdog timer
- Power-on reset
- SAR ADC (8-CH)
- IGBT
- IrDA

□ **Clock**

- Support input range from 20~27MHz
- Multiple PLL for various application combination
- Support fractional and spread-spectrum type PLL

□ **Package**

- 13x13mm BGA 304-pins (external DDR2 / DDR3)
- 13x13mm BGA 277-pins (stack LPDDR)
- 15x15mm BGA 338-pins (stack DDR3)

Ordering Information

Part Number	Package Size	Note
AIT8328G	13mm X 13mm X 1.2mm BGA, 304-pins	
AIT8328P	13mm X 13mm X 1.2mm BGA, 277-pins	
AIT8328Q	15mm x 15mm X 1.2mm BGA, 338-pins	TBD.

3 Block Diagram

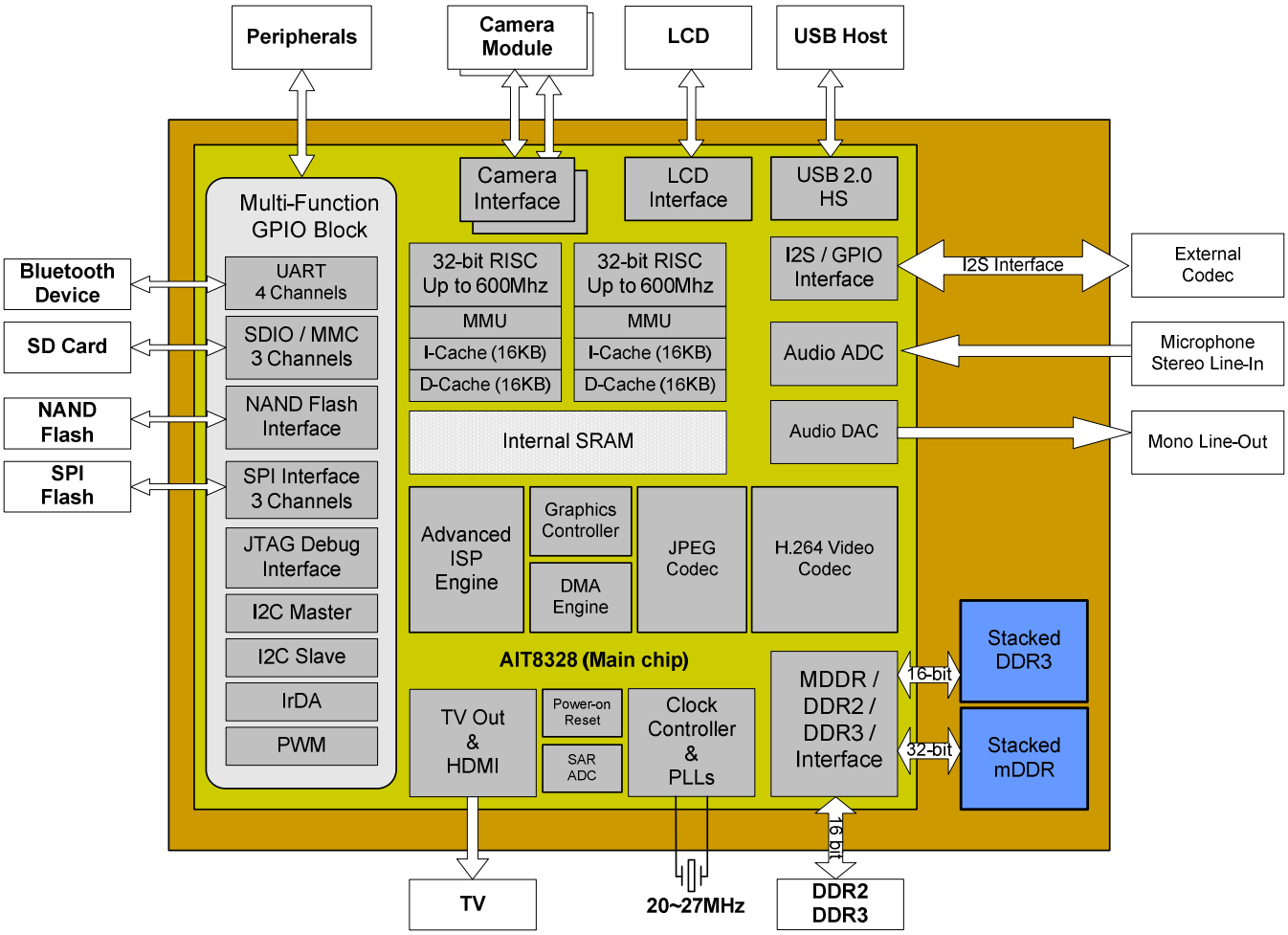


Figure 1. Block Diagram

4 Pin Description and Diagram

4.1 Pin Description (BGA304 AIT8328G)

I : Input pin
IO: Bidirection pin
ID: Input pin with pull-down configuration
IU: Input pin with pull-up configuration
IOU: Bidirection pin with pull-up configuration
IOD: Bidirection pin with pull-down configuration
O: Output pin
Z: Tri-state at reset
HZ: Tri-state Hi-Z at reset
LZ: Tri-state Lo-Z at reset

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
System Interface (11 pin) (VDD_AGPIO/VSS)					
1	PRST_N	I	W8	Z	Chip reset (low active)
2	PHI2C_SCL	IOU	U11	HZ	Host I2C slave clock
3	PHI2C_SDA	IOU	T11	HZ	Host I2C slave data
4	AGPIO0	IOD	W9	LZ	A-group GPIO0 (Download mode strapping bit0) {AGPIO6, AGPIO0}= 00: Serial flash (SPI type) 01: Serial flash (I2C type) 10: Internal ROM (32K) 11: Host I2C
5	AGPIO1				A-group GPIO1 (I2C slave address strapping: 0:7'h3, 1:7'h4)
6	AGPIO2	IOD	V9	LZ	A-group GPIO2 (Boot-up CPU select strapping: 0:CPU A, 1:CPU B)
7	AGPIO3	IOD	U10	LZ	A-group GPIO3 (PLL boot auto switch boot strapping: 0:enable, 1: disable)
8	AGPIO4	IOD	W10	LZ	A-group GPIO4 CPU JTAG MODE[0] : CPU JTAG Multi-function select boot strapping '0' CPU A from Multi-function Set 0, CPU B from Set1, Chain mode from Set 0 if enabled '1' CPU A from Multi-function Set 1, CPU B from Set0, Chain mode from Set 1 if enabled
9	AGPIO5	IOD	V10	LZ	A-group GPIO5 CPU JTAG MODE[1] : CPU JTAG Chain mode boot strapping '0' JTAG chain mode enable '1' JTAG chain mode disable
10	AGPIO6	IOU	V11	HZ	A-group GPIO6 (Download mode strapping bit1) {AGPIO6, AGPIO0}= 00: Serial flash (SPI type) 01: Serial flash (I2C type) 10: Internal ROM (32K) 11: Host I2C
11	AGPIO7	IOD	T10	LZ	A-group GPIO7 CPU JTAG MODE[2] : CPU debug mode enable boot strapping '0' CPU Debug mode disable '1' CPU Debug mode enable

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
					Note: To enable CPU SRST debug mode, {AGPIO7,AGPIO6,APGIO0} = 3'b111;
Main Clock interface (2 pin) (VDD_CLK/VSS)					
12	XSCI	I	B1	Z	Crystal oscillator and main clock input
13	XSCO	O	C1	Z	Crystal oscillator output
I2S interface (5 pin) (VDD_I2S/VSS)					
14	PI2S_SCK	IOD	W11	LZ	I2S serial clock
15	PI2S_WS	IOD	V12	LZ	I2S word clock
16	PI2S_SDI	IOD	W12	LZ	I2S data input
17	PI2S_MCLK	IOD	U12	LZ	I2S master clock
18	PI2S_SDO	IOD	T12	LZ	I2S data output
Sensor Control Interface (11 pin) (VDD_SEN/VSS)					
19	PS_RST_N	IOD	R16	LZ	Sensor0 reset
20	PDCLK	IOD	P16	LZ	Sensor0 main clock
21	PSCK	IOD	N17	LZ	Sensor0 serial interface clock
22	PSDA	IOD	N16	LZ	Sensor0 serial interface data
23	PSEN	IOD	P17	LZ	Sensor0 enable
24	PPXL_CLK	IOD	N19	LZ	Sensor0 pixel clock
25	PVSYNC	IOD	N18	LZ	Sensor0 vertical sync
26	PHSYNC	IOD	M18	LZ	Sensor0 horizontal sync
27	PS_RST_N_1	IOD	M17	LZ	Sensor1 reset
28	PDCLK_1	IOD	M19	LZ	Sensor1 main clock
29	PSEN_1	IOD	L16	LZ	Sensor1 enable
MIPI_RX0 I/F (10 pin) (AVDD_MIPI_RX0/VSS)					
30	MIPI_RX_0_DA0P	AI	V19	Z	MIPI RX0 D-PHY positive data lane0 input Sensor 12-bit mode raw data [11] Sensor 10-bit mode raw data [9] Sensor 8-bit mode raw data [7]
31	MIPI_RX_0_DA0N	AI	V18	Z	MIPI RX0 D-PHY negative data lane0 input Sensor 12-bit mode raw data [10] Sensor 10-bit mode raw data [8] Sensor 8-bit mode raw data [6]
32	MIPI_RX_0_DA1P	AI	U19	Z	MIPI RX0 D-PHY positive data lane1 input Sensor 12-bit mode raw data [9] Sensor 10-bit mode raw data [7] Sensor 8-bit mode raw data [5]
33	MIPI_RX_0_DA1N	AI	U18	Z	MIPI RX0 D-PHY negative data lane1 input Sensor 12-bit mode raw data [8] Sensor 10-bit mode raw data [6] Sensor 8-bit mode raw data [4]
34	MIPI_RX_0_CKP	AI	T19	Z	MIPI RX0 D-PHY positive clock lane input Sensor 12-bit mode raw data [7] Sensor 10-bit mode raw data [5] Sensor 8-bit mode raw data [3]
35	MIPI_RX_0_CKN	AI	T18	Z	MIPI RX0 D-PHY negative clock lane input Sensor 12-bit mode raw data [6] Sensor 10-bit mode raw data [4] Sensor 8-bit mode raw data [2]
36	MIPI_RX_0_DA2P	AI	R19	Z	MIPI RX0 D-PHY positive data lane2 input Sensor 12-bit mode raw data [5] Sensor 10-bit mode raw data [3] Sensor 8-bit mode raw data [1]
37	MIPI_RX_0_DA2N	AI	R18	Z	MIPI RX0 D-PHY negative data lane2 input

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
					Sensor 12-bit mode raw data [4] Sensor 10-bit mode raw data [2] Sensor 8-bit mode raw data [0]
38	MIPI_RX_0_DA3P	AI	P19	Z	MIPI RX0 D-PHY positive data lane3 input Sensor 12-bit mode raw data [3] Sensor 10-bit mode raw data [1]
39	MIPI_RX_0_DA3N	AI	P18	Z	MIPI RX0 D-PHY negative data lane3 input Sensor 12-bit mode raw data [2] Sensor 10-bit mode raw data [0]
MIPI_RX1 I/F (6 pin) (AVDD_MIPI_RX1/VSS)					
40	MIPI_RX_1_DA1P	AI	L19	Z	MIPI RX1 D-PHY positive data lane1 input Sensor 12-bit mode raw data [1]
41	MIPI_RX_1_DA1N	AI	L18	Z	MIPI RX1 D-PHY negative data lane1 input Sensor 12-bit mode raw data [0]
42	MIPI_RX_1_CKP	AI	K19	Z	MIPI RX1 D-PHY positive clock lane input
43	MIPI_RX_1_CKN	AI	K18	Z	MIPI RX1 D-PHY negative clock lane input
44	MIPI_RX_1_DA2P	AI	J19	Z	MIPI RX1 D-PHY positive data lane2 input
45	MIPI_RX_1_DA2N	AI	J18	Z	MIPI RX1 D-PHY negative data lane2 input
BGPIO interface (23 pin) (VDD_BGPIO/VSS)					
46	BGPIO0	IOD	W1	LZ	B-group GPIO10 SIF clock
47	BGPIO1	IOD	V1	LZ	B-group GPIO11 SIF chip select
48	BGPIO2	IOD	W2	LZ	B-group GPIO12 SIF data output
49	BGPIO3	IOD	V2	LZ	B-group GPIO13 SIF data input
50	BGPIO4	IOD	V3	LZ	B-group GPIO14 SIF WP_N
51	BGPIO5	IOD	W3	LZ	SIF HOLD_N
52	BGPIO6	IOD	W4	LZ	B-group GPIO16
53	BGPIO7			LZ	B-group GPIO17
54	BGPIO8	IOD	U4	LZ	B-group GPIO18
55	BGPIO9	IOD	T6	LZ	B-group GPIO19
56	BGPIO10	IOD	W5	LZ	B-group GPIO20
57	BGPIO11	IOD	V5	LZ	B-group GPIO21
58	BGPIO12	IOD	U5	LZ	B-group GPIO22
59	BGPIO13	IOD	U6	LZ	B-group GPIO23
60	BGPIO14	IOD	V6	LZ	B-group GPIO24
61	BGPIO15	IOD	W6	LZ	B-group GPIO25
62	BGPIO16	IOD	U7	LZ	B-group GPIO26
63	BGPIO17	IOD	V7	LZ	B-group GPIO27
64	BGPIO18	IOD	W7	LZ	B-group GPIO28
65	BGPIO19	IOD	T7	LZ	B-group GPIO29
66	BGPIO20	IOD	T8	LZ	B-group GPIO30
67	BGPIO21	IOD	U8	LZ	B-group GPIO31
68	POR_OPT	I	P9	Z	Power-on reset option (0:external, 1:internal)
CGPIO interface (27 pin) (VDD_CGPIO/VSS)					
69	CGPIO0	IOD	J16	LZ	C-group GPIO32
70	CGPIO1	IOD	J17	LZ	C-group GPIO33
71	CGPIO2	IOD	H17	LZ	C-group GPIO34
72	CGPIO3	IOD	H19	LZ	C-group GPIO35

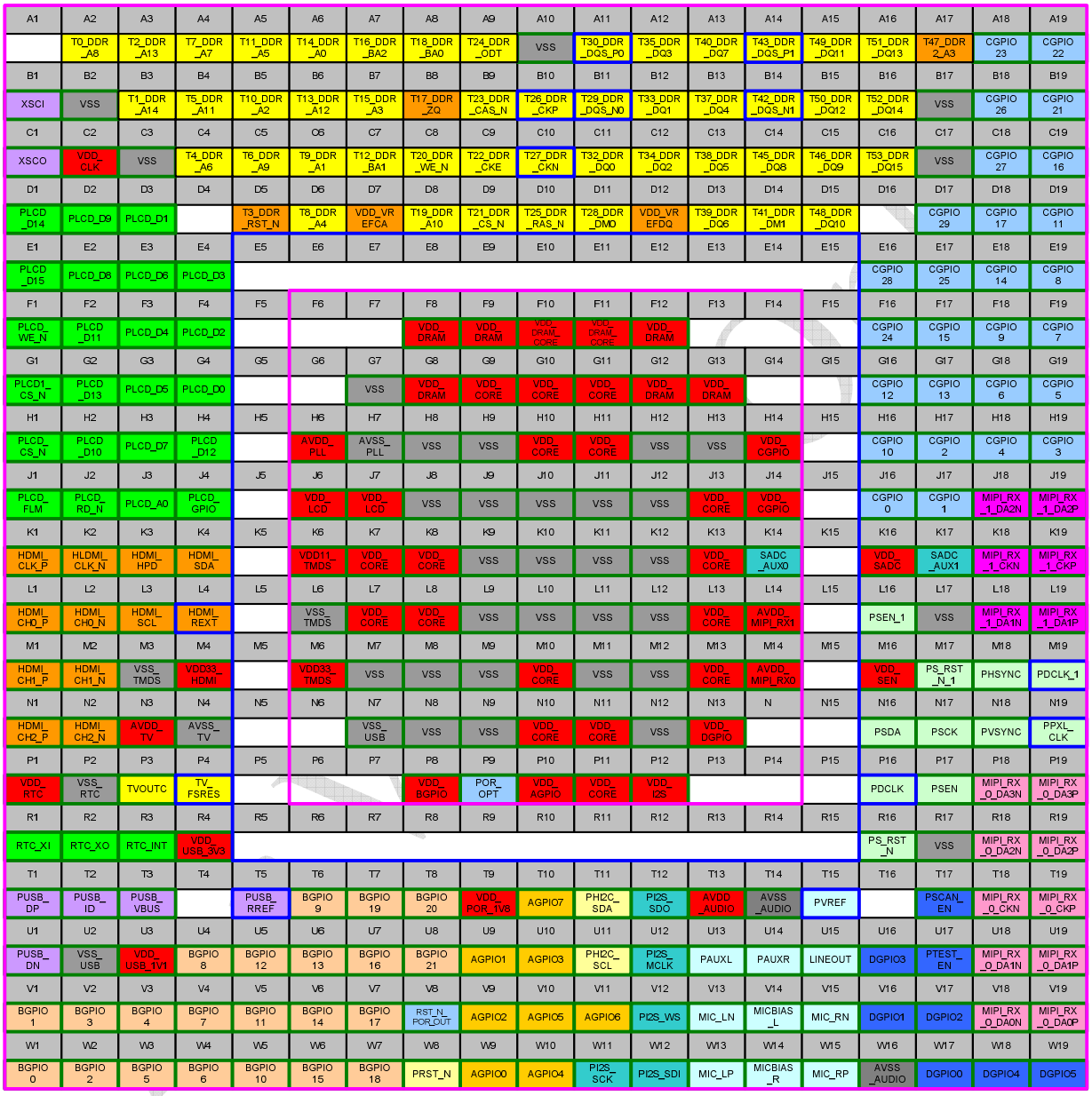
Pin Num	Pin Name	Type	Loc.	Rst# state	Description
73	CGPIO4	IOD	H18	LZ	C-group GPIO36
74	CGPIO5	IOD	G19	LZ	C-group GPIO37
75	CGPIO6	IOD	G18	LZ	C-group GPIO38
76	CGPIO7	IOD	F19	LZ	C-group GPIO39
77	CGPIO8	IOD	E19	LZ	C-group GPIO40
78	CGPIO9	IOD	F18	LZ	C-group GPIO41
79	CGPIO10	IOD	H16	LZ	C-group GPIO42
80	CGPIO11	IOD	D19	LZ	C-group GPIO43
81	CGPIO12	IOD	G16	LZ	C-group GPIO44
82	CGPIO13	IOD	G17	LZ	C-group GPIO45
83	CGPIO14	IOD	E18	LZ	C-group GPIO46
84	CGPIO15	IOD	F17	LZ	C-group GPIO47
85	CGPIO16	IOD	C19	LZ	C-group GPIO48
86	CGPIO17	IOD	D18	LZ	C-group GPIO49
87	CGPIO21	IOD	B19	LZ	C-group GPIO53
88	CGPIO22	IOD	A19	LZ	C-group GPIO54
89	CGPIO23	IOD	A18	LZ	C-group GPIO55
90	CGPIO24	IOD	F16	LZ	C-group GPIO56
91	CGPIO25	IOD	E17	LZ	C-group GPIO57
92	CGPIO26	IOD	B18	LZ	C-group GPIO58
93	CGPIO27	IOD	C18	LZ	C-group GPIO59
94	CGPIO28	IOD	E16	LZ	C-group GPIO60
95	CGPIO29	IOD	D17	LZ	C-group GPIO61
DGPIO interface (6 pin) (VDD_DGPIO/VSS)					
96	DGPIO0	IOD	W17	LZ	D-group GPIO64
97	DGPIO1	IOD	V16	LZ	D-group GPIO65
98	DGPIO2	IOD	V17	LZ	D-group GPIO66
99	DGPIO3	IOD	U16	LZ	D-group GPIO67
100	DGPIO4	IOD	W18	LZ	D-group GPIO68
101	DGPIO5	IOD	W19	LZ	D-group GPIO69
LCD interface (23 pin) (VDD_LCD/VSS)					
102-117	PLCD_D15~0		E1, D1, G2, H4, F2, H2, D2, E2, H3, E3, G3, F3, E4, F4, D3, G4		LCD data [15:0] LCD[0]: software boot-strapping debug mode LCD[1]: software boot-strapping USB full/high-speed select LCD[2]: software boot-strapping USB PID/VID select LCD[5:3]: software boot-strapping options
118	PLCD_WE_N	IO	F1	Z	LCD write signal
119	PLCD_A0	IO	J3	Z	LCD command or data selection
120	PLCD_RD_N	IO	J2	Z	LCD read signal
121	PLCD_CS_N	IO	H1	Z	LCD enable
122	PLCD1_CS_N	IO	G1	Z	LCD1 enable
123	PLCD_FLM	IOD	J1	LZ	LCD frame sync control
124	PLCD_GPIO	IOD	J4	LZ	LCD GPIO
TV out (2 pin) (AVDD_TV/AVSS_TV)					
125	TVOUTC	AO	P3	Z	TV composite current out
126	TV_FSRES	AI	P4	Z	TV_FSRES out
HDMI (12 pins) (VDD11_TMDS/VDD33_HDMI/VDD33_TMDS/VSS_TMDS)					
127	HDMI_HPD	I/O	K3	Z	HDMI hot plug detect
128	HDMI_SCL	I/O	L3	Z	HDMI serial interface clock
129	HDMI_SDA	I/O	K4	Z	HDMI serial interface data

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
130	HDMI_REXT	O	L4	Z	Connect to external 12Kohm resistor
131	HDMI_CLK_P	O	K1	Z	HDMI differential CLK positive output
132	HDMI_CLK_N	O	K2	Z	HDMI differential CLK negative output
133	HDMI_CH0_P	O	L1	Z	HDMI differential CH0 positive output
134	HDMI_CH0_N	O	L2	Z	HDMI differential CH0 negative output
135	HDMI_CH1_P	O	M1	Z	HDMI differential CH1 positive output
136	HDMI_CH1_N	O	M2	Z	HDMI differential CH1 negative output
137	HDMI_CH2_P	O	N1	Z	HDMI differential CH2 positive output
138	HDMI_CH2_N	O	N2	Z	HDMI differential CH2 negative output
POR interface (1 pin) (VDD_BGPIO/VSS)					
139	RST_N_POR_OUT	AO	V8	Z	Power on reset output (open drain output)
RTC interface (3 pin) (VDD_RTC/VSS_RTC)					
140	RTC_XI	I	R1	Z	RTC crystal oscillator input
141	RTC_XO	O	R2	Z	RTC crystal oscillator output
142	RTC_INT	O	R3	Z	RTC interrupt output
SAR ADC interface (2 pin) (VDD_SADC/VSS)					
143	SADC_AUX0	AI	K14	Z	Auxiliary ADC input channel0
144	SADC_AUX1	AI	K17	Z	Auxiliary ADC input channel1
DDR3 interface (53 pin) (VDD_DRAM/VSS)					
145	DDR_RST_N	O	D5	Z	DDR3 reset (low active)
146	DDR_CKP	O	B10	Z	DDR3 differential clock positive
147	DDR_CKN	O	C10	Z	DDR3 differential clock negative
148	DDR_CKE	O	C9	Z	DDR3 clock enable
149	DDR_CS_N	O	D9	Z	DDR3 chip select (low active)
150	DDR_ODT	O	A9	Z	DDR3 on die termination
151	DDR_RAS_N	O	D10	Z	DDR3 RAS (low active)
152	DDR_CAS_N	O	B9	Z	DDR3 CAS (low active)
153	DDR_WE_N	O	C8	Z	DDR3 write enable (low active)
154-155	DDR_DM1~0	O	D14, D11	Z	DDR3 write data mask [1:0]
156-158	DDR_BA2~0	O	A7, C7, A8	Z	DDR3 bank address [2:0]
159-173	DDR_A14~0	O	B3, A3, B6, B4, D8, C5, A2, A4, C4, A5, D6, B7, B5, C6, A6	Z	DDR3 address [14:0]
174-175	DDR_DQS_P1~0	IO	A14, A11	Z	DDR3 data strobe[1:0] positive
176-177	DDR_DQS_N1~0	IO	B14, B11	Z	DDR3 data strobe[1:0] negative
178-185	DDR_DQ7~0	IO	A13, D13 C13, B13, A12, C12, B12, C11	Z	DDR3 input/output data [7:0]
186-193	DDR_DQ15~8	IO	C16, B16, A16, B15, A15, D15, C15, C14	Z	DDR3 input/output data [15:8]
194	DDR_ZQ	AI	B8	Z	DDR3 calibration
195	VDD_VREFDQ	AI	D12	Z	DDR3 PHY DQ reference voltage
196	VDD_VREFCA	AI	D7	Z	DDR3 PHY Command/Address reference voltage
197	DDR2_A3	O	A17	Z	DDR2 A3
Audio interface (10 pin) (AVDD_AUDIO /AVSS_AUDIO)					
198	MIC_LP	AI	W13	Z	Left differential microphone positive input

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
199	MIC_LN	AI	V13	Z	Left differential microphone negative input
200	MIC_RP	AI	W15	Z	Right differential microphone positive input
201	MIC_RN	AI	V15	Z	Right differential microphone negative input
202	PAUXL	AI	U13	Z	Left channel single-ended auxiliary input
203	PAUXR	AI	U14	Z	Right channel single-ended auxiliary input
204	MICBIAS_L	AO	V14	Z	Left microphone bias output
205	MICBIAS_R	AO	W14	Z	Right microphone bias output
206	LINEOUT	AO	U15	Z	Line amplifier positive output
207	PVREF	AO	T15	Z	Band-gap reference voltage output (A 10uF capacitor is recommended to connect to this pin)
USB (5 pin) (VDD_USB_3V3/VSS_USB)					
208	PUSB_DP	IO	T1	Z	USB2.0 D+
209	PUSB_DN	IO	U1	Z	USB2.0 D-
210	PUSB_RREF	AO	T5	Z	USB PHY external reference resistor (12K ohm +/-1%)
211	PUSB_ID	AI	T2	Z	USB plug indicator
212	PUSB_VBUS	AI	T3	Z	USB bus power
NC (2 pin) (VDD_DGPIO/VSS)					
213	PTEST_EN	ID	U17	LZ	For test mode only
214	PSCAN_EN	ID	T17	LZ	For test mode only
Power and Ground (90 pin)					
215-231	VDD_CORE	P	G9, G10, G11, H10, H11, J13, K7, K8, K13, L7, L8, L13, M10, M13, N10, N11,		Core power
232	VDD_CLK	P	C2		IO PAD power for Clock
233	VDD_SEN				IO PAD power for SENSOR
234	VDD_I2S	P			IO PAD power for I2S
235-236	VDD_LCD	P	J6, J7		IO PAD power for LCD
237	VDD_AGPIO				IO PAD power for GPIO groupA
238	VDD_BGPIO	P	P8		IO PAD power for GPIO groupB
239~240	VDD_CGPIO				IO PAD power for GPIO groupC
241	VDD_DGPIO	P	N13		IO PAD power for GPIO groupD
242-247	VDD_DRAM	P	F8, F9, F12, G8, G12, G13		IO PAD power for DRAM
248-249	VDD_DRAM_CORE	P	F10, F11		DRAM top core power
250	VDD_USB_1V1	P	U3		USB 1.1V power
251	VDD_USB_3V3	P	R4		USB 3.3V power
252-253	VSS_USB	G	N7, U2		USB ground
254	AVDD_PLL	P	H6		DPLL power
255	AVSS_PLL	G	H7		DPLL ground
256	AVDD_MIPI_RX0	P	M14		MIPI_RX0 power
257	AVDD_MIPI_RX1	P	L14		MIPI_RX1 power
258	AVDD_AUDIO	P	T13		Audio power
259~260	AVSS_AUDIO	G	T14, W16		Audio ground
261	AVDD_TV	P	N3		Video DAC power
262	AVSS_TV	G	N4		Video DAC ground
263	VDD11_TMDS	P	K6		HDMI transmitter 1.1V power
264	VDD33_TMDS	P	M6		HDMI transmitter 3.3V power

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
265	VDD33_HDMI	P	M4		HDMI analog 3.3V power
266-267	VSS_TMDS	G	L6, M3		HDMI transmitter ground
268	VDD_RTC	P	P1		RTC power
269	VSS_RTC	G	P2		RTC ground
270	VDD_POR_1V8	P	T9		POR detect 1.8V input power
271	VDD_SADC	P	K16		SAR ADC power
272-304	VSS	G	A10, B2, B17, C3, C17, G7, H8, H9, H12, H13, J8, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, L17, M7, M8, M9, M11, M12, N8, N9, N12, R17		Common ground (33 pins)

4.2 Pin Diagram (BGA304 AIT8328G)



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4.3 Pin Description (BGA277 AIT8328P)

I : Input pin
IO: Bidirection pin
ID: Input pin with pull-down configuration
IU: Input pin with pull-up configuration
IOU: Bidirection pin with pull-up configuration
IOD: Bidirection pin with pull-down configuration
O: Output pin
Z: Tri-state at reset
HZ: Tri-state Hi-Z at reset
LZ: Tri-state Lo-Z at reset

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
System Interface (11 pin) (VDD_AGPIO/VSS)					
1	PRST_N	I	W9	Z	Chip reset (low active)
2	PHI2C_SCL	IOU	W12	HZ	Host I2C slave clock
3	PHI2C_SDA	IOU	U12	HZ	Host I2C slave data
4	AGPIO0	IOD	W10	LZ	A-group GPIO0 (Download mode strapping bit0) {AGPIO6, AGPIO0}= 00: Serial flash (SPI type) 01: Serial flash (I2C type) 10: Internal ROM (32K) 11: Host I2C
5	AGPIO1	IOD	T10		A-group GPIO1 (I2C slave address strapping: 0:7'h3, 1:7'h4)
6	AGPIO2	IOD	U10		A-group GPIO2 (Boot-up CPU select strapping: 0:CPU A, 1:CPU B)
7	AGPIO3	IOD	V10	LZ	A-group GPIO3 (PLL boot auto switch boot strapping: 0:enable, 1: disable)
8	AGPIO4	IOD	U1	LZ	A-group GPIO4 CPU JTAG MODE[0] : CPU JTAG Multi-function select boot strapping '0' CPU A from Multi-function Set 0, CPU B from Set1, Chain mode from Set 0 if enabled '1' CPU A from Multi-function Set 1, CPU B from Set0, Chain mode from Set 1 if enabled
9	AGPIO5	IOD	V11	LZ	A-group GPIO5 CPU JTAG MODE[1] : CPU JTAG Chain mode boot strapping '0' JTAG chain mode enable '1' JTAG chain mode disable
10	AGPIO6	IOU	W11	HZ	A-group GPIO6 (Download mode strapping bit1) {AGPIO6, AGPIO0}= 00: Serial flash (SPI type) 01: Serial flash (I2C type) 10: Internal ROM (32K) 11: Host I2C
11	AGPIO7	IOD	T11	LZ	A-group GPIO7 CPU JTAG MODE[2] : CPU debug mode enable boot strapping '0' CPU Debug mode disable '1' CPU Debug mode enable Note: To enable CPU SRST debug mode, {AGPIO7,AGPIO6,APGIO0} = 3'b111;
Main Clock interface (2 pin) (VDD_CLK/VSS)					
12	XSCI	I	A2	Z	Crystal oscillator and main clock input
13	XSCO	O	A3	Z	Crystal oscillator output

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
I2S interface (5 pin) (VDD_I2S/VSS)					
14	PI2S_SCK	IOD	T13	LZ	I2S serial clock
15	PI2S_WS	IOD	W13	LZ	I2S word clock
16	PI2S_SDI	IOD	V12	LZ	I2S data input
17	PI2S_MCLK	IOD	U13	LZ	I2S master clock
18	PI2S_SDO	IOD	V13	LZ	I2S data output
Sensor Control Interface (11 pin) (VDD_SEN/VSS)					
19	PS_RST_N	IOD	N16	LZ	Sensor0 reset
20	PDCLK	IOD	M16	LZ	Sensor0 main clock
21	PSCK	IOD	L17	LZ	Sensor0 serial interface clock
22	PSDA	IOD	L16	LZ	Sensor0 serial interface data
23	PSEN	IOD	M17	LZ	Sensor0 enable
24	PPXL_CLK	IOD	L19	LZ	Sensor0 pixel clock
25	PVSYNC	IOD	L18	LZ	Sensor0 vertical sync
26	PHSYNC	IOD	K18	LZ	Sensor0 horizontal sync
27	PS_RST_N_1	IOD	K17	LZ	Sensor1 reset
28	PDCLK_1	IOD	K19	LZ	Sensor1 main clock
29	PSEN_1	IOD	J16	LZ	Sensor1 enable
MIPI_RX0 I/F (10 pin) (AVDD_MIPI_RX0/VSS)					
30	MIPI_RX_0_DA0P	AI	T19	Z	MIPI RX0 D-PHY positive data lane0 input Sensor 12-bit mode raw data [11] Sensor 10-bit mode raw data [9] Sensor 8-bit mode raw data [7]
31	MIPI_RX_0_DA0N	AI	T18	Z	MIPI RX0 D-PHY negative data lane0 input Sensor 12-bit mode raw data [10] Sensor 10-bit mode raw data [8] Sensor 8-bit mode raw data [6]
32	MIPI_RX_0_DA1P	AIZ	R19	Z	MIPI RX0 D-PHY positive data lane1 input Sensor 12-bit mode raw data [9] Sensor 10-bit mode raw data [7] Sensor 8-bit mode raw data [5]
33	MIPI_RX_0_DA1N	AI	R18	Z	MIPI RX0 D-PHY negative data lane1 input Sensor 12-bit mode raw data [8] Sensor 10-bit mode raw data [6] Sensor 8-bit mode raw data [4]
34	MIPI_RX_0_CKP	AI	P19	Z	MIPI RX0 D-PHY positive clock lane input Sensor 12-bit mode raw data [7] Sensor 10-bit mode raw data [5] Sensor 8-bit mode raw data [3]
35	MIPI_RX_0_CKN	AI	P18	Z	MIPI RX0 D-PHY negative clock lane input Sensor 12-bit mode raw data [6] Sensor 10-bit mode raw data [4] Sensor 8-bit mode raw data [2]
36	MIPI_RX_0_DA2P	AI	N19	Z	MIPI RX0 D-PHY positive data lane2 input Sensor 12-bit mode raw data [5] Sensor 10-bit mode raw data [3] Sensor 8-bit mode raw data [1]
37	MIPI_RX_0_DA2N	AI	N18	Z	MIPI RX0 D-PHY negative data lane2 input Sensor 12-bit mode raw data [4] Sensor 10-bit mode raw data [2] Sensor 8-bit mode raw data [0]
38	MIPI_RX_0_DA3P	AI	M19	Z	MIPI RX0 D-PHY positive data lane3 input Sensor 12-bit mode raw data [3]

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
					Sensor 10-bit mode raw data [1]
39	MIPI_RX_0_DA3N	AI	M18	Z	MIPI RX0 D-PHY negative data lane3 input Sensor 12-bit mode raw data [2] Sensor 10-bit mode raw data [0]
MIPI_RX1 I/F (6 pin) (AVDD_MIPI_RX1/VSS)					
40	MIPI_RX_1_DA1P	AI	J19	Z	MIPI RX1 D-PHY positive data lane1 input Sensor 12-bit mode raw data [1]
41	MIPI_RX_1_DA1N	AI	J18	Z	MIPI RX1 D-PHY negative data lane1 input Sensor 12-bit mode raw data [0]
42	MIPI_RX_1_CKP	AI	H19	Z	MIPI RX1 D-PHY positive clock lane input
43	MIPI_RX_1_CKN	AI	H18	Z	MIPI RX1 D-PHY negative clock lane input
44	MIPI_RX_1_DA2P	AI	G19	Z	MIPI RX1 D-PHY positive data lane2 input
45	MIPI_RX_1_DA2N	AI	G18	Z	MIPI RX1 D-PHY negative data lane2 input
BGPIO interface (23 pin) (VDD_BGPIO/VSS)					
46	BGPIO0	IOD	U3	LZ	B-group GPIO10 SIF clock
47	BGPIO1	IOU	V1	HZ	B-group GPIO11 SIF chip select
48	BGPIO2	IOD	U4	LZ	B-group GPIO12 SIF data output
49	BGPIO3	IOD	W1	LZ	B-group GPIO13 SIF data input
50	BGPIO4	IOD	V2	LZ	B-group GPIO14 SIF WP_N
51	BGPIO5	IOD	W2	LZ	B-group GPIO15 SIF HOLD_N
52	BGPIO6	IOD	T5	LZ	B-group GPIO16
53	BGPIO7	IOD	W3	LZ	B-group GPIO17
54	BGPIO8	IOD	V3	LZ	B-group GPIO18
55	BGPIO9			LZ	B-group GPIO19
56	BGPIO10	IOD		LZ	B-group GPIO20
57	BGPIO11				
58	BGPIO12				
59	BGPIO13				
60	BGPIO14			LZ	B-group GPIO24
61	BGPIO15	IOD	V6	LZ	B-group GPIO25
62	BGPIO16	IOD	U6	LZ	B-group GPIO26
63	BGPIO17	IOD	W6	LZ	B-group GPIO27
64	BGPIO18	IOD	T7	LZ	B-group GPIO28
65	BGPIO19	IOD	V7	LZ	B-group GPIO29
66	BGPIO20	IOD	U7	LZ	B-group GPIO30
67	BGPIO21	IOD	W7	LZ	B-group GPIO31
68	POR_OPT	I	N8	Z	Power-on reset option (0:external, 1:internal)
CGPIO interface (32 pin) (VDD_CGPIO/VSS)					
69	CGPIO0	IOD	F17	LZ	C-group GPIO32
70	CGPIO1	IOD	G17	LZ	C-group GPIO33
71	CGPIO2	IOD	F16	LZ	C-group GPIO34
72	CGPIO3	IOD	F18	LZ	C-group GPIO35
73	CGPIO4	IOD	E19	LZ	C-group GPIO36
74	CGPIO5	IOD	E18	LZ	C-group GPIO37
75	CGPIO6	IOD	D19	LZ	C-group GPIO38
76	CGPIO7	IOD	C18	LZ	C-group GPIO39

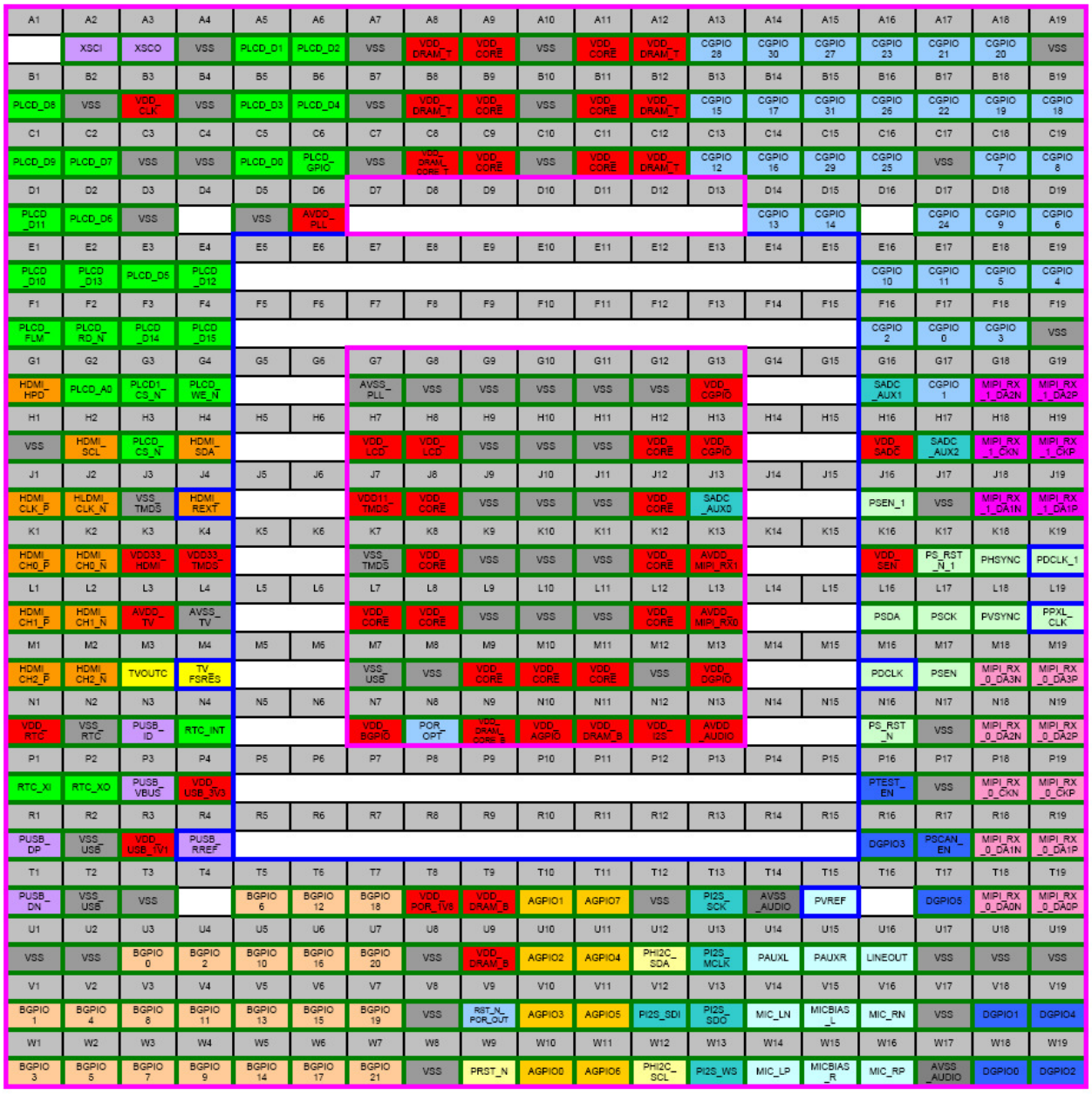
Pin Num	Pin Name	Type	Loc.	Rst# state	Description
77	CGPIO8	IOD	C19	LZ	C-group GPIO40
78	CGPIO9	IOD	D18	LZ	C-group GPIO41
79	CGPIO10	IOD	E16	LZ	C-group GPIO42
80	CGPIO11	IOD	E17	LZ	C-group GPIO43
81	CGPIO12	IOD	C13	LZ	C-group GPIO44
82	CGPIO13	IOD	D14	LZ	C-group GPIO45
83	CGPIO14	IOD	D15	LZ	C-group GPIO46
84	CGPIO15	IOD	B13	LZ	C-group GPIO47
85	CGPIO16	IOD	C14	LZ	C-group GPIO48
86	CGPIO17	IOD	B14	LZ	C-group GPIO49
87	CGPIO18	IOD	B19	LZ	C-group GPIO50
88	CGPIO19	IOD	B18	LZ	C-group GPIO51
89	CGPIO20	IOD	A18	LZ	C-group GPIO52
90	CGPIO21	IOD	A17	LZ	C-group GPIO53
91	CGPIO22	IOD	B17	LZ	C-group GPIO54
92	CGPIO23	IOD	A16	LZ	C-group GPIO55
93	CGPIO24	IOD	D17	LZ	C-group GPIO56
94	CGPIO25	IOD	C16	LZ	C-group GPIO57
95	CGPIO26	IOD	B16	LZ	C-group GPIO58
96	CGPIO27	IOD	A15	LZ	C-group GPIO59
97	CGPIO28	IOD	A13	LZ	C-group GPIO60
98	CGPIO29	IOD	C15	LZ	C-group GPIO61
99	CGPIO30	IOD	A14	LZ	C-group GPIO62
100	CGPIO31	IOD	B15	LZ	C-group GPIO63
DGPIO interface (6 pin) (VDD_DGPIO/VSS)					
101	DGPIO0	IOD	W18	LZ	D-group GPIO64
102	DGPIO1	IOD	V18	LZ	D-group GPIO65
103	DGPIO2	IOD	W19	LZ	D-group GPIO66
104	DGPIO3		R16	LZ	D-group GPIO67
105	DGPIO4				
106	DGPIO5				
107-122	PLCD_D15~0	IOD	F4,F3, E2,E4, D1,E1, C1,B1, C2,D2, E3,B6, B5,A6, A5,C5	LZ	LCD data [15:0] LCD[0]: software boot-strapping debug mode LCD[1]: software boot-strapping USB full/high-speed select LCD[2]: software boot-strapping USB PID/VID select LCD[5:3]: software boot-strapping options
123	PLCD_WE_N	IO	G4	Z	LCD write signal
124	PLCD_A0	IO	G2	Z	LCD command or data selection
125	PLCD_RD_N	IO	F2	Z	LCD read signal
126	PLCD_CS_N	IO	H3	Z	LCD enable
127	PLCD1_CS_N	IO	G3	Z	LCD1 enable
128	PLCD_FLM	IOD	F1	LZ	LCD frame sync control
129	PLCD_GPIO	IOD	C6	LZ	LCD GPIO
TV out (2 pin) (AVDD_TV/AVSS_TV)					
130	TVOUTC	AO	M3	Z	TV composite current out
131	TV_FSRES	AI	M4	Z	TV_FSRES out
HDMI (12 pins) (VDD11_TMDS/VDD33_HDMI/VDD33_TMDS/VSS_TMDS)					
132	HDMI_HPD	I/O	G1	Z	HDMI hot plug detect
133	HDMI_SCL	I/O	H2	Z	HDMI serial interface clock

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
134	HDMI_SDA	I/O	H4	Z	HDMI serial interface data
135	HDMI_REXT	O	J4	Z	Connect to external 12Kohm resistor
136	HDMI_CLK_P	O	J1	Z	HDMI differential CLK positive output
137	HDMI_CLK_N	O	J2	Z	HDMI differential CLK negative output
138	HDMI_CH0_P	O	K1	Z	HDMI differential CH0 positive output
139	HDMI_CH0_N	O	K2	Z	HDMI differential CH0 negative output
140	HDMI_CH1_P	O	L1	Z	HDMI differential CH1 positive output
141	HDMI_CH1_N	O	L2	Z	HDMI differential CH1 negative output
142	HDMI_CH2_P	O	M1	Z	HDMI differential CH2 positive output
143	HDMI_CH2_N	O	M2	Z	HDMI differential CH2 negative output
POR interface (1 pin) (VDD_BGPIO/VSS)					
144	RST_N_POR_OUT	AO	V9	Z	Power on reset output (open drain output)
RTC interface (3 pin) (VDD_RTC/VSS_RTC)					
145	RTC_XI	I	P1	Z	RTC crystal oscillator input
146	RTC_XO	O	P2	Z	RTC crystal oscillator output
147	RTC_INT	O	N4	Z	RTC interrupt output
SAR ADC interface (3 pin) (VDD_SADC/VSS)					
148	SADC_AUX0	AI	J13	Z	Auxiliary ADC input channel0
149	SADC_AUX1	AI	G16	Z	Auxiliary ADC input channel1
150	SADC_AUX2	AI	H17	Z	Auxiliary ADC input channel2
Audio interface (10 pin) (AVDD_AUDIO /AVSS_AUDIO)					
151	MIC_LP	AI	W14	Z	Left differential microphone positive input
152	MIC_LN	AI	V14	Z	Left differential microphone negative input
153	MIC_RP	AI	W16	Z	Right differential microphone positive input
154	MIC_RN	AI	V16	Z	Right differential microphone negative input
155	PAUXL	AI	U14	Z	Left channel single-ended auxiliary input
156	PAUXR	AI	U15	Z	Right channel single-ended auxiliary input
157	MICBIAS_L	AO	V15	Z	Left microphone bias output
158	MICBIAS_R			Z	Right microphone bias output
159	LINEOUT	AO	U16	Z	Line amplifier positive output
160	PVREF	AO	T15	Z	Band-gap reference voltage output (A 10uF capacitor is recommended to connect to this pin)
USB (5 pin) (VDD_USB_3V3/VSS_USB)					
161	PUSB_DP	IO	R1	Z	USB2.0 D+
162	PUSB_DN	IO	T1	Z	USB2.0 D-
163	PUSB_RREF	AO	R4	Z	USB PHY external reference resistor (12K ohm +/-1%)
164	PUSB_ID	AI	N3	Z	USB plug indicator
165	PUSB_VBUS	AI	P3	Z	USB bus power
NC (2 pin) (VDD_DGPIO/VSS)					
166	PTEST_EN	ID	P16	LZ	For test mode only
167	PSCAN_EN	ID	R17	LZ	For test mode only
Power and Ground (110 pin)					
168-184	VDD_CORE	P	A9.A11, B9,B11, C9,C11, H12,J8, J12,K8, K12,L7, L8,L12, M9,M10, M11		Core power (17 pins)
185	VDD_CLK	P	B3		IO PAD power for Clock
186	VDD_SEN	P	K16		IO PAD power for SENSOR

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
187	VDD_I2S	P	N12		IO PAD power for I2S
188-189	VDD_LCD	P	H7,H8		IO PAD power for LCD
190	VDD_AGPIO	P	N10		IO PAD power for GPIO groupA
191	VDD_BGPIO	P	N7		IO PAD power for GPIO groupB
192-193	VDD_CGPIO	P	G13,H13		IO PAD power for GPIO groupC
194	VDD_DGPIO	P	M13		IO PAD power for GPIO groupD
195-199	VDD_DRAM_T	P	A8,A12, B8,B12, C12		IO PAD power for DRAM top side
200-202	VDD_DRAM_B	P	N11,T9, U9		IO PAD power for DRAM bottom side
203	VDD_DRAM_CORE_T	P	C8		DRAM top core power
204	VDD_DRAM_CORE_B	P	N9		DRAM bottom core power
205	VDD_USB_1V1	P	R3		USB 1.1V power
206	VDD_USB_3V3	P	P4		USB 3.3V power
207-209	VSS_USB	G	M7,R2, T2		USB ground
210	AVDD_PLL	P	D6		DPLL power
211	AVSS_PLL	G	G7		DPLL ground
212	AVDD_MIPI_RX0	P	L13		MIPI_RX0 power
213	AVDD_MIPI_RX1	P	K13		MIPI_RX1 power
214	AVDD_AUDIO	P	N13		Audio power
215-216	AVSS_AUDIO	G	T14,W17		Audio ground
217	AVDD_TV	P	L3		Video DAC power
218	AVSS_TV	G	L4		Video DAC ground
219	VDD11_TMDS	P	J7		HDMI transmitter 1.1V power
220	VDD33_TMDS	P	K4		HDMI transmitter 3.3V power
221	VDD33_HDMI	P	K3		HDMI analog 3.3V power
222-223	VSS_TMDS	G	J3,K7		HDMI transmitter ground
224	VDD_RTC				
225	VSS_RTC	G	N2		RTC ground
226	VDD_POR_1V8	P	T8		POR detect 1.8V input power
227	VDD_SADC				
228-277	VSS	G	A4,A7, A10,A19, B2,B4, B7,B10, C3,C4, C7,C10, C17,D3, D5,F19, G8,G9, G10,G11, G12,H1, H9,H10, H11,J9, J10,J11, J17,K9, K10,K11, L9,L10, L11,M8, M12,N17, P17,T3, T12,U1, U2,U8, U17,U18,		Common ground (50 pins)

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
			U19,V8, V17,W8		

4.4 Pin Diagram (BGA277 AIT8328P)



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4.5 Pin Description (BGA338 AIT8328Q) (Preliminary)

I : Input pin
IO: Bidirection pin
ID: Input pin with pull-down configuration
IU: Input pin with pull-up configuration
IOU: Bidirection pin with pull-up configuration
IOD: Bidirection pin with pull-down configuration
O: Output pin
Z: Tri-state at reset
HZ: Tri-state Hi-Z at reset
LZ: Tri-state Lo-Z at reset

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
System Interface (11 pin) (VDD_AGPIO/VSS)					
1	PRST_N	I	AB12	Z	Chip reset (low active)
2	PHI2C_SCL	IOU	Y14	HZ	Host I2C slave clock
3	PHI2C_SDA	IOU	AA14	HZ	Host I2C slave data
4	AGPIO0	IOD	AB13	LZ	A-group GPIO0 (Download mode strapping bit0) {AGPIO6, AGPIO0}= 00: Serial flash (SPI type) 01: Serial flash (I2C type) 10: Internal ROM (32K) 11: Host I2C
5	AGPIO1	IOD	W13	LZ	A-group GPIO1 (I2C slave address strapping: 0:7'h3, 1:7'h4)
6	AGPIO2	IOD	Y12	LZ	A-group GPIO2 (Boot-up CPU select strapping: 0:CPU A, 1:CPU B)
7	AGPIO3	IOD	W12	LZ	A-group GPIO3 (PLL boot auto switch boot strapping: 0:enable, 1: disable)
8	AGPIO4	IOD	Y13	LZ	A-group GPIO4 CPU JTAG MODE[0] : CPU JTAG Multi-function select boot strapping '0' CPU A from Multi-function Set 0, CPU B from Set1, Chain mode from Set 0 if enabled '1' CPU A from Multi-function Set 1, CPU B from Set0, Chain mode from Set 1 if enabled
9	AGPIO5	IOD	AA13	LZ	A-group GPIO5 CPU JTAG MODE[1] : CPU JTAG Chain mode boot strapping '0' JTAG chain mode enable '1' JTAG chain mode disable
10	AGPIO6	IOU	AB14	HZ	A-group GPIO6 (Download mode strapping bit1) {AGPIO6, AGPIO0}= 00: Serial flash (SPI type) 01: Serial flash (I2C type) 10: Internal ROM (32K) 11: Host I2C
11	AGPIO7	IOD	W14	LZ	A-group GPIO7 CPU JTAG MODE[2] : CPU debug mode enable boot strapping '0' CPU Debug mode disable '1' CPU Debug mode enable Note: To enable CPU SRST debug mode, {AGPIO7,AGPIO6,APGIO0} = 3'b111;
Main Clock interface (2 pin) (VDD_CLK/VSS)					
12	XSCI	I	K1	Z	Crystal oscillator and main clock input
13	XSCO	O	K2	Z	Crystal oscillator output
I2S interface (5 pin) (VDD_I2S/VSS)					

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
14	PI2S_SCK	IOD	AB15	LZ	I2S serial clock
15	PI2S_WS	IOD	AA15	LZ	I2S word clock
16	PI2S_SDI	IOD	Y15	LZ	I2S data input
17	PI2S_MCLK	IOD	AA16	LZ	I2S master clock
18	PI2S_SDO	IOD	W15	LZ	I2S data output
Sensor Control Interface (11 pin) (VDD_SEN/VSS)					
19	PS_RST_N	IOD	U19	LZ	Sensor0 reset
20	PDCLK	IOD	V19	LZ	Sensor0 main clock
21	PSCK	IOD	T22	LZ	Sensor0 serial interface clock
22	PSDA	IOD	R21	LZ	Sensor0 serial interface data
23	PSEN	IOD	P21	LZ	Sensor0 enable
24	PPXL_CLK	IOD	R22	LZ	Sensor0 pixel clock
25	PVSYNC	IOD	T20	LZ	Sensor0 vertical sync
26	PHSYNC	IOD	T21	LZ	Sensor0 horizontal sync
27	PS_RST_N_1	IOD	N21	LZ	Sensor1 reset
28	PDCLK_1	IOD	P22	LZ	Sensor1 main clock
29	PSEN_1	IOD	N22	LZ	Sensor1 enable
MIPI_RX0 I/F (10 pin) (AVDD_MIPI_RX0/VSS)					
30	MIPI_RX_0_DA0P	AI	AA22	Z	MIPI RX0 D-PHY positive data lane0 input Sensor 12-bit mode raw data [11] Sensor 10-bit mode raw data [9] Sensor 8-bit mode raw data [7]
31	MIPI_RX_0_DA0N	AI	AA21	Z	MIPI RX0 D-PHY negative data lane0 input Sensor 12-bit mode raw data [10] Sensor 10-bit mode raw data [8] Sensor 8-bit mode raw data [6]
32	MIPI_RX_0_DA1P	AI	Y22	Z	MIPI RX0 D-PHY positive data lane1 input Sensor 12-bit mode raw data [9] Sensor 10-bit mode raw data [7] Sensor 8-bit mode raw data [5]
33	MIPI_RX_0_DA1N				MIPI RX0 D-PHY negative data lane1 input Sensor 12-bit mode raw data [8] Sensor 10-bit mode raw data [6] Sensor 8-bit mode raw data [4]
34	MIPI_RX_0_CKP	AI	W22	Z	MIPI RX0 D-PHY positive clock lane input Sensor 12-bit mode raw data [7] Sensor 10-bit mode raw data [5] Sensor 8-bit mode raw data [3]
35	MIPI_RX_0_CKN	AI	W21	Z	MIPI RX0 D-PHY negative clock lane input Sensor 12-bit mode raw data [6] Sensor 10-bit mode raw data [4] Sensor 8-bit mode raw data [2]
36	MIPI_RX_0_DA2P	AI	V22	Z	MIPI RX0 D-PHY positive data lane2 input Sensor 12-bit mode raw data [5] Sensor 10-bit mode raw data [3] Sensor 8-bit mode raw data [1]
37	MIPI_RX_0_DA2N	AI	V21	Z	MIPI RX0 D-PHY negative data lane2 input Sensor 12-bit mode raw data [4] Sensor 10-bit mode raw data [2] Sensor 8-bit mode raw data [0]
38	MIPI_RX_0_DA3P	AI	U22	Z	MIPI RX0 D-PHY positive data lane3 input Sensor 12-bit mode raw data [3] Sensor 10-bit mode raw data [1]

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
39	MIPI_RX_0_DA3N	AI	U21	Z	MIPI RX0 D-PHY negative data lane3 input Sensor 12-bit mode raw data [2] Sensor 10-bit mode raw data [0]
MIPI_RX1 I/F (6 pin) (AVDD_MIPI_RX1/VSS)					
40	MIPI_RX_1_DA1P	AI	M22	Z	MIPI RX1 D-PHY positive data lane1 input Sensor 12-bit mode raw data [1]
41	MIPI_RX_1_DA1N	AI	M21	Z	MIPI RX1 D-PHY negative data lane1 input Sensor 12-bit mode raw data [0]
42	MIPI_RX_1_CKP	AI	L22	Z	MIPI RX1 D-PHY positive clock lane input
43	MIPI_RX_1_CKN	AI	L21	Z	MIPI RX1 D-PHY negative clock lane input
44	MIPI_RX_1_DA2P	AI	K22	Z	MIPI RX1 D-PHY positive data lane2 input
45	MIPI_RX_1_DA2N	AI	K21	Z	MIPI RX1 D-PHY negative data lane2 input
BGPIO interface (23 pin) (VDD_BGPIO/VSS)					
46	BGPIO0	IOD	AA3	LZ	B-group GPIO10 SIF clock
47	BGPIO1	IOU	AA4	HZ	B-group GPIO11 SIF chip select
48	BGPIO2	IOD	AB3	LZ	B-group GPIO12 SIF data output
49	BGPIO3	IOD	AB2	LZ	B-group GPIO13 SIF data input
50	BGPIO4	IOD	AB5	LZ	B-group GPIO14 SIF WP_N
51	BGPIO5	IOD	AB4	LZ	B-group GPIO15 SIF HOLD_N
52	BGPIO6	IOD	AB7	LZ	B-group GPIO16
53	BGPIO7	IOD	AB6	LZ	B-group GPIO17
54	BGPIO8	IOD	AA5	LZ	B-group GPIO18
55	BGPIO9	IOD	AA6	LZ	B-group GPIO19
56	BGPIO10			LZ	B-group GPIO20
57	BGPIO11	IOD	AA7	LZ	B-group GPIO21
58	BGPIO12				
59	BGPIO13				
60	BGPIO14				
61	BGPIO15			LZ	B-group GPIO25
62	BGPIO16	IOD	Y10	LZ	B-group GPIO26
63	BGPIO17	IOD	AB10	LZ	B-group GPIO27
64	BGPIO18	IOD	Y11	LZ	B-group GPIO28
65	BGPIO19	IOD	AA11	LZ	B-group GPIO29
66	BGPIO20	IOD	AB11	LZ	B-group GPIO30
67	BGPIO21	IOD	AA9	LZ	B-group GPIO31
68	POR_OPT	I	V11	Z	Power-on reset option (0:external, 1:internal)
CGPIO interface (32 pin) (VDD_CGPIO/VSS)					
69	CGPIO0	IOD	P19	LZ	C-group GPIO32
70	CGPIO1	IOD	P20	LZ	C-group GPIO33
71	CGPIO2	IOD	H19	LZ	C-group GPIO34
72	CGPIO3	IOD	J19	LZ	C-group GPIO35
73	CGPIO4	IOD	N19	LZ	C-group GPIO36
74	CGPIO5	IOD	H22	LZ	C-group GPIO37
75	CGPIO6	IOD	M19	LZ	C-group GPIO38
76	CGPIO7	IOD	H21	LZ	C-group GPIO39
77	CGPIO8	IOD	G22	LZ	C-group GPIO40

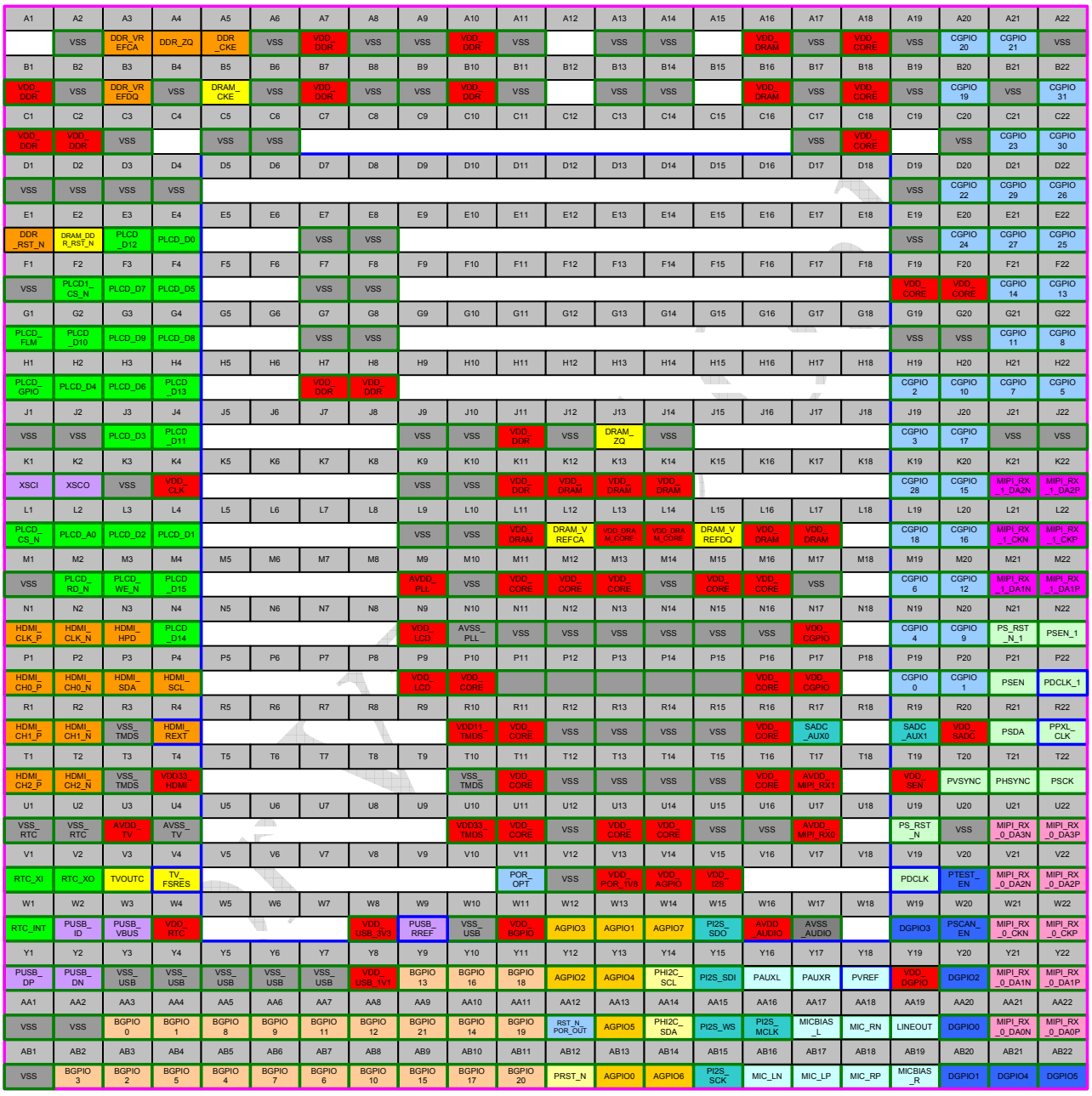
Pin Num	Pin Name	Type	Loc.	Rst# state	Description
78	CGPIO9	IOD	N20	LZ	C-group GPIO41
79	CGPIO10	IOD	H20	LZ	C-group GPIO42
80	CGPIO11	IOD	G21	LZ	C-group GPIO43
81	CGPIO12	IOD	M20	LZ	C-group GPIO44
82	CGPIO13	IOD	F22	LZ	C-group GPIO45
83	CGPIO14	IOD	F21	LZ	C-group GPIO46
84	CGPIO15	IOD	K20	LZ	C-group GPIO47
85	CGPIO16	IOD	L20	LZ	C-group GPIO48
86	CGPIO17	IOD	J20	LZ	C-group GPIO49
87	CGPIO18	IOD	L19	LZ	C-group GPIO50
88	CGPIO19	IOD	B20	LZ	C-group GPIO51
89	CGPIO20	IOD	A20	LZ	C-group GPIO52
90	CGPIO21	IOD	A21	LZ	C-group GPIO53
91	CGPIO22	IOD	D20	LZ	C-group GPIO54
92	CGPIO23	IOD	C21	LZ	C-group GPIO55
93	CGPIO24	IOD	E20	LZ	C-group GPIO56
94	CGPIO25	IOD	E22	LZ	C-group GPIO57
95	CGPIO26	IOD	D22	LZ	C-group GPIO58
96	CGPIO27	IOD	E21	LZ	C-group GPIO59
97	CGPIO28	IOD	K19	LZ	C-group GPIO60
98	CGPIO29	IOD	D21	LZ	C-group GPIO61
99	CGPIO30	IOD	C22	LZ	C-group GPIO62
100	CGPIO31	IOD	B22	LZ	C-group GPIO63
DGPIO interface (6 pin) (VDD_DGPIO/VSS)					
101	DGPIO0	IOD	AA20	LZ	D-group GPIO64
102	DGPIO1	IOD	AB20	LZ	D-group GPIO65
103	DGPIO2	IOD	Y20	LZ	D-group GPIO66
104	DGPIO3	IOD	W19	LZ	D-group GPIO67
105	DGPIO4				
106	DGPIO5	IOD	AB22	LZ	D-group GPIO69
LCD interface (23 pin) (VDD_LCD/VSS)					
107-122	PLCD_D15~0		M4, N4, H4, E3, J4, G2, G3, G4, F3, H3, F4, H2, J3, L3, L4, E4.		LCD data [15:0] LCD[0]: software boot-strapping debug mode LCD[1]: software boot-strapping USB full/high-speed select LCD[2]: software boot-strapping USB PID/VID select LCD[5:3]: software boot-strapping options
123	PLCD_WE_N	IO	M3	Z	LCD write signal
124	PLCD_A0	IO	L2	Z	LCD command or data selection
125	PLCD_RD_N	IO	M2	Z	LCD read signal
126	PLCD_CS_N	IO	L1	Z	LCD enable
127	PLCD1_CS_N	IO	F2	Z	LCD1 enable
128	PLCD_FLM	IOD	G1	LZ	LCD frame sync control
129	PLCD_GPIO	IOD	H1	LZ	LCD GPIO
TV out (2 pin) (AVDD_TV/AVSS_TV)					
130	TVOUTC	AO	V3	Z	TV composite current out
131	TV_FSRES	AI	V4	Z	TV_FSRES out
HDMI (12 pins) (VDD11_TMDS/VDD33_HDMI/VDD33_TMDS/VSS_TMDS)					
132	HDMI_HPD	I/O	N3	Z	HDMI hot plug detect
133	HDMI_SCL	I/O	P4	Z	HDMI serial interface clock
134	HDMI_SDA	I/O	P3	Z	HDMI serial interface data

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
135	HDMI_REXT	O	R4	Z	Connect to external 12Kohm resistor
136	HDMI_CLK_P	O	N1	Z	HDMI differential CLK positive output
137	HDMI_CLK_N	O	N2	Z	HDMI differential CLK negative output
138	HDMI_CH0_P	O	P1	Z	HDMI differential CH0 positive output
139	HDMI_CH0_N	O	P2	Z	HDMI differential CH0 negative output
140	HDMI_CH1_P	O	R1	Z	HDMI differential CH1 positive output
141	HDMI_CH1_N	O	R2	Z	HDMI differential CH1 negative output
142	HDMI_CH2_P	O	T1	Z	HDMI differential CH2 positive output
143	HDMI_CH2_N	O	T2	Z	HDMI differential CH2 negative output
POR interface (1 pin) (VDD_BGPIO/VSS)					
144	RST_N_POR_OUT	AO	AA12	Z	Power on reset output (open drain output)
RTC interface (3 pin) (VDD_RTC/VSS_RTC)					
145	RTC_XI	I	V1	Z	RTC crystal oscillator input
146	RTC_XO	O	V2	Z	RTC crystal oscillator output
147	RTC_INT	O	W1	Z	RTC interrupt output
SAR ADC interface (2 pin) (VDD_SADC/VSS)					
148	SADC_AUX0	AI	R17	Z	Auxiliary ADC input channel0
149	SADC_AUX1	AI	R19	Z	Auxiliary ADC input channel1
Audio interface (10 pin) (AVDD_AUDIO /AVSS_AUDIO)					
150	MIC_LP	AI	AB17	Z	Left differential microphone positive input
151	MIC_LN	AI	AB16	Z	Left differential microphone negative input
152	MIC_RP	AI	AB18	Z	Right differential microphone positive input
153	MIC_RN	AI	AA18	Z	Right differential microphone negative input
154	PAUXL	AI	Y16	Z	Left channel single-ended auxiliary input
155	PAUXR	AI	Y17	Z	Right channel single-ended auxiliary input
156	MICBIAS_L	AO	AA17	Z	Left microphone bias output
157	MICBIAS_R	AO	AB19	Z	Right microphone bias output
158	LINEOUT	AO	AA19	Z	Line amplifier positive output
159	PVREF				Band-gap reference voltage output (A 10uF capacitor is recommended to connect to this pin)
USB (5 pin) (VDD_USB_3V3/VSS_USB)					
160	PUSB_DP	IO	Y1	Z	USB2.0 D+
161	PUSB_DN		Y2	Z	USB2.0 D-
162	PUSB_RREF	AO	W9	Z	USB PHY external reference resistor (12K ohm +/-1%)
163	PUSB_ID			Z	USB plug indicator
164	PUSB_VBUS	AI	W3	Z	USB bus power
Stack DDR3 (10 pin)					
165	DDR_RST_N	I	E1	Z	DDR3 reset (dram chip input)
166	DRAM_RST_N	O	E2	Z	DDR3 reset (main chip output)
167	DDR_CKE	I	A5	Z	DDR3 clock enable (dram chip input)
168	DRAM_CKE	O	B5	Z	DDR3 clock enable (main chip output)
169	DDR_ZQ	AI	A4	Z	DDR3 calibration (dram chip input) (240 ohm to GND)
170	DRAM_ZQ	AI	J13	Z	DDR3 calibration (main chip input) (240 ohm to GND)
171	DDR_VREFDQ	AI	B3	Z	DDR3 PHY DQ reference voltage (dram chip input)
172	DRAM_VREFDQ	AI	L15	Z	DDR3 PHY DQ reference voltage (main chip input)
173	DDR_VREFCA	P	A3	Z	DDR3 PHY CMD/ADDR reference voltage (dram chip input)
174	DRAM_VREFCA	P	L12	Z	DDR3 PHY CMD/ADDR reference voltage (main chip input)
NC (2 pin) (VDD_DGPIO/VSS)					
175	PTEST_EN	ID	V20	LZ	For test mode only
176	PSCAN_EN	ID	W20	LZ	For test mode only
Power and Ground (110 pin)					
177-	VDD_CORE	P	A18, B18,		Core power (19 pins)

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
195			C18, F19, F20, M11, M12, M13, M15, M16, P10, P16, R11, R16, T11, T16, U11, U13, U14		
196	VDD_CLK	P	K4		IO PAD power for Clock
197	VDD_SEN	P	T19		IO PAD power for SENSOR
198	VDD_I2S	P	V15		IO PAD power for I2S
199-200	VDD_LCD	P	N9, P9		IO PAD power for LCD
201	VDD_AGPIO	P	V14		IO PAD power for GPIO groupA
202	VDD_BGPIO	P	W11		IO PAD power for GPIO groupB
203-204	VDD_CGPIO	P	N17, P17		IO PAD power for GPIO groupC
205	VDD_DGPIO	P	Y19		IO PAD power for GPIO groupD
206-213	VDD_DRAM	P	A16, B16, K12, K13, K14, L11, L16, L17		IO PAD power for DRAM
214-224	VDD_DDR	P	A7, A10, B1, B7, B10, C1, C2, H7, H8, J11, K11		DDR3 chip power
225-226	VDD_DRAM_CORE	P	L13, L14		DRAM core power
227	VDD_USB_1V1	P	Y8		USB 1.1V power
228	VDD_USB_3V3	P	W8		USB 3.3V power
229-234	VSS_USB		W10, Y3 Y4, Y5, Y6, Y7		
235	AVDD_PLL	P	M9		DPLL power
236	AVSS_PLL				
237	AVDD_MIPI_RX0	P	U17		MIPI_RX0 power
238	AVDD_MIPI_RX1	P	T17		MIPI_RX1 power
239	AVDD_AUDIO				
240	AVSS_AUDIO	G	W17		Audio ground
241	AVDD_TV	P	U3		Video DAC power
242	AVSS_TV	G	U4		Video DAC ground
243	VDD11_TMDS	P	R10		HDMI transmitter 1.1V power
244	VDD33_TMDS	P	U10		HDMI transmitter 3.3V power
245	VDD33_HDMI	P	T4		HDMI analog 3.3V power
246-248	VSS_TMDS	G	R3, T3, T10		HDMI transmitter ground
249	VDD_RTC	P	W4		RTC power
250-251	VSS_RTC	G	U1, U2		RTC ground
252	VDD_POR_1V8	P	V13		POR detect 1.8V input power
253	VDD_SADC	P	R20		SAR ADC power
254-338	VSS	G	A2, A6, A8, A9, A11, A13, A14, A17, A19, A22, B2, B4,		Common ground (85 pins)

Pin Num	Pin Name	Type	Loc.	Rst# state	Description
			B6, B8, B9, B11, B13, B14, B17, B19, B21, C3, C5, C6, C17, C20, D1, D2, D3, D4, D19, E7, E8, E19, F1, F7, F8, G7, G8, G19, G20, J1, J2, J9, J10, J12, J14, J21, J22, K3, K9, K10, L9, L10, M1, M10, M14, M17, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, R12, R13, R14, R15, T12, T13, T14, T15, U12, U15, U16, U20, V12, AA1, AA2, AB1		

4.6 Pin Diagram (BGA338 AIT8328Q) (Preliminary)



0.1d

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Core Voltage	VDDmax	-0.3	1.3	V
Supply IO Voltage	VDDIOmax	-0.5	3.7	V
IO Signal Voltage	VIOmax	-0.5	VDDIO[1]+0.3	V
ESD (human body mode)	ESD-HBM	<-2.0	>2.0	KV
ESD (machine mode)	ESD-MM	<-200	>200	V
Latch-Up		<-100	>100	mA
Storage Temperature	Tstorage	-40	125	℃
Operation Temperature	Toperate	-10	85	℃
Junction Temperature	Tjunction	-40	125	℃

Table 1. Absolute Maximum Ratings

[1] The voltage depends on different power group

* Permanent device damage may occur if the absolute maximum ratings are exceeded

5.2 DC Recommended Operating Conditions

Symbol	Parameter	For 1.8V I/O			For 2.5V I/O			For 3.3V I/O		
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
VDD (V)	Core power supply	0.99	1.1	1.21	0.99	1.1	1.21	0.99	1.1	1.21
VDDIO (V)	IO power supply	1.62	1.8	1.98	2.25	2.5	2.75	2.97	3.3	3.63
Temp (°C)	Junction temperature	-40	25	125	-40	25	125	-40	25	125
-	Hyteresis	0.2		0.3	0.2		0.3	0.25		0.35
V_{IL} (V)	Input low voltage			0.6			0.7			0.8
V_{IH} (V)	Input high Voltage	1.2			1.7			2.0		
V_{OL} (V)	Output low voltage			0.4			0.4			0.4
V_{OH} (V)	Output high voltage	VDDIO-0.4			VDDIO-0.4			VDDIO-0.4		
I_{LI} (uA)	Input leakage current	-10		+10	-10		+10	-10		+10
I_{LO} (uA)	Output leakage current	-10		+10	-10		+10	-10		+10
Pull-up (kohm)	Pull-up resistor		90			54			38	
Pull-down (kohm)	Pull-down resistor		90			54			38	

Table 2. I/O electrical characteristics

Symbols	Min.	Typ.	Max.	Unit	Note
VDD_CORE	1.05	1.1	1.3		
VDD_CLK	1.7		3.6	V	
VDD_SEN	1.62	1.8	1.98		
VDD_I2S	1.7		3.6	V	
VDD_LCD	1.7		3.6		
VDD_AGPIO	1.7		3.6	V	
VDD_BGPIO	2.52	3.3	3.6	V	
VDD_CGPIO	1.7		3.6	V	
VDD_DGPIO	1.7		3.6	V	
VDD_DRAM	1.35	1.5	1.65	V	For AIT8328G and AIT8328Q
VDD_DRAM	1.7	1.8	1.9	V	For AIT8328P LPDDR
VDD_DDR	1.35	1.5	1.65	V	For AIT8328Q DDR3
VDD_DRAM_CORE	0.99	1.1	1.21	V	For AIT8328G and AIT8328Q
VDD_DRAM_CORE_T/B	0.99	1.1	1.21	V	For AIT8328P
VDD_VREFDQ/VREFCA	0.675	0.75	0.825	V	For AIT8328G. Equal VDD_DRAM*0.5
VDD_USB_1V1	1.0	1.1	1.2	V	Output by internal LDO
VDD_USB_3V3	2.97	3.3	3.63	V	

Symbols	Min.	Typ.	Max.	Unit	Note
AVDD_PLL	0.99	1.1	1.21	V	
AVDD_MIPI_RX0	0.99	1.1	1.21	V	
AVDD_MIPI_RX1	0.99	1.1	1.21	V	
AVDD_AUDIO	2.52	2.8	3.3	V	
AVDD_TV	2.52	2.8	3.3	V	
VDD11_TMDS	0.99	1.1	1.21	V	
VDD33_TMDS	2.97	3.3	3.63	V	
VDD33_HDMI	2.97	3.3	3.63	V	
VDD_RTC	2	3.3	3.63	V	
VDD_POR_1V8	1.62	1.8	1.98	V	
VDD_SADC	2.52	2.8	3.08	V	

Table 3. Voltage domain

5.3 Host/Sensor serial Interface

		Standard-Mode		Fast-Mode		
Symbol	Parameter	Min	Max	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time for START	4.0	-	0.6	-	us
$t_{SU;STA}$	Set-up time for repeated START condition	4.7	-	0.6	-	us
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	High period of the SCL clock	4.0	-	0.6	-	us
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.9	us
$t_{SU;DAT}$	Data set-up time	250	-	100	-	ns
tr	Rise time of both SCL and SDA	-	500	-	300	ns
tf	Fall time of both SCL and SDA	-	300	-	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	us
t_{BUF}	Bus free time between STOP	4.7	-	1.3	-	us

	and START condition					
C_b	Capacitive load for each bus line	-	400	-	400	pF

Table 4. Host/sensor serial interface timing parameter

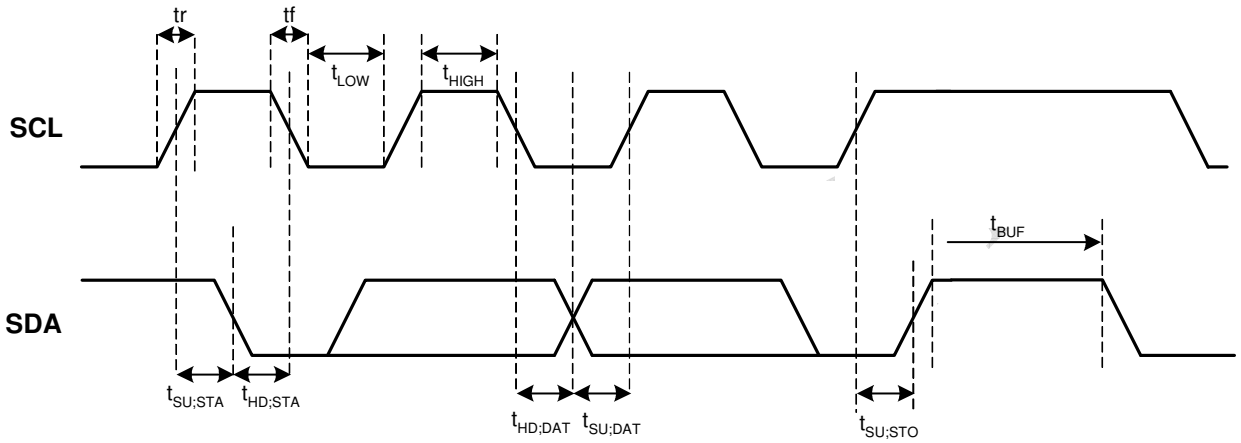


Figure 2. Host/sensor serial interface timing parameter

5.4 Parallel Sensor Interface

Symbol	Parameter	Min	Max	Unit
t_{CK}	Pixel clock cycle	7	-	ns
t_{CKH}	Pixel clock high level width	45%~55% duty cycle		ns
t_{CKL}	Pixel clock low level width			ns
t_{SS}	Sync signal output setup time	3	-	ns
t_{SH}	Sync signal output hold time	3	-	ns
t_{DS}	Data output setup time	3	-	ns
t_{DH}	Data output hold time	3	-	ns
t_{HS}	Hsync time	-	Frame width	cycle
t_{HHS}	Hsync start time	-	-	cycle
t_{BK}	Blanking time	64	-	cycle
t_{VSE}	Vsync end time	-	-	cycle

Table 5. Parallel sensor interface timing

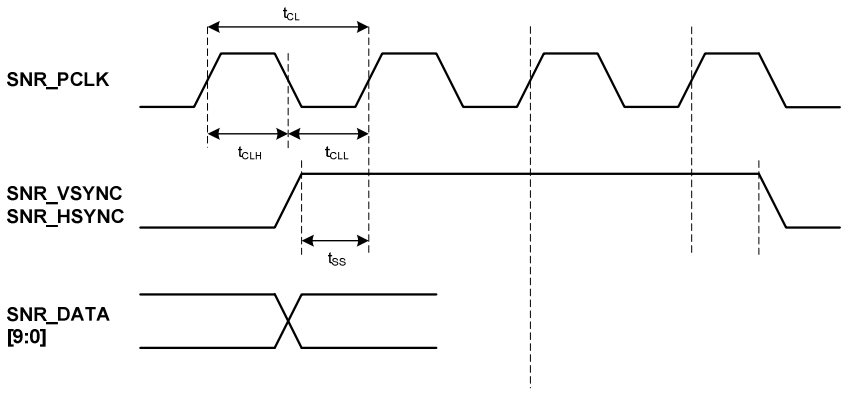


Figure 3. Parallel sensor interface timing

5.5 UART Interface

Symbol			Max	Unit
t_{rxsw}	Receive start bit pulse width	0.985T	1.015T	ns
t_{rxdw}	Receive data bit pulse width	0.985T	1.015T	ns
t_{rxpw}	Receive parity bit pulse width	0.985T	1.015T	ns
t_{rxspw}	Receive stop bit pulse width	0.985T	-	ns
f_{baud}	Programmable baud rate	0.496	8000	KHz
t_{txsw}	Transmit start bit pulse width		T	ns
t_{txdw}	Transmit data bit pulse width		T	ns
t_{txpw}	Transmit parity bit pulse width		T	ns
t_{txspw}	Transmit stop bit pulse width		-	ns

*T (baud period) = 1/programmed baud rate

Table 6. UART interface timing

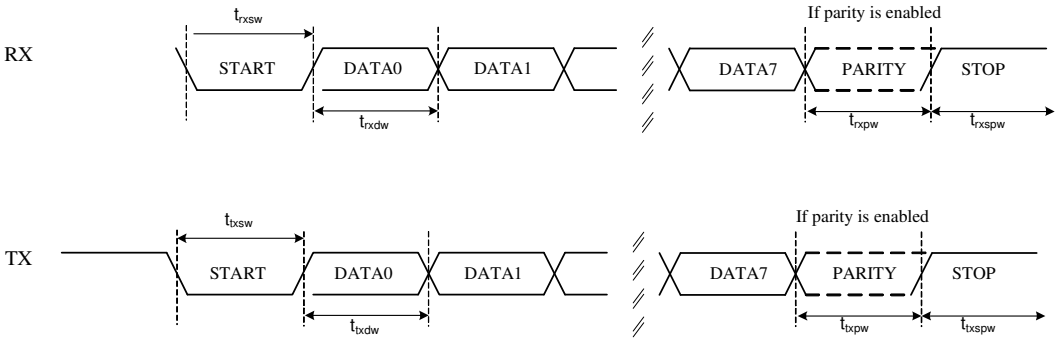
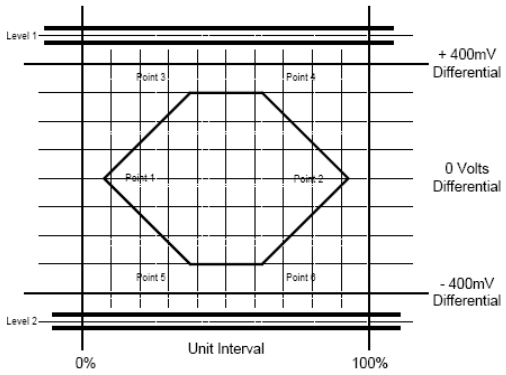


Figure 4. UART interface timing

5.6 USB2.0 High Speed Interface

Symbol	Parameter	Min	Max	Unit
High-speed Mode				
t_{HSR}	High-speed differential rise time (10% - 90%)	500	-	ps
t_{HSF}	High-speed differential fall time (10% - 90%)	500		ps
Full-speed Mode				
t_{FR}	Rise Time for DP/DM	4	20	ns
t_{FF}	Fall Time for DP/DM	4	20	ns
t_{FRFM}	Differential rise/fall Time Matching (t_{FR} / t_{FF})	90	110	%
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Table 7. USB Driver Characteristic

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
— Driver timing						
═ High-speed mode						
Driver waveform requirement	See the eye pattern of template 1 (described in the USB 2.0 spec.) 		Follow template 1 described in USB specification Rev 2.0. <table><tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr><tr><td>Level 1</td><td>525 mV in UI following a transition, 475 mV in all others</td><td>N/A</td></tr><tr><td>Level 2</td><td>-525 mV in UI following a transition, -475 in all others</td><td>N/A</td></tr><tr><td>Point 1</td><td>0 V</td><td>7.5% UI</td></tr><tr><td>Point 2</td><td>0 V</td><td>92.5% UI</td></tr><tr><td>Point 3</td><td>300 mV</td><td>37.5% UI</td></tr><tr><td>Point 4</td><td>300 mV</td><td>62.5% UI</td></tr><tr><td>Point 5</td><td>-300 mV</td><td>37.5% UI</td></tr><tr><td>Point 6</td><td>-300 mV</td><td>62.5% UI</td></tr></table>			
— Full-speed mode						
Propagation delay	For the detailed description of VI, FSE 0, and		-	-	15	ns

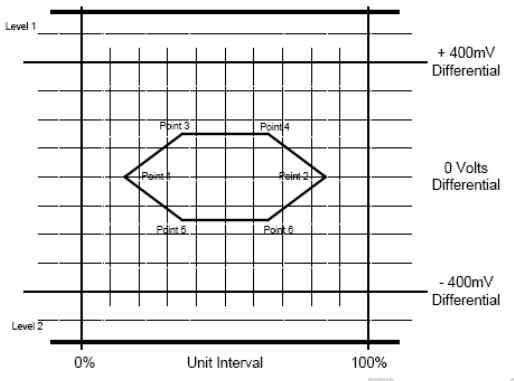
<table>
<tr><td>(VI, FSE 0, OE to DP, DM)</td><td>OE, (please refer to the USB 1.1 spec.)</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="7">═ Receiver timing</td></tr>
<tr><td colspan="7">═ High-speed mode (template 4, USB 2.0 spec.)</td></tr>
<tr><td>Data source jitter and receiver jitter tolerance</td><td colspan="2">See the eye pattern of template 4 (described in the USB 2.0 spec.)
 
</td><td colspan="4">Follow template 4 described in USB specification Rev 2.0.
<table>
<tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr>
<tr><td>Level 1</td><td>575 mV</td><td>N/A</td></tr>
<tr><td>Level 2</td><td>-575 mV</td><td>N/A</td></tr>
<tr><td>Point 1</td><td>0 V</td><td>15% UI</td></tr>
<tr><td>Point 2</td><td>0 V</td><td>85% UI</td></tr>
<tr><td>Point 3</td><td>150 mV</td><td>35% UI</td></tr>
<tr><td>Point 4</td><td>150 mV</td><td>65% UI</td></tr>
<tr><td>Point 5</td><td>-150 mV</td><td>35% UI</td></tr>
<tr><td>Point 6</td><td>-150 mV</td><td>65% UI</td></tr>
</table></td></tr>
<tr><td colspan="7">═ Full-speed mode</td></tr>
<tr><td>$t_{PLH(rcv)}$
$t_{PHL(rcv)}$</td><td>Receiver propagation delay (DP; DM to RX_RCV)</td><td>For the detailed description of RCV, (please refer to the USB 1.1 spec.)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
<tr><td>$t_{PLH(single)}$
$t_{PHL(single)}$</td><td>Receiver propagation delay (DP; DM to VOP, VON)</td><td>-</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
</table>

Table 8. USB Driver/Receiver Timing

5.7 Power On/Off Sequence

Symbol	Parameter	Min	Max	Unit
t_{PUD}	Core power up to IO power up delay	100	-	ns
t_{RUD}	IO power on to reset assert delay	1	-	ms
t_{POD}	IO power off to Core power off delay	100	-	ns
t_{ROD}	Reset de-assert to IO power delay	0	-	Ns
t_{CKRST}	Clock on to reset assert delay	8T	-	T=42ns(24MHz)

Table 9. Power on/off sequence parameter

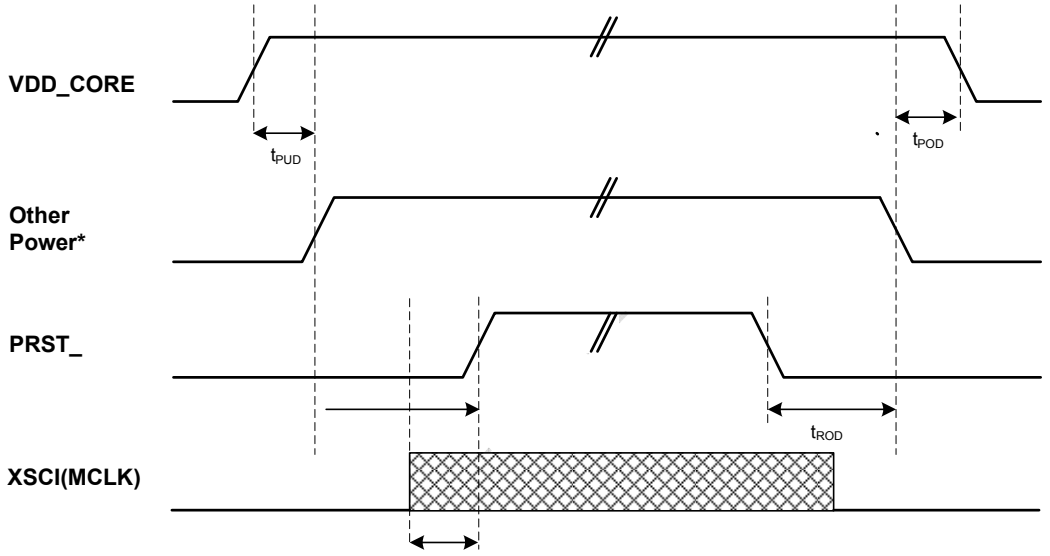
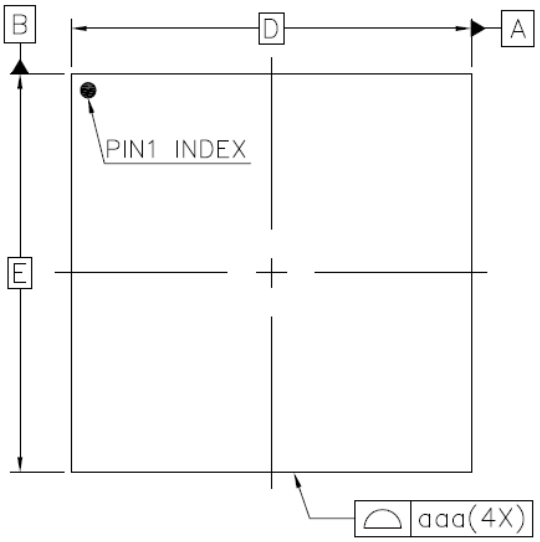


Figure 5. Power on/off timing diagram

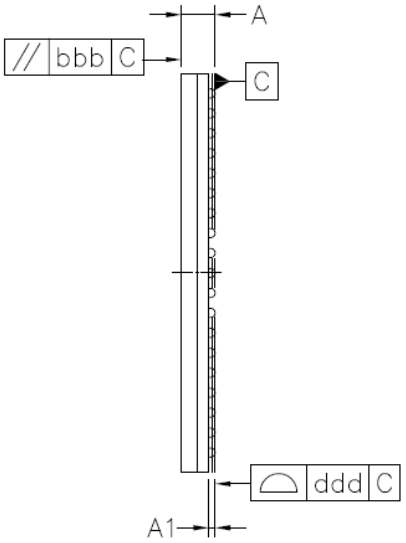
6 Package Information

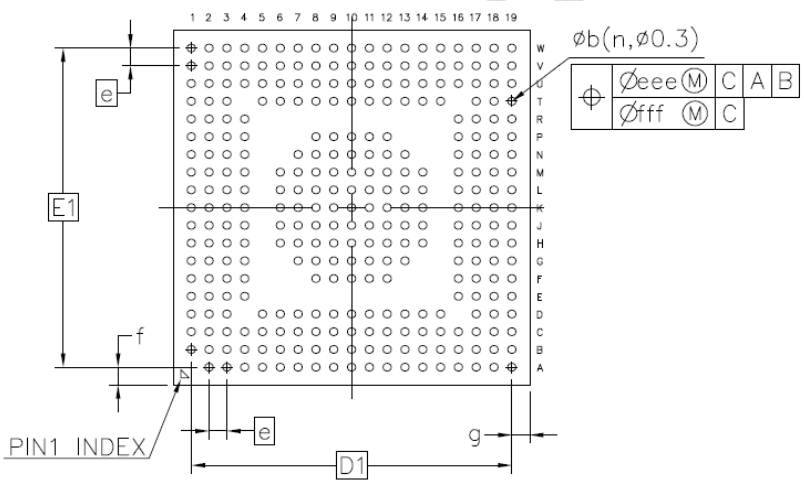
6.1 AIT8328G (BGA304)

Top View



Side View



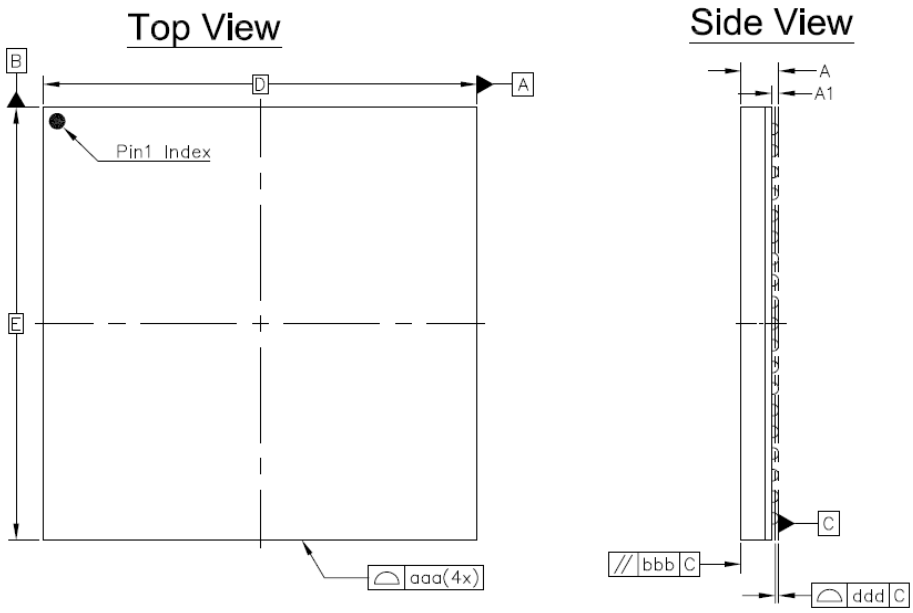


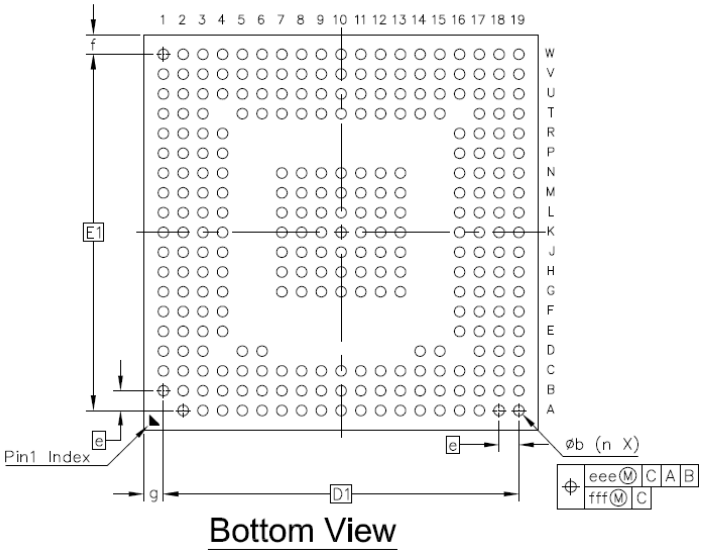
Bottom View

	Axis	Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Body Size:	X	D	12.90	13.00	13.10
	Y	E	12.90	13.00	13.10
Ball Pitch:		e		0.65	
Total Thickness:		A	---	---	1.20
Mold Thickness:			0.675	0.7	0.725
Substrate Thickness:			0.18	0.21	0.24
Ball Diameter:				0.30	
Stand Off:		A1	0.18	0.21	0.24
Ball Width:		b	0.25	0.30	0.35
Package Edge Tolerance:		aaa		0.10	
Mold Flatness:		bbb		0.10	
Coplanarity:		ddd		0.10	
Ball Offset (Package):		eee		0.15	
Ball Offset (Ball):		fff		0.08	
Ball Count:		n		277	
Edge Ball Center to Center:	X	D1		11.70	
	Y	E1		11.70	
Edge Ball Center to Package Edge:	X	g	0.55	0.65	0.75
	Y	f	0.55	0.65	0.75

DIMENSION		.XX	± 0.05
UNIT	mm	.X	± 0.1

6.2 AIT8328P (BGA277)





	Axis	Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Body Size:	X	D	12.90	13.00	13.10
	Y	E	12.90	13.00	13.10
Ball Pitch:		e		0.65	
Total Thickness:		A	---	---	1.20
Mold Thickness:			0.675	0.7	0.725
Substrate Thickness:			0.18	0.21	0.24
Ball Diameter:				0.30	
Stand Off:		A1	0.18	0.21	0.24
Ball Width:		b	0.25	0.30	0.35
Package Edge Tolerance:		aaa		0.10	
Mold Flatness:		bbb		0.10	
Coplanarity:		ddd		0.10	
Ball Offset (Package):		eee		0.15	
Ball Offset (Ball):		fff		0.08	
Ball Count:		n		277	
Edge Ball Center to Center:	X	D1		11.70	
	Y	E1		11.70	
Edge Ball Center to Package Edge:	X	g	0.55	0.65	0.75
	Y	f	0.55	0.65	0.75

DIMENSION		.XX	± 0.05
UNIT	mm	.X	± 0.1

6.3 AIT8328Q (BGA338)

TBD.