SSC333
High-Integrated IP Camera SoC Processor

Preliminary Product Brief Version 0.1

REVISION HISTORY

Revision No.	Description	Date
0.1	• Initial release	02/11/2020

FEATURES

- High Performance Processor Core
  - ARM Cortex-A7 Single Core
  - Neon and FPU
  - Memory Management Unit for Linux support
  - DMA Engine
- Image/Video Processor
  - Supports 10-bit parallel interface for raw data input
  - Supports MIPI interface with two data lanes and one clock lane
  - Supports 8/10-bit CCIR656 interface
  - Supports 3M (2304x1296 or 2048x1536) pixels video recording and image snapshot
  - Bad pixel compensation
  - Noise Reduction (NR)
  - Optical black correction
  - Lens shading compensation
  - Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
  - CFA color interpolation
  - Color correction
  - Gamma correction
  - Wide Dynamic Range (WDR)
  - Rotation with 90 or 270 degrees
  - Fully programmable multi-function scaling engines
- H.265/HEVC Encoder
  - Supports H.265/HEVC main profile encoding
  - Supports MVs 32x32, 16x16, and 8x8
  - Supports up to quarter-pixel
  - Supports frame level and MB level rate control
  - Supports ROI (Intra map or ZMV map)
  - Supports max. 3M + D1 @ 20fps encoding
- H.264 Encoder
  - Supports H.264 baseline and main profile encoding
  - Supports MVs 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, and 4x4
  - Supports up to quarter-pixel
  - Supports frame level and MB level rate control
  - Supports ROI (Intra map or ZMV map)
  - Supports max. 3M + D1 @ 20fps encoding
- JPEG Encoder
  - Supports JPEG baseline encoding
  - Supports YUV422 or YUV420 format
  - Supports max. 3Mp/20fps encoding
  - Supports real-time mode and frame encode mode
- Video Encoding Performance
  - Supports 3Mp20 + D1p20 H.265/HEVC or H.264 encoding
  - Supports MJPEG up to 3Mp20 encoding
- Audio Processor
  - One stereo ADC for microphone inputs
  - One DAC for lineout
  - Supports 8K/16K/32KHz sampling rate audio recording
  - Digital and analog gain adjustment
- SPI NOR/NAND Flash Interface
  - Compliant with standard, dual and quad SPI flash memory components
- SD Card Interface
  - Compatible with SD spec. 2.0, data bus 1/4-bit mode
  - Compatible with SDIO spec. 2.0, data bus 1/4-bit mode
- SDIO 2.0 Interface
  - Compatible with SDIO spec. 2.0, data bus 1/4-bit mode
  - Compatible with SD spec. 2.0, data bus 1/4-bit mode

- USB 2.0 Interface
  - One USB 2.0 configurable host or device
    - Host mode supports EHCI specifications
    - Device mode supports 3 endpoints
- DRAM Memory
  - Embedded 512Mb DDR2
- Connectivity
  - One USB 2.0 Host Controller could be used for USB Wi-Fi dongle or module
  - One SDIO 2.0 Host Controller could be used for SDIO Wi-Fi module
- Security Engines
  - Supports AES128/AES192/AES256/ DES/3DES/RSA/SHA-I/SHA-256
  - Supports secure booting
- Boot Options
  - SPI NOR
  - SPI NAND
  - SD Card
- Peripherals
  - Dedicated GPIOs for system control
  - Supports 11 PWM outputs (shared with GPIOs)
  - Two generic UARTs and one fast UART with flow control
  - Three generic timers and one watchdog timer
  - Two SPI masters
  - Two I2C Masters
  - Built-in 10-bit SAR ADC with 4-channel analog inputs for different kinds of application
  - Supports internal temperature sensor
  - Supports ISP sensor clock 12MHz, 24MHz, 37.125MHz
- Operating Voltage Range
  - Core: 0.9V
  - I/O: 1.8 ~ 3.3V
  - DRAM: 1.8V
  - Power Consumption: TBD
- Package
  - 88-pin QFN, 9mm x 9mm

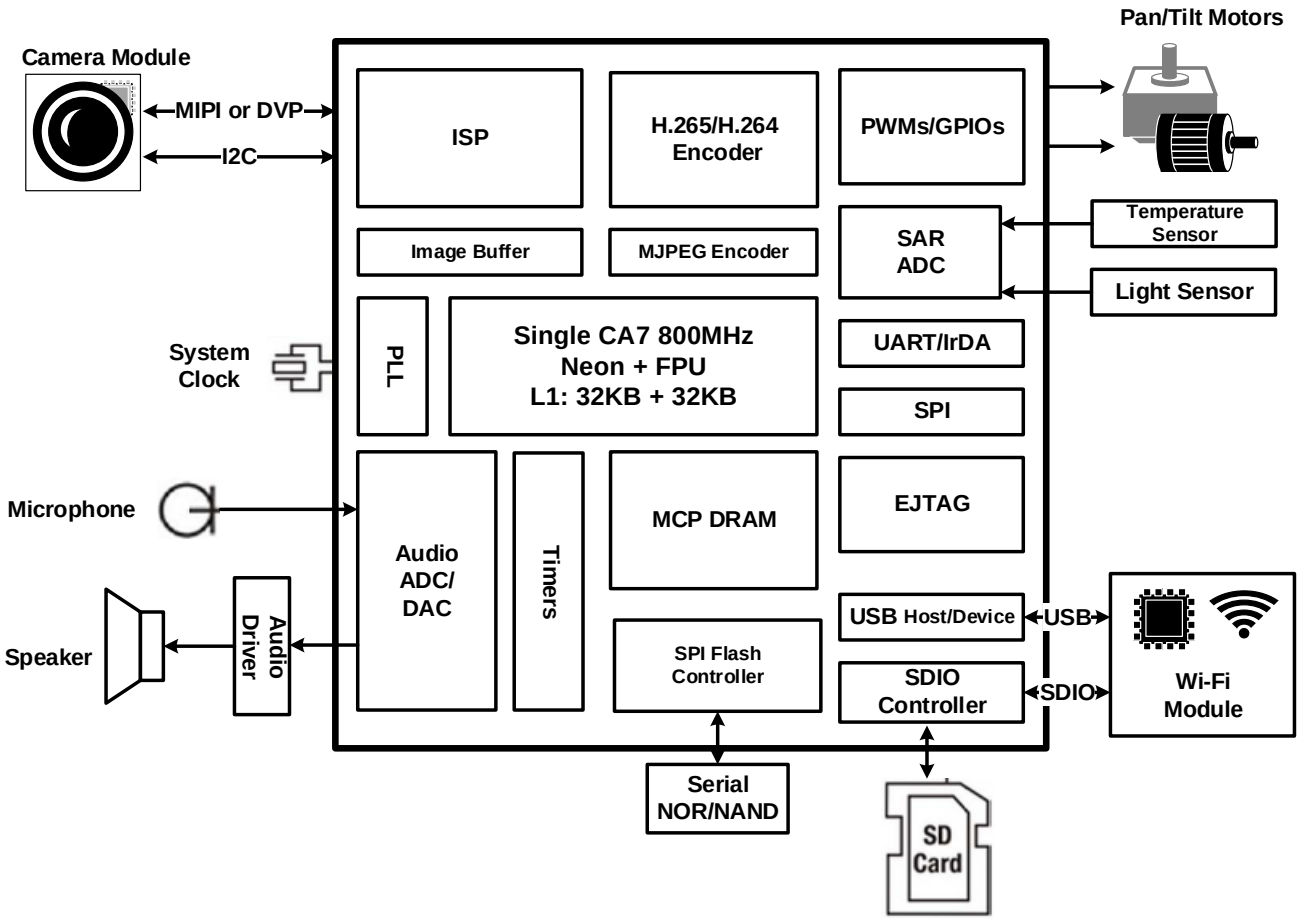
GENERAL DESCRIPTIONS

The SSC333 is a highly integrated SoC. Based on ARM Cortex-A7, the application processor integrates Image Signal Processor (ISP), Video (H.264/H.265/MJPEG) Encoders and other useful peripherals for IP camera applications.

A typical utilization of the SSC333 application processor is demonstrated in the following block diagram. The complete system includes a camera module (CMOS sensor), a connectivity module (Wi-Fi), and a non-volatile storage (SPI NOR/NAND flash or SD card). The ISP handles images captured from the camera sensor, and the video stream is composed of a large amount of images. There are pre- and post- video processing stages. The pre-video processing rotates images, reduces noises, enhances signals and translates color domains. The post-video processing adjusts color quality, and generates multiple video streams with different resolutions. Multimedia Encoders can compress those video streams with different compressing standards at the same time. The well compressed video/audio streams could be streamed or stored in the cloud server through Wi-Fi or stored in a local SD card. The SPI NOR/NAND flash is usually reserved for operating system and application software. Moreover, other peripherals such as SAR ADC, Audio ADC/DAC, UARTs, PWMs, GPIOs and SPI are supported to realize applications with maximal flexibility.

The SSC333 supports secure booting and personalization authentication mechanism for system security. The AES/DES/3DES cipher engines could further help encrypt the compressed video/audio streams to enhance privacy.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Video Encoder

I. JPE Feature Description

- Supports JPEG encoding 3Mp20
  - Frame mode
  - IMI row mode
- Supports YUYV input format
- Supports NV12 input format
- Supports DCT mode to accelerate SW encoding

II. H.264/H.265 Feature Description

H.264/H.265 engine (abbr. as VEN) is a hardware encoder for H.264/H.265 baseline/main profile. It encodes image data from frame buffer (DRAM) in YUV420 format and generates bit-streams to memory. Maximum resolution of 3M (2304x1296 or 2048x1536) + D1 with 20fps is supported.

In IP-CAM application, the bitrate is very important due to limited storage space in long time recording. Consequently, VEN implements bitrate control mechanism in frame level or macro-block (MB) level. Both variable bitrate (VBR) and constant bitrate (CBR) are supported. In general, VBR encoding will produce better image quality than CBR.

To save memory bandwidth, VEN provides data compression/decompression option when accessing DRAM. Besides, internal SRAM is used as a cache architecture to reduce DRAM read/write operations. It is very helpful in complex system application where image rotation, and/or fisheye correction are enabled simultaneously.

Another feature called Region of Interest (ROI) Encoding is supported to provide the highest image quality on the areas or scene or objects of most interest while reducing the quality level in uninteresting areas to provide the highest quality/lowest bandwidth results.

ISP

I. Brief Feature Description

The ISP design is used to transfer raw sensor data output to YUV data. It also supports YUV sensor at ISP bypass mode default.

- Supports up to 3M (2304X1296 or 2048X1536) @20Hz
- WDR
- Bad pixel compensation
- Green equal
- Supports rgbir2x2 or rgbir4x4 mode input
- Optical black correction
- Lens shading compensation
- Asymmetric lens shading compensation
- Statistic for AWB/AE/AF
- Supports de-noise 3DNR/2DNR
- Supports rotation
- White Balance PreGain and PostGain can be enabled at the same time
- CFA color interpolation
- Gamma correction
- Edge enhancement
- Supports menuload for ALSC_gain/DefectPxl/Gamma table

Peripheral

I. USB Brief Feature Description

One port of host/OTG controller is fully compliant with the USB 2.0 specification and the Enhanced Host Controller Interface (EHCI) specification. This Host/OTG Controller can support FS/LS transactions, Interrupt/Control/Bulk transfers and split/preamble transactions for hub.

II. MIPI CSI Interface

The features are listed below:

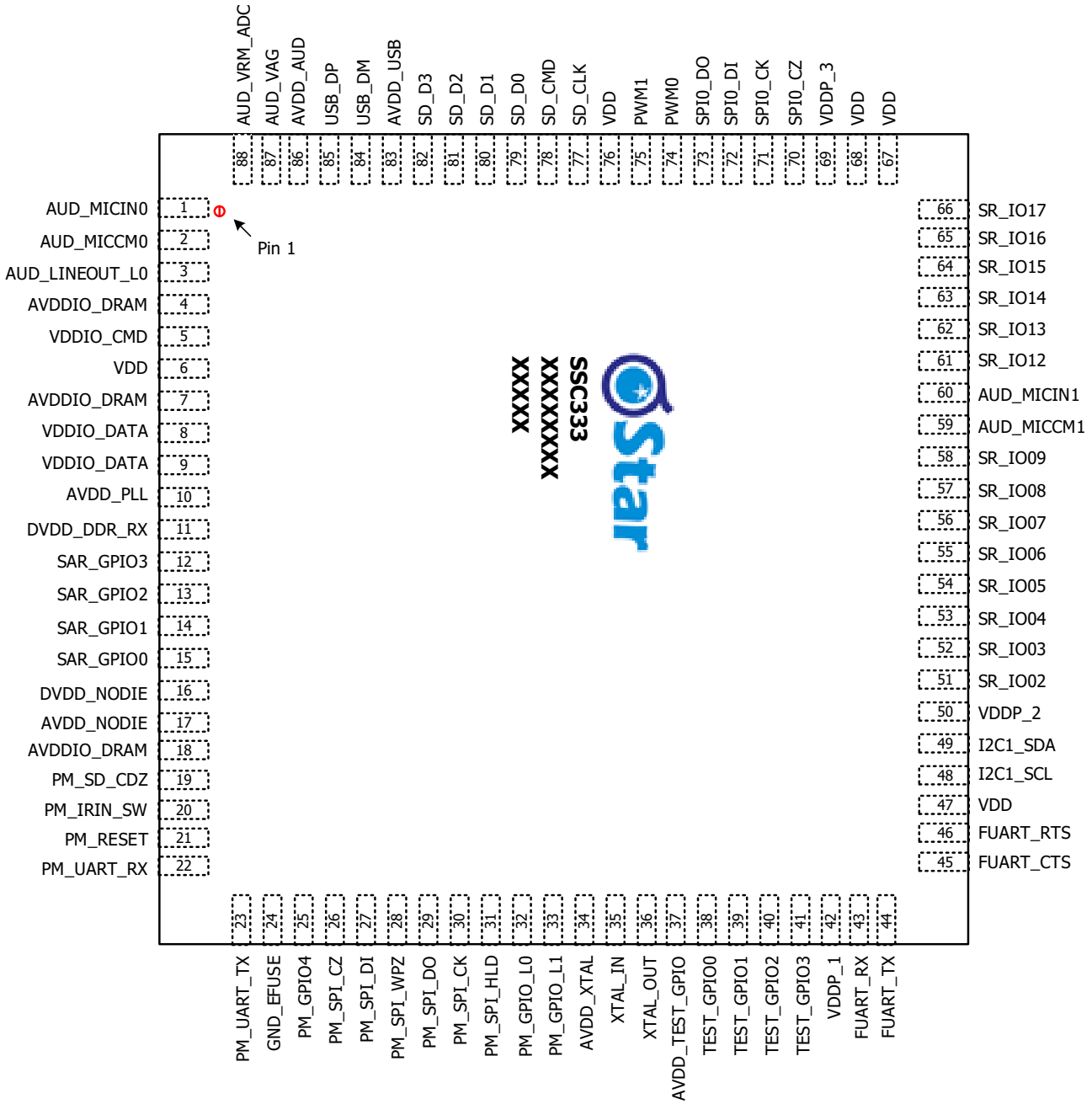
- CSI-2 1.1/D-PHY 1.1 compliant receiver with maximum Input Frequency 1.5GHz
- Supports 1 clock lane, 2 data lanes
- Supports YUV422 8-bit, Raw8, Raw10, Raw12, Generic 8-bit long packet and User defined byte-based data type
- Supports 1-bit error correction/2-bit error detection for packet header
- Supports checksum error detection for payload data
- Supports timing generation for Vsync and Hsync

III. Encryption Brief Feature Description

AESDMA is a secure IP for Secure Boot and HDMI Key Authentication. There are three engines inside this IP:

- AES: ECB, CBC (dvs042), ECB_CTS, CBC_CTS, CTR
- SHA: SHA_1, SHA_256
- RSA: RSA_2048 in HW key mode, programmable size in SW key mode

PIN DIAGRAM



SIGNAL DESCRIPTION

Signal Name	Signal Type	Function	QFN88 (9 x 9) Pin Location
System Reset Interface			
PM_RESET	I	System Reset (Active High)	21
Debug UART Interface			
PM_UART_RX	I	Debug UART Receive Data Input with Pull Up Resistor / Slave I2C Serial Clock	22
PM_UART_TX	O	Debug UART Transmit Data Output with Pull Up Resistor / Slave I2C Serial Data	23
System Interface			
XTAL_IN	I	24MHz Crystal Input	35
XTAL_OUT	O	24MHz Crystal Output	36
SPI Flash Interface			
PM_SPI_CZ	O	SPI Flash Chip Select (Active Low)	26
PM_SPI_DI	O	SPI Flash Serial Data To Device (MOSI)	27
PM_SPI_WPZ	O	SPI Flash Write Protect	28
PM_SPI_DO	I	SPI Flash Serial Data From Device (MISO)	29
PM_SPI_CK	O	SPI Flash Clock	30
PM_SPI_HLD	O	SPI Flash Hold	31
Test GPIO			
TEST_GPIO0	I/O	General Purpose Input/Output	38
TEST_GPIO1	I/O	General Purpose Input/Output	39
TEST_GPIO2	I/O	General Purpose Input/Output	40
TEST_GPIO3	I/O	General Purpose Input/Output	41
PM GPIO Interface			
PM_GPIO4	I/O	Power Manage Group General Purpose Input/Output	25
PM_IRIN_SW	I	General Purpose Input/Output Software Mode Infrared Input from IR Receiver	20
PM_GPIO_L0	I/O	General Purpose Input/Output	32
PM_GPIO_L1	I/O	General Purpose Input/Output	33
SAR ADC Interface			
SAR_GPIO0	I	General Purpose Input/Output or Muxed to SARADC Input Channel 0	15

Signal Name	Signal Type	Function	QFN88 (9 x 9) Pin Location
SAR_GPIO1	I	General Purpose Input/Output or Muxed to SARADC Input Channel 1	14
SAR_GPIO2	I	General Purpose Input/Output or Muxed to SARADC Input Channel 2	13
SAR_GPIO3	I	General Purpose Input/Output or Muxed to SARADC Input Channel 3	12
Master I2C Interface			
I2C1_SCL	O	I2C 1 Master Mode I2C Clock (for Sensor)	48
I2C1_SDA	I	I2C 1 Master Mode I2C Data (for Sensor)	49
Master SPI Interface			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	70
SPI0_CK	O	Master SPI 0 Serial Clock	71
SPI0_DI	O	Master SPI 0 Serial Data To Device (MOSI)	72
SPI0_DO	I	Master SPI 0 Serial Data From Device (MISO)	73
Fast UART Interface			
FUART_RX	I	Fast UART Receive Data Input	43
FUART_TX	O	Fast UART Transmit Data Output	44
FUART_CTS	I	Fast UART Clear to Send	45
FUART_RTS	O	Fast UART Request to Send	46
PWM Interface			
PWM0	O	PWM 0 Output	74
PWM1	O	PWM 1 Output	75
Image Sensor Interface			
SR_IO02	I/O	Sensor General Purpose Input/Output 2	51
SR_IO03	I/O	Sensor General Purpose Input/Output 3	52
SR_IO04	I/O	Sensor General Purpose Input/Output 4	53
SR_IO05	I/O	Sensor General Purpose Input/Output 5	54
SR_IO06	I/O	Sensor General Purpose Input/Output 6	55
SR_IO07	I/O	Sensor General Purpose Input/Output 7	56
SR_IO08	I/O	Sensor General Purpose Input/Output 8	57
SR_IO09	I/O	Sensor General Purpose Input/Output 9	58
SR_IO12	I/O	Sensor General Purpose Input/Output 12	61
SR_IO13	I/O	Sensor General Purpose Input/Output 13	62
SR_IO14	I/O	Sensor General Purpose Input/Output 14	63

Signal Name	Signal Type	Function	QFN88 (9 x 9) Pin Location
SR_IO15	I/O	Sensor General Purpose Input/Output 15	64
SR_IO16	I/O	Sensor General Purpose Input/Output 16	65
SR_IO17	I/O	Sensor General Purpose Input/Output 17	66
SD 2.0 Card Interface			
SD_CLK	O	SD 2.0 Clock	77
SD_CMD	O	SD 2.0 Command	78
SD_D0	I/O	SD 2.0 Data Bus 0	79
SD_D1	I/O	SD 2.0 Data Bus 1	80
SD_D2	I/O	SD 2.0 Data Bus 2	81
SD_D3	I/O	SD 2.0 Data Bus 3	82
PM_SD_CDZ	I	Power Manage SD 2.0 Card Detect	19
Line Out Interface			
AUD_LINEOUT_L0	O	Audio Left Channel Line Output	3
AUD_VAG	O	Audio Reference Voltage from 1/2 AVDD_AUD	87
AUD_VRM_ADC	I	Audio Reference Voltage for ADC	88
Analog Microphone Interface			
AUD_MICIN0	I	Audio Left Channel Microphone Positive Input	1
AUD_MICCM0	I	Audio Left Channel Microphone Negative Input	2
AUD_MICIN1	I	Audio Right Channel Microphone Positive Input	60
AUD_MICCM1	I	Audio Right Channel Microphone Negative Input	59
USB 2.0 Interface			
USB_DM	I/O	USB 2.0 Differential Pair, Negative	84
USB_DP	I/O	USB 2.0 Differential Pair, Positive	85

Signal Name	Signal Type	Function	QFN88 (9 x 9) Pin Location
Power Pins			
VDD	Core Power	Digital Core Power	6, 47, 67, 68, 76
VDDP_1	3.3V Power	Digital Power for VDDP_1 Group	42
VDDP_2	1.8/3.3V Power	Digital Power for VDDP_2 Group (Sensor IO Power)	50
VDDP_3	3.3V Power	Digital Power for VDDP_3 Group	69
DVDD_DDR_RX	Core Power	Digital Power for DDR RX	11
VDDIO_DATA	DDR Power	Analog Power for DDR MCLK/DATA	8, 9
VDDIO_CMD	DDR Power	Analog Power for DDR CMD	5
AVDDIO_DRAM	DDR Power	Stack DRAM Power	4, 7, 18
AVDD_NODIE	3.3V Power	Analog Power for PM	17
DVDD_NODIE	O	PM LDO Output (Cap to GND)	16
AVDD_PLL	3.3V Power	Analog Power for PLL	10
AVDD_XTAL	3.3V Power	Analog Power for XTAL	34
AVDD_USB	3.3V Power	Analog Power for USB	83
AVDD_TEST_GPIO	3.3V Power	Power for Test GPIO	37
AVDD_AUD	3.3V Power	Analog Power for Audio	86
GND_EFUSE	I	Power Source if eFuse is Burnt (Connected to Ground)	24
GND	GND	Digital Ground	ePad

PIN CHARACTERISTICS

QFN88 (9 x 9) Pin Location	Ball/Pin Name	Default Value after Reset	5V-tolerance	Driving Control
19	PM_SD_CDZ	Input, pull-up	Yes	
20	PM_IRIN	Input, pull-up	Yes	
25	PM_GPIO4	Input, pull-up	Yes	
26	PM_SPI_CZ	Output	Yes	Yes
27	PM_SPI_DI	Output	Yes	Yes
28	PM_SPI_WPZ	Output	Yes	Yes
29	PM_SPI_DO	Input, pull-up	Yes	Yes
30	PM_SPI_CK	Output	Yes	Yes
31	PM_SPI_HLD	Output	Yes	Yes
32	PM_GPIO_L0	Input, pull-down	Yes	Yes
33	PM_GPIO_L1	Input, pull-down	Yes	Yes
12	SAR_GPIO3	N/A	Yes	
13	SAR_GPIO2	N/A	Yes	
14	SAR_GPIO1	N/A	Yes	
15	SAR_GPIO0	N/A	Yes	
38	TEST_GPIO0	N/A	No	
39	TEST_GPIO1	N/A	No	
40	TEST_GPIO2	N/A	No	
41	TEST_GPIO3	N/A	No	
43	FUART_RX	Input, pull-up	Yes	
44	FUART_TX	Input, pull-up	Yes	
45	FUART_CTS	Input, pull-up	Yes	
46	FUART_RTS	Input, pull-up	Yes	
48	I2C1_SCL	Input, pull-up	Yes	Yes
49	I2C1_SDA	Input, pull-up	Yes	Yes
51	SR_IO02	Input, pull-up	No	Yes
52	SR_IO03	Input, pull-up	No	Yes
53	SR_IO04	Input, pull-up	No	Yes
54	SR_IO05	Input, pull-up	No	Yes
55	SR_IO06	Input, pull-up	No	Yes
56	SR_IO07	Input, pull-up	No	Yes
57	SR_IO08	Input, pull-up	No	Yes

QFN88 (9 x 9) Pin Location	Ball/Pin Name	Default Value after Reset	5V-tolerance	Driving Control
58	SR_IO09	Input, pull-up	No	Yes
61	SR_IO12	Input, pull-down	No	Yes
62	SR_IO13	Input, pull-down	No	Yes
63	SR_IO14	Input, pull-up	No	Yes
64	SR_IO15	Input, pull-up	No	Yes
65	SR_IO16	Input, pull-up	No	Yes
66	SR_IO17	Input, pull-up	No	Yes
70	SPI0_CZ	Input, pull-up	No	Yes
71	SPI0_CK	Input, pull-down	No	Yes
72	SPI0_DI	Input, pull-down	No	Yes
73	SPI0_DO	Input, pull-down	No	Yes
74	PWM0	Input, pull-down	Yes	Yes
75	PWM1	Input, pull-down	Yes	Yes
77	SD_CLK	Input, pull-down	Yes	Yes
78	SD_CMD	Input, pull-up	Yes	Yes
79	SD_D0	Input, pull-up	Yes	Yes
80	SD_D1	Input, pull-up	Yes	Yes
81	SD_D2	Input, pull-up	Yes	Yes
82	SD_D3	Input, pull-up	Yes	Yes
84	USB_DM	N/A	No	
85	USB_DP	N/A	No	

MULTI-FUNCTION TABLE

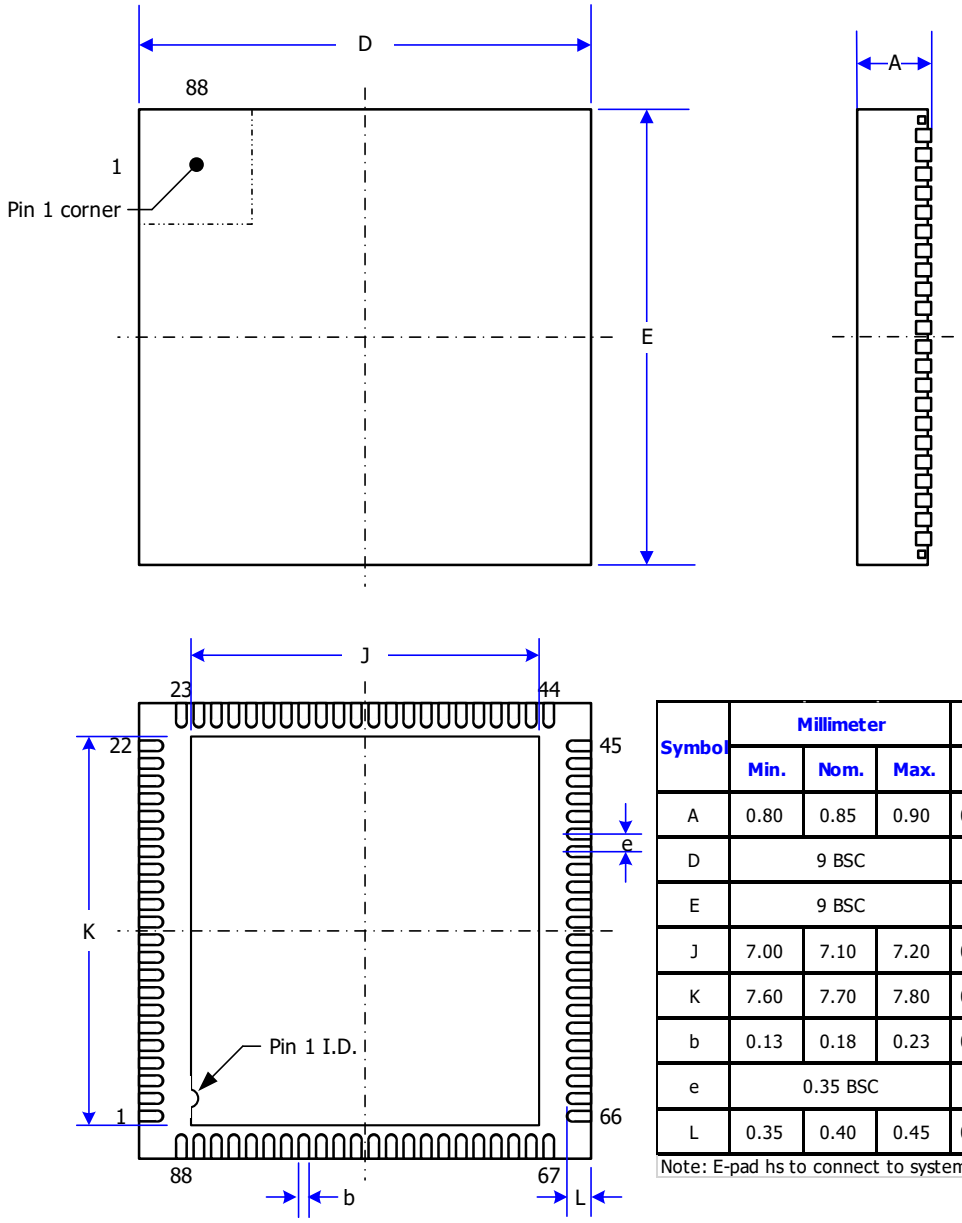
Signal Name	Signal Type	Function (QFN88)	QFN88 (9 x 9) Pin Location
Image Sensor (Parallel/BT656)			
SR_IO02	I	Parallel Input Data Bit 2 BT656 Input Data Bit 0	51
SR_IO03	I	Parallel Input Data Bit 3 BT656 Input Data Bit 1	52
SR_IO04	I	Parallel Input Data Bit 4 BT656 Input Data Bit 2	53
SR_IO05	I	Parallel Input Data Bit 5 BT656 Input Data Bit 3	54
SR_IO06	I	Parallel Input Data Bit 6 BT656 Input Data Bit 4	55
SR_IO07	I	Parallel Input Data Bit 7 BT656 Input Data Bit 5	56
SR_IO08	I	Parallel Input Data Bit 8 BT656 Input Data Bit 6	57
SR_IO09	I	Parallel Input Data Bit 9 BT656 Input Data Bit 7	58
SR_IO12	I	Parallel Input Data Bit 10 BT656 Input Data Bit 8	61
SR_IO13	I	Parallel Input Data Bit 11 BT656 Input Data Bit 9	62
Parallel/BT656 Control			
SR_IO14	I	Parallel HSYNC Input	63
SR_IO15	I	Parallel / BT656 Pixel Clock Input	64
SR_IO16	I	Parallel VSYNC Input	65
SR_IO17	O	SNR Master Clock Output	66
PWM0	O	SNR Power Down Control NOTE: 3.3V Level IO	74
PWM1	O	SNR Reset NOTE: 3.3V Level IO	75

Signal Name	Signal Type	Function (QFN88)	QFN88 (9 x 9) Pin Location
Image Sensor (2 lane MIPI_Mode2)			
SR_IO03	I	MIPI Data Input (Differential Pair 0, Negative)	52
SR_IO04	I	MIPI Data Input (Differential Pair 0, Positive)	53
SR_IO05	I	MIPI Clock Input (Differential Clock Pair, Negative)	54
SR_IO06	I	MIPI Clock Input (Differential Clock Pair, Positive)	55
SR_IO07	I	MIPI Data Input (Differential Pair 1, Negative)	56
SR_IO08	I	MIPI Data Input (Differential Pair 1, Positive)	57
MIPI Control			
SR_IO12	O	SNR Power Down Control	61
SR_IO13	O	SNR Reset	62
SR_IO17	O	SNR Master Clock Output	66
JTAG Mode1			
EJ_TCK	I	CA7 JTAG Clock	43
EJ_TMS	I	CA7 JTAG Mode Select	44
EJ_TDO	O	CA7 JTAG Data Out	45
EJ_TDI	I	CA7 JTAG Data In	46
JTAG Mode2			
EJ_TCK	I	CA7 JTAG Clock	70
EJ_TMS	I	CA7 JTAG Mode Select	71
EJ_TDO	O	CA7 JTAG Data Out	72
EJ_TDI	I	CA7 JTAG Data In	73
I2C 0 Mode2			
I2C0_SCL	O	Master I2C 0 Serial Clock	74
I2C0_SDA	I/O	Master I2C 0 Serial Data	75
I2C 1 Mode1			
I2C1_SCL	O	Master I2C 1 Serial Clock (for Sensor)	48
I2C1_SDA	I/O	Master I2C 1 Serial Data (for Sensor)	49
I2C 1 Mode2			
I2C1_SCL	O	Master I2C 1 Serial Clock	74
I2C1_SDA	I/O	Master I2C 1 Serial Data	75

Signal Name	Signal Type	Function (QFN88)	QFN88 (9 x 9) Pin Location
UART 0 Mode2			
UART0_RX	I	UART 0 Receiver	43
UART0_TX	O	UART 0 Transmitter	44
UART 1 Mode2			
UART1_RX	I	UART 1 Receiver	45
UART1_TX	O	UART 1 Transmitter	46
FUART Mode1			
FUART_RX	I	Fast UART Receiver	43
FUART_TX	O	Fast UART Transmitter	44
FUART_CTS	I	Fast UART Clear to Send	45
FUART_RTS	O	Fast UART Request to Send	46
FUART Mode5			
FUART_RX	I	Fast UART Receiver	43
FUART_TX	O	Fast UART Transmitter	44
SPI 0 Mode1			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	70
SPI0_CK	O	Master SPI 0 Serial Clock	71
SPI0_DI	O	Master SPI 0 Serial Data In (MOSI)	72
SPI0_DO	I	Master SPI 0 Serial Data Out (MISO)	73
SPI 0 Mode3			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	43
SPI0_CK	O	Master SPI 0 Serial Clock	44
SPI0_DI	O	Master SPI 0 Serial Data In (MOSI)	45
SPI0_DO	I	Master SPI 0 Serial Data Out (MISO)	46
SPI 1 Mode3			
SPI1_CZ	O	Master SPI 1 Chip Select (Active Low)	79
SPI1_CK	O	Master SPI 1 Serial Clock	80
SPI1_DI	O	Master SPI 1 Serial Data In (MOSI)	81
SPI1_DO	I	Master SPI 1 Serial Data Out (MISO)	82

Signal Name	Signal Type	Function (QFN88)	QFN88 (9 x 9) Pin Location
PWM Mode1			
PWM0	O	PWM 0 Output	74
PWM1	O	PWM 1 Output	75
PWM Mode2			
PWM2	O	PWM 2 Output	45
PWM3	O	PWM 3 Output	46
PWM4	O	PWM 4 Output	70
PWM5	O	PWM 5 Output	71
PWM6	O	PWM 6 Output	72
PWM7	O	PWM 7 Output	73
PWM9	O	PWM 9 Output	74
PWM10	O	PWM 10 Output	75
PWM Mode3			
PWM0	O	PWM 0 Output	43
PWM1	O	PWM 1 Output	44
PWM Mode4			
PWM8	O	PWM 8 Output	63
PWM9	O	PWM 9 Output	64
PWM10	O	PWM 10 Output	65
PM PWM Mode1			
PWM4	O	PWM 4 Output	32
PWM5	O	PWM 5 Output	33
PWM9	O	PWM 9 Output	32
PWM10	O	PWM 10 Output	33

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	0.90	0.031	0.033	0.035
D	9 BSC			0.354 BSC		
E	9 BSC			0.354 BSC		
J	7.00	7.10	7.20	0.276	0.280	0.283
K	7.60	7.70	7.80	0.299	0.303	0.307
b	0.13	0.18	0.23	0.005	0.007	0.009
e	0.35 BSC			0.014 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018

Note: E-pad hs to connect to system GND net.

ELECTRICAL SPECIFICATIONS

Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	V_{IH}	2.5			V
Input Voltage, Low	V_{IL}			0.8	V
Input Current, High	I_{IH}			-1.0	uA
Input Current, Low	I_{IL}			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	V_{OH}	VDDP-0.1[Note]			V
Output Voltage, Low	V_{OL}			0.1	V
SAR ADC Input		0		V_{VDD_33}	V
AUDIO OUTPUTS					
Line-Out			2.54		Vp-p
XTAL Specifications					
Input Voltage, High	V_{IH}	2.0		3.6	V
Input Voltage, Low	V_{IL}	-0.3		0.8	V
Clock frequency			24		MHz
Crystal accuracy			+/-30		ppm
Long-term jitter			+/-500		ps

Note: 1. VDDP can be V_{VDD_33}, V_{VDD_18}

2. 0.9Vrms @10Kohm load

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}	3.14	3.3	3.46	V
1.8V Supply Voltage (DDR II)	V_{VDD_18}	1.71	1.8	1.89	V
Core Power Supply Voltage (Core)	V_{VDD_core}	0.87	0.9	0.93	V
Ambient Operation Temperature	T_A	-20		70	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}	2.97	3.30	3.63	V
1.8V Supply Voltage (DDR II)	V_{VDD_18}			1.98	V
Core Power Supply Voltage (Core)	V_{VDD_core}			1.26	V
Storage Temperature	T_{STG}	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

HARDWARE POWER SEQUENCE PROCEDURE

The timing requirements of the hardware reset signal are shown as below:

Hardware Reset

HWRESET: Chip Reset; High Reset (Level)

The HWRESET pin is suggested to connect with 3.3V standby as shown in Figure 1. The VIH is 2V (Typ) +/- 10% (2.2V~1.8V); the VIL is 1.2V (Typ) +/- 10% (1.08V~1.32V). The power sequence is as shown in Figure 2.

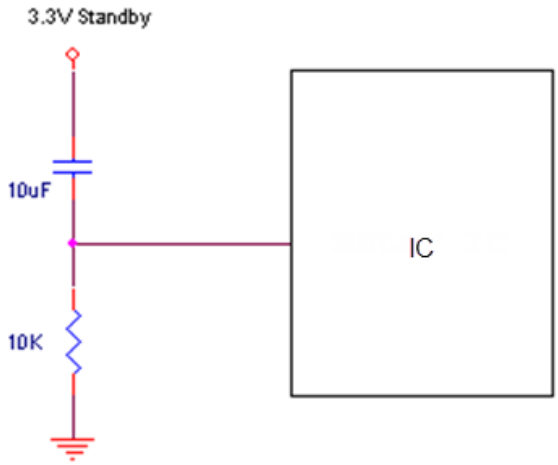
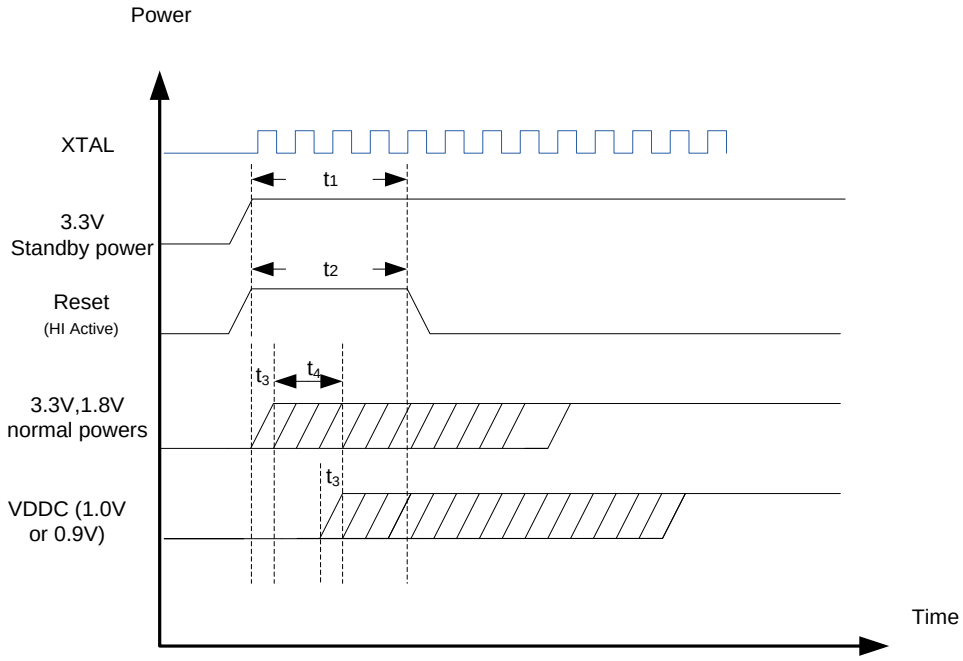


Figure 1: Reset Application Circuit

External Reset IC with External LDO

The timing is shown as Figure 2. The RST and power waveform must satisfy Figure 2 with parameters listed in Table 1.



Note:

***3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_TEST_GPIO)**

***1.0V/0.9V (VDD, DVDD_DDR_RX)**

***1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD)**

***1.8V (VDDP_2)**

***3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)**

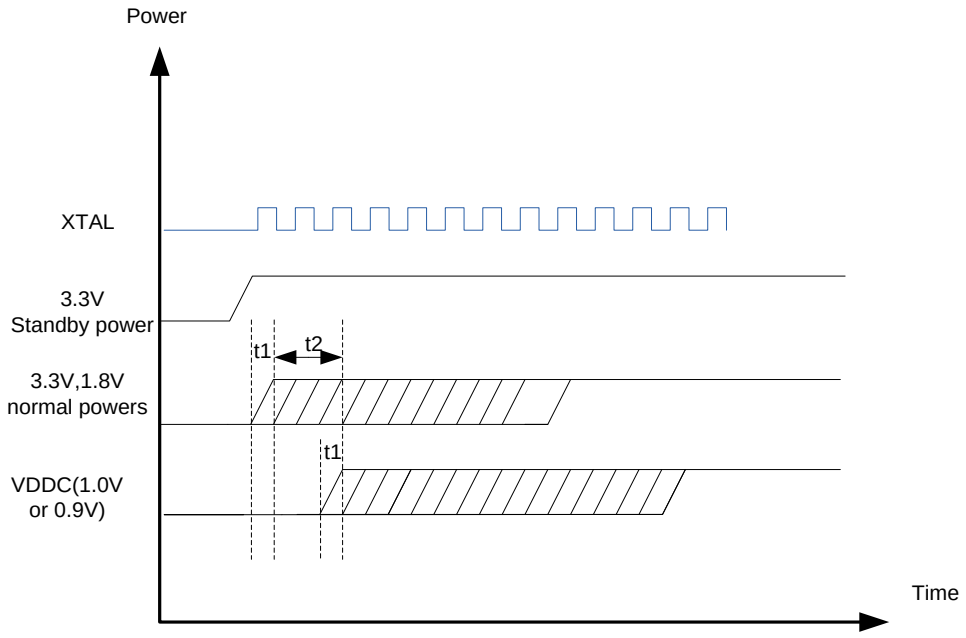
Figure 2: Power on Sequence

Table 1: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	XTAL stable to Reset falling	5	—	—	ms
t_2	Reset pulse width	5	—	—	ms
t_3	Normal 3.3V, 1.8V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t_4	Normal 3.3V and 1.8V to VDDC lead time	1	—	—	ms

Without External Reset IC with External LDO

The timing is shown as Figure 3. The power waveform must satisfy Figure 3 with parameters listed in Table 1.



Note:

***3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_TEST_GPIO)**

***1.0V/0.9V (VDD, DVDD_DDR_RX)**

***1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD)**

***1.8V (VDDP_2)**

***3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)**

Figure 3: Power on Sequence

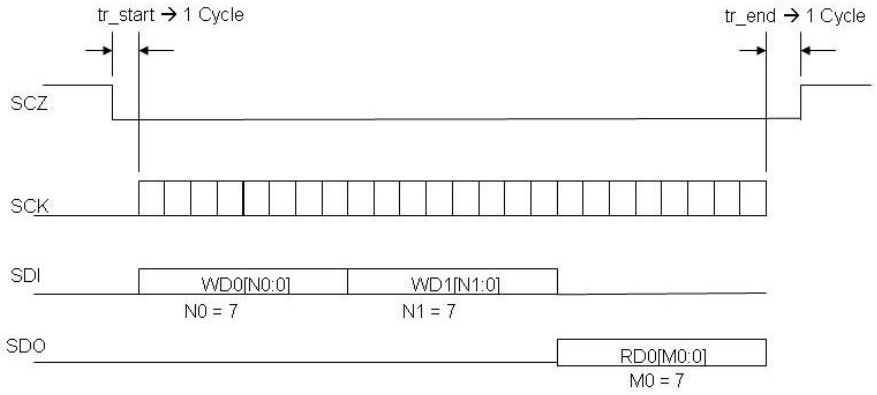
Table 2: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	Normal 3.3V, 1.8V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t_2	Normal 3.3V and 1.8V to VDDC lead time	1	—	—	ms

MSPI OPERATION EXAMPLE

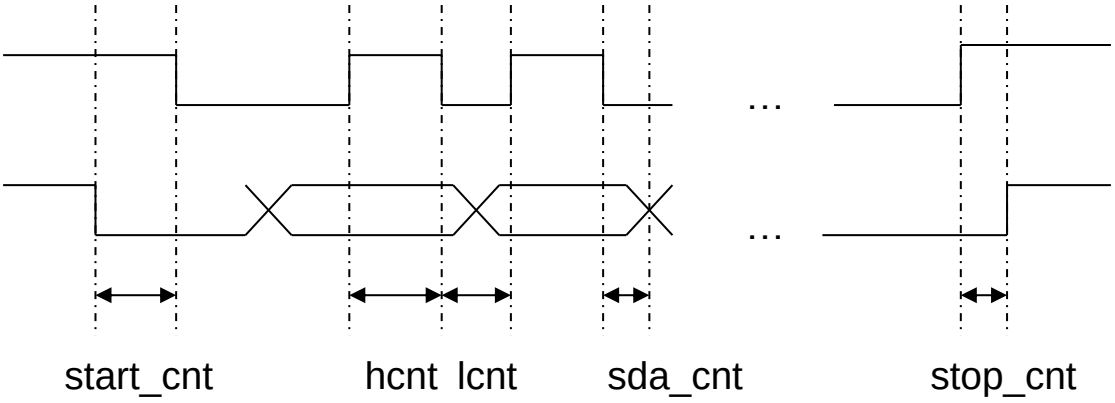
This section describes an example of MSPI operation.

(0). Initial
(1). CS goes low
(2). Write 2Bytes data
(3). Read 1Bytes data
(4). CS goes high



I2C clock frequency configurable is between 100Khz ~ 400Khz

Set MIIC Speed



clk_miic	12MHz	24MHz
lcnt (>1.3us)	>16T	>31T
hcnt (>0.6us)	>8T	>15T
start (>0.6us)	>8T	>15T
stop (>0.6us)	>8T	>15T
between start and stop (>1.3us)	>16T	>31T
data_latch (>0us)	>0T	>0T
sda change (<0.9us)	<11T	<22T

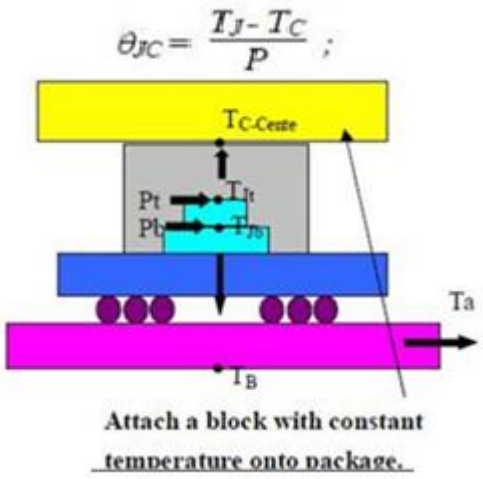
Register name	Address	Description
reg_stop_cnt	'h08[15:0]	Sets the SCL and SDA count for stop
reg_hcnt	'h09[15:0]	Sets the SCL clock high-period count
reg_lcnt	'h0a[15:0]	Sets the SCL clock low-period count
reg_sda_cnt	'h0b[15:0]	Sets the clock count between falling edge SCL and SDA
reg_start_cnt	'h0c[15:0]	Sets the SCL and SDA count for start
reg_data_lat_cnt	'h0d[15:0]	Sets the data latch timing

THERMAL RESISTANCE (°C/W)

Thermal simulation mode

PCB condition: JEDEC JESD51-5
PCB layers: 4 (2S2P)
PCB dimensions: 76.2 x 114.3 (mm x mm)
PCB thickness: 1.6 (mm)

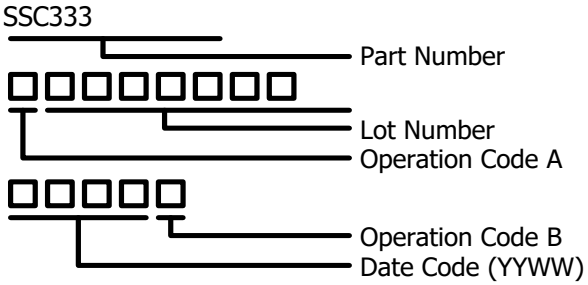
Part Number	Manufacture/ Vendor	Package		Thermal Resistance (°C/W)		
			PCB Layer	θ_{JA}	θ_{JC}	θ_{JB}
SSC333		QFN88_9x9	4L PCB	20.0	7.5	3.94



ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
SSC333	-20°C to +70°C	QFN	88-pin

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. SSC333 comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.