

# **MStar MSW8535N**

## **GSM/GPRS/EGPRS Baseband Processor**

### **Preliminary Product Brief**

#### **Version 0.1**

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## 1. INTRODUCTION

### 1.1. Scope

This document presents the general architecture and feature overview of the MSW8535N baseband product. More detailed or specific information is available on request.

### 1.2. Glossary

The following acronyms are used in this document:

DBB	Digital Baseband
ABB	Analog Baseband
MMP	Multimedia Processor
DigRF	Digital RF standard
EMI	External Memory Interface
EBI	External Bus Interface
IMI	Internal Memory Interface
FIR	Finite Impulse Response
MMC/SD	Multimedia Card / Secure Digital
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit Interface
UART	Universal Asynchronous Receiver Transmitter
RTOS	Real Time Operating System
MMI	Man Machine Interface
Mb	Mega bit
MB	Mega byte
Kb	Kilo bit
KB	Kilo byte
RTK	Real Time Kernel
HAL	Hardware Abstraction Layer
RFDL	RF Downloader Interface
HWL	Hardware Layer (modem related)
HCLK	ARM AMBA AHB clock
AGC	Automatic Gain Control
TXPR	Transmit Power
TDMA	Time Division Multiple Access

## 2. OVERVIEW

MSW8535N is a single-chip solution for GSM/GPRS/EGPRS baseband processor with rich multimedia features. Equipped with the ARM926EJ-STM 32-bit RISC CPU, the MSW8535N based platform offers a complete and flexible reference design to address a wide range of mobile handset market applications.

MSW8535N combines the functions of the GSM/GPRS/EGPRS digital baseband processor (DBB), the analog baseband (ABB), the power management unit (PMU), and the mobile multimedia processor (MMP) into one 13.5x13.5 mm package.

### 2.1. GSM/GPRS/EGPRS Modem

MSW8535N features a modem that supports quad-band GSM voice and circuit switched data service and GPRS/EGPRS packet switched service. With class 10 EGPRS, the baseband modem is capable of delivering data rate up to 240Kbps for the downlink (DL).

The RF interface can be configured to use either the standard analog I/Q data interface or the 2.5G DigRFTM interface. The flexible interface design allows the baseband to support a variety of GSM/GPRS/EGPRS RF transceiver solutions in the market. MSW8535N also provides two auxiliary DACs – APC DAC for transmit power ramping control and AFC DAC for the control of the reference clock frequency.

### 2.2. Power Management

The MSW8535N power management unit integrates on-chip voltage regulators and buck converters to power internal subsystems and external devices. A state machine controls power-on, power-off, enter-standby and exit-standby sequences of the LDOs and the buck converters.

MSW8535N offers ten LDO regulators to supply IO and external devices (e.g. RFIC, Bluetooth, SIM, LCD, camera, Memory Module, etc.). Each LDO regulator can be used in three modes (high power, low power or off mode) in order to achieve minimum power consumption.

Two buck converters are available to supply the core voltages and external memory inside the chip. One linear charger supports Li-Ion battery. One boost step-up converter can be used as a standalone controller, with the boosted level up to 16V. This can be used to support LCM backlight modules.

In addition, a low-power LDO is implemented to supply the RTC and charge a super-capacitor or a back-up battery.

### 2.3. Audio Subsystem

MSW8535N audio subsystem supports the GSM voiceband and vocoders (8 KHz sampling rate) and the stereo audio playback with sampling rate up to 48 KHz. Two fully-differential microphone inputs are available for the handset and headset microphone connections. The audio output integrates three drivers supporting the 16Ω/32Ω mono handset receiver, the 16Ω/32Ω stereo headset speaker, and the 10KΩ stereo line-out driver that is used for external power amplifier. One mono channel filterless 0.5W Class-D power amplifier is available for mono channel line-out speaker.

The GSM vocoders supported by MSW8535N include AMR (Adaptive Multirate), FR (Full-rate), EFR (Enhanced Full-rate) and HR (Half-rate).

The acoustic echo canceller and noise suppression algorithm are embedded to allow the implementation of true hands-free operation. In addition, FIR filters are available to compensate the audio quality imperfection from the speaker and the microphone during production calibration.

MSW8535N provides the capability to play back a wide range of digital stereo audio sources, including MIDI, WAV, AMR, MP3, and AAC. It also allows voice memo recording using the AMR encoder.

## 2.4. Multimedia

MSW8535N adds camera feature to the mobile handset by connecting a CMOS image sensor, which captures up to 3M pixels image, with YUV data output or raw Bayer RGB pattern output. The embedded Image Color Processor (ICP) not only enhances the image quality but also provides a variety of special image effects such as negative and oil painting. The playback file format could be YUV422, YUV420, and RGB565.

Both still image codec and video codec are implemented. The still image codec is compliant with ISO/IEC 10918-1 International Standard with JPEG (baseline) file format and supports resolution up to 3M pixels. The video codec can encode and decode H.263 and MPEG4 video bit-stream.

## 2.5. User Interface

MSW8535N can support two LCD displays simultaneously. The display interface is capable of supporting scan mode, command mode, and CCIR656 format output for different types of LCM. Embedded LCM controller and external/built-in PWM (for dimming control) are available. Touch panel controller is also integrated, which supports resistive type touch screen via a general auxiliary ADC.

MSW8535N connectivity interface offers many high-speed communication ports for various applications. High-speed UART and PCM interface can be connected to external device, such as Bluetooth. I<sup>2</sup>C master interface provides efficient control of external devices and camera modules.

MSW8535N integrates a Smart Card Interface dedicated to the GSM SIM card supporting transmission protocols T=0 (character based) and T=1 (block based). Automatic presence detection and 272-byte buffered FIFO mode are supported.

USB 2.0 / USB 1.1 controller of MSW8535N operates as a peripheral device in point-to-point communication with the host. The USB classes supported include mass storage, video class and communications device class (CDC). The USB port is also used for code downloading during production.

MSW8535N SPI works not only in slave mode but also in master mode. Full-duplex or half-duplex read/write mode with configurable number of words (up to 32768) can be transferred.

Embedded drivers for keypad, LED and vibrator are supported. Functions such as LED outputs (Red, Green, Blue, 12mA each) and keypad LED output (100mA), can be easily driven by the platform.

MSW8535N storage interface supports many popular storage cards on the market, including SD/T-Flash, MMC and Memory Stick. It also supports NAND-type flash and SPI serial flash interface.

### 3. TYPICAL APPLICATION

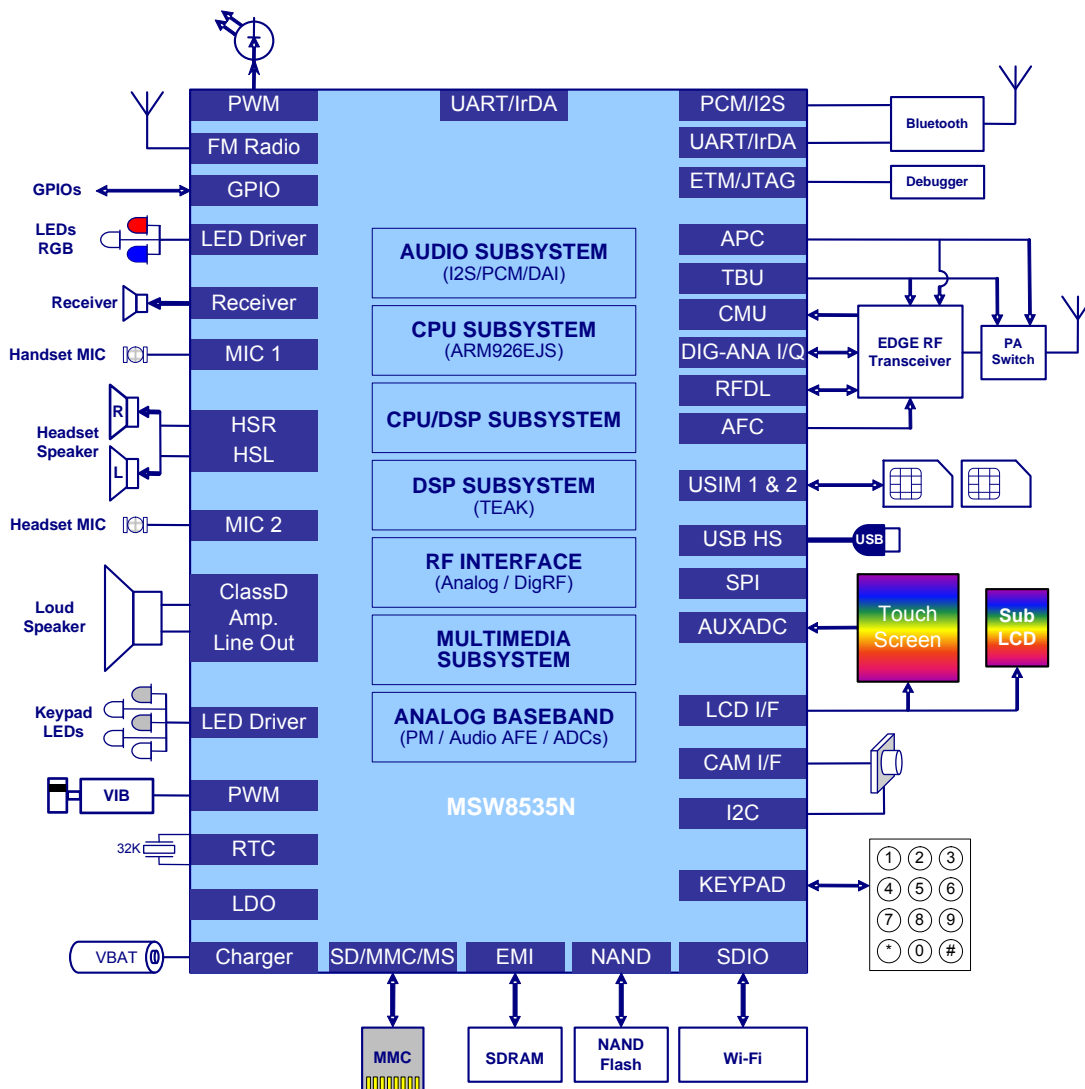


Figure 1: Typical Application with MSW8535N Based platform

## 4. FEATURES

### 4.1. Platform

#### 4.1.1. General

- 2.5G GSM/GPRS/EGPRS baseband support:
  - Quad band GSM
  - Up to GPRS class 10
  - Up to EGPRS class 10

#### 4.1.2. MCU Subsystem

- 32-bit ARM926EJ-STM processor with 16 KB instruction cache and 16 KB data cache
- Memory Management Unit for instruction and data
- Separate instruction and data AHB bus (32-bit)
- Embedded Trace Module (ETM9, Medium-large)
- Embedded Trace Buffer (ETB, 6 KB)
- Supports 32-bit (ARM mode), 16-bit (Thumb mode) and 8-bit Java bytecode (Jazelle mode) instruction sets
- Scalable clock frequency to optimize the power consumption to each specific application (up to 208 MHz)
- Dynamic mapping of the memory space

#### 4.1.3. Boot ROM

- Boot mode detection (boot pins)
- Configuration for a 13 or 26 MHz input clock
- Boot Loader: software downloading through the USB or UART interface

#### 4.1.4. External Memory Controllers

- SDRAM controller
  - Standard SDRAM protocol
  - 16-bit data interface
  - Supports 64Mbyte



#### 4.1.5. User Interface

- 8 x 8 keypad matrix scanner
- Supports multiple key detection and programmable debouncing function
- Two independent SIM/USIM controllers with hardware T=0 and T=1 compliant
- Two independent Pulse Width Modulated output channels
- Infrared capability up to 115.2 Kbps (physical layer link standard 1.2)
- Seven individual interrupts can be masked, cleared and mapped to either interrupt output (support wakeup from sleep mode)
- Three UARTs (two high speed UARTs up to 3.25Mbs, and one common speed UART at 115200 baud)
- I2C master
- I2S buses
- Three 32-bit timers
- USB 2.0/1.1 device
- Three on-chip LED drivers (Red, Green and Blue)
- Two Keypad LED Open-Drain outputs (100 mA) which can also be used to drive a vibrator
- Two 10-bit multi-channel general purpose auxiliary ADCs which can be used for touch-screen application, and power management functionality
- GPIOs: 1.8V GPIO, 2.8V GPIO, 1.8V/2.8V GPIO, and Interrupt

#### 4.1.6. Power Management

- Embedded PMU unit, which could provide following functions:
  - Thermal overload protection
  - Under voltage lock out protection
  - Over voltage protection
  - Li-Ion/Li-Po battery charge function
- Power Down mode for analog and digital circuits
- Processor Sleep Mode
- Embedded Real Time Clock (RTC) to provide 32 KHz digital clock output in extremely low power consumption
- One 7-channel 10-bit auxiliary ADC with two inputs dedicated to battery and charger measurement
- Two buck converters to provide high power of the core supply
- Ten LDOs for IO and external components to achieve power saving and independency
- Dual SIM LDOs

#### 4.1.7. Debug Function

- Debug bus for monitoring internal signals
- 32-bit debug bus for peripherals
- 16-bit debug bus for interrupts, clocks, GSM timer, DSP timer and system timer
- Local debug bus in each module with configurable signal multiplexing
- Debug bus multiplexing at the sub-system and top level
- Individual bit selection and bits reversing capabilities
- Two ways of configuration:
  - JTAG interface
  - Under CPU control

## 4.2. Modem

### 4.2.1. Radio Related

- GMSK/8PSK modulator with analog I and Q channel outputs
- RX data format:
  - Data sample rate (IQ couple) per symbol: 1x, 2x or 4x
  - I and Q resolution: 12-bit
- RX A/D Converter
  - Output rate of 48x
  - Separate power supplies for analog and digital parts
  - Fully differential architecture
- TX data format
  - 4 bits/symbol open to GSM, EDGE or proprietary GMSK coding (DigRF)
  - 1 bit/symbol in GSM and 3 bits/symbol in EDGE
- TX D/A converter
  - Dual matched differential digital to analog converters
  - 10-bit resolution
  - Programmable gain on both I and Q channels
  - Separate power supply for analog and digital parts
- Modem: supporting GSM/GPRS/EGPRS
  - GPRS up to Class 10 (CS-1 to CS-4, 9.05 to 21.4 Kbps per timeslot)
  - EGPRS Class 10 release 4 compliant with no restriction (MSC-1 to MSC-9 in RX and TX, 10.6 to 61.85 Kbps per timeslot)
- Speech Coders: FR, EFR, HR, NB-AMR
- Hardware Accelerator for GSM/GPRS Receive Path
  - A5/1 and A5/2 encryption algorithms
  - GEA1 and GEA2 encryption for GPRS
  - Ciphering and deciphering sequence processing
- Bi-directional serial digital IQ interface to/from the RF transceiver
- Bi-directional serial analog IQ interface to/from the RF transceiver
- Automatic Gain Control (AGC)
- Automatic Power Control (APC)
- Automatic Frequency Control (AFC)

### 4.2.2. Voice & Audio Codec

- Two microphone inputs: for handset and headset
  - Headset detection circuitry
  - Integrated mono channel microphone bias and detection circuitry
- Output audio drivers support:
  - 16Ω/32Ω handset receiver
  - Stereo 16Ω/32Ω headset speaker
  - Stereo 10KΩ line-out driver for external amplifier
- Low-noise PLL and sampling-rate converter for multi-rate audio signal processing
- Low-power mono voice ADC and stereo audio DAC
- Supports built-in stereo FM audio play
- Adjustable side-tone mixing
- Independent volume controls for both left and right channels
- GSM-compliance mask filters (VUL/VDL) in voice uplink/downlink
- Automatic digital gain control to maintain the constant count envelope during voice call
- PCM/I<sup>2</sup>S for Bluetooth
  - Master mode with clock rate 128kHz, 256kHz or 512kHz
  - Slave mode with clock rate from 128kHz up to 2.048MHz
  - Long synchro pulse or programmable short synchro pulse
  - 8kHz and 16kHz sample rate (16kHz is not supported by DSP, so it is not actually usable)
  - MSB first or LSB first
  - Companding modes: 16-bit linear, 8-bit-law, 8-bit μ-law, 8-bit linear (upper byte or lower byte)

## 4.3. Multi-media

### 4.3.1. Graphic Compression

- GIF decoder (GIF87, GIF89a)
- PNG decoder

### 4.3.2. JPEG Decoder & Encoder

- Supports YUV422 or grayscale format encode
- Supports YUV444, YUV422H1V2, YUV422H2V1, YUV420, and YUV411 decompression
- The JPEG decoder supports both color picture and grayscale format (up to 8176x8176 pixel pictures)
- The decoded output is stored in YUV422H2V1 format with original, 1/2, or 1/4 downscale picture
- Four Huffman tables (Y-DC, Y-AC, C-DC, and C-AC) are supported to decode JPEG source pictures with default or customized Huffman table

### 4.3.3. LCD Controller & Interface

- Supports I80/M68 and RGB sync parallel interface
- Capable of displaying up to HVGA/320x480 (by condition) and up to 16M colors LCM
- Supports 8-bit parallel data streams in CCIR656 format
- Supports hardware display rotation

#### 4.3.4. Audio CODEC

- Adaptive Multi-Rate (AMR) encoding for voice
- AMR, MP3, AAC decoding for media

#### 4.3.5. T-Flash Controller

- The card reader block supports T-flash interface with support for read/write/erase operation
- Supports both 1-bit and 4-bit mode
- Supports SDHC and normal type

#### 4.3.6. Image Signal Processor

- Image Signal Processing (ISP)
  - The ISP Engine processes CMOS image sensor's RGB raw data into YCbCr 4:2:2 data
  - Black level correction
  - Lens shading compensation
  - Color interpolation
  - Gamma correction
  - Suppression of inherent false color of mosaic image sensor
  - Auto exposure control
  - Auto white balance and auto focus control

#### 4.3.7. Video CODEC

- Compression engine encodes captured video raw data in H.263 format

#### 4.3.8. Graphic Accelerator

- 3D Graphic Engine to support OpenGL ES 1.1

**5. BALL OUT****(Top View)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	
<b>A</b>		F_DA6	F_DA4		F_DA0	F_WRZ		UART2_RXD	MPIF2_CLK		MPIF2_D3	VDD_GPIO_A2		
<b>B</b>	VDD_APLL	F_DA7	F_DA5	F_DA2	F_DA1	F_CLE	F_CEN	GPIO[22]	MPIF2_BUSY	MPIF2_CS0N	MPIF2_D1	MPIF2_D2	SDIO_CLK	
<b>C</b>	VDD_SDR	GND_APLL		F_DA3			F_CEN1			MPIF2_D0			BT_SCK	
<b>D</b>	GND_SDR	SDR_DQ[5]	F_ALE											
<b>E</b>		SDR_DQ[7]			SDR_DQ[15]	F_RDZ	GPIO[23]	UART2_CTS	UART2_TXD	VDD_MPIF2	GPIO[16]	GPIO[20]	UART1_TXD	
<b>F</b>	SDR_DQ[4]	SDR_DQ[2]			SDR_DQ[14]	SDR_DQ[9]	F_RBN	UART2_RTS	MGPIO[90]	MGPIO[91]	MGPIO[93]	GPIO[15]	UART1_RXD	
<b>G</b>		SDR_DQ[1]	SDR_DQ[6]		SDR_DQ[11]	SDR_DQ[12]								
<b>H</b>	GND_SDR	SDR_DQ[0]			SDR_DQ[10]	SDR_DQ[8]		VDD_MNAND	GPIO[4]	VDD_GPIO_C	MGPIO[95]	GPIO[21]	UART1_CTS	
<b>J</b>	VDD_SDR	GND_SDR	SDR_DQ[3]		SDR_DQ[13]	SDR_DQM[1]		F_WPT						
<b>K</b>			SDR_A[10]		SDR_A[5]	SDR_A[6]					GNDIO	GPIO[19]	MGPIO[92]	GNDIO
<b>L</b>	SDR_DQM[0]	SDR_A[4]			SDR_A[2]			SDR_A[9]		VDD_MSD				
<b>M</b>	GND_SDR	VDD_SDR			SDR_A[11]	SDR_A[3]		SDR_CSZ		SD_MS_IN_S		VDDC	GNDC	
<b>N</b>			SDR_BA[0]		SDR_WEZ	SDR_CASZ		SDR_RASZ		SD_PCTL		GNDC	GNDAUDD	
<b>P</b>		SDR_MCLK	SDR_BA[1]		SDR_A[12]	SDR_CKE				SD_CDZ		GNDGSUB_FM	GNDC	
<b>R</b>	SDR_A[1]	SDR_A[0]			SDR_A[7]	SDR_A[8]		SD_D3		SD_D1		GNDAUDRV	GNDAUDDA	
<b>T</b>	SD_D0	SD_D2			SD_CLK	SD_CMD		COL[1]		NC				
<b>U</b>		COL[2]	COL[4]		SD_WPT	COL[0]		ROW[1]		HDRP	SPKDET	HSDET	VDDC	
<b>V</b>	ROW[0]	ROW[4]			VDD_GPIO_A1	COL[3]		ROW[3]						
<b>W</b>	ROW[2]	VDD_USIM1			COL[5]	ROW[5]		FM_TST1	GNDPLL_FM	HDRN	HPNCM	HSMBIAS	AUXADC3	
<b>Y</b>		USIM1DATA	USIM1RST		USIM2CLK	USIM2RST								
<b>A A</b>	VDD_USB	USIM1CLK			USIM2DATA	VDD_USIM2	FM_TST2	PMU_PWREN	HPNL	HPNR	MICBIAS	PATEMP	AUXADC1	
<b>A B</b>	USB_DP	USB_DM			GNDLNA_FM	GND_FM	ONOFF	ABBRESETB	PMTEST	MICINP	MICINN	AUDREFN	VAUXLDO	
<b>A C</b>		GND_USB	GNDC											
<b>A D</b>	NC	GNDC		VDD_FM			VDDADC_FM			VDDAUD			BATTEMP	
<b>A E</b>	NC	NC	NC	FM_RXM	FM_RXP	FM_REFP	FM_REFN	LINEROUTN	LINEROUTP	VABBAUD	XOUT	AUDREFP	HSMICINP	
<b>A F</b>	NC	NC	GNDC		VLNACAP_FM	VDDPLL_FM		LINEROUTP	LINEROUTN		XIN	VRTCCAP		
	1	2	3	4	5	6	7	8	9	10	11	12	13	

14	15	16	17	18	19	20	21	22	23	24	25	26	
	SDIO_CMD	SPI_CLK		SPI_DI	MPIF1_CS1N		MPIF1_D3	MPIF1_D2		LCD_D14	LCD_D12	LCD_D8	<b>A</b>
SDIO_D2	MGPIO[89]	SDIO_D3	SPI_CS0_N	SPI_DO	MPIF1_CLK	MPIF1_D0	MPIF1_BUSY	MPIF1_CS0N	LCD_CLK	LCD_D11	LCD_D8	LCD_D0	<b>B</b>
BTWS			MGPIO[81]			MPIF1_D1			LCD_D10		LCD_D2	SR_D1	<b>C</b>
										LCD_D4	SR_D7		<b>D</b>
BTSDO	I2S_WS	I2S_SDI	MGPIO[83]	SDIO_D0	MGPIO[79]	LCD_CS0_N	LCD_D16	LCD_RD			SR_PWRDN	SR_HSYNC	<b>E</b>
BTSDI	VDD_SDIO	I2S_SCL	MGPIO[82]	MGPIO[80]	MGPIO[1]	LCD_PWM0	LCD_D6	SR_D9			GPIO[18]	TBU05	<b>F</b>
							VDD_MLCD	SR_D5		SR_I2CSDA	TBU03		<b>G</b>
UART1_RTS	VDD_MPIF1	MGPIO[84]	VDD_BJTAG	VDD_GPIO_B	LCD_D13		LCD_D3	SR_D0			SYSCLKEN	TBU07	<b>H</b>
					SR_I2CSCL		SR_D8	SR_MCLK			RXTXEN	TBU01	<b>J</b>
MGPIO[94]	SDIO_PCTL	SDIO_D1	LCD_D5		SR_D2		SR_D4	SR_PCLK		PMU_SCLK	SPI_RF_EN		<b>K</b>
			LCD_D7		SR_VSYNC		SR_D3	GPIO[17]			PMU_BATON	VDD3	<b>L</b>
VDDC	MCP_HIZ		LCD_D9		SR_D6		RXTXDATA	SPI_RF_OUT			ABB_TEST	PMU_CLK	<b>M</b>
GND_A	GND_C		LCD_D15		VDD_MSR		SPI_RF_IN	I2CCLK		VPER4	VPER3		<b>N</b>
GND_AUX	GND_RFD		LCD_D17		PMU_SDIO		I2CDATA	MCLKSEL		VPER2	GNDIO		<b>P</b>
GND_RTC	GND1		LCD_D1		VDDPEXT1		TBU06	VPER1			VIO1	QM	<b>R</b>
			LCD_CS1_N		TBU04		TBU02	VIO2			IM	QP	<b>T</b>
JTAG_TCK	LCD_PWM1	LCD_CMD	LCD_WR		SPI_RF_CLK		MPLL_BYPASS	VA		VSIM1	IP		<b>U</b>
					EXT_IQ_CLK		MAIN_MCLK	VDIG			APCOUT	AFCOUT	<b>V</b>
KEYPAD2	JTAG_TDO	JTAG_TDI	JTAG_TMS	RTCK	TBU00		VDIGRF	VSIM2			PMU_BKEN	PMU_CHGDET	<b>W</b>
							VREFSYS	GNDBK1		PMU_BKSW1	VBKOUT1		<b>Y</b>
AUXADC0	BLEOD	GLEOD	JTAG_NTRST		VDD2	VDD1	GNDAMP	VINUSB		VBUSIN	GNDRF	PMU_OVPEXT	<b>A A</b>
AUXADC2	KEYPAD1	RLEDOD	PMU_SPKON	PMU_SPKOP	VBATTAMP	PMU_SPKIP	PMU_SPKIN	PMU_INT			VRF2	VBSTISENSE	<b>A B</b>
							PMU_BSTEIN			VRF1	VBSTFB		<b>A C</b>
VABBRF			VADAIN			USB_CID	VBATT_AB_B	VBATT_AB_B	VSTDLD02		GNDBST	VBATT_RF	<b>A D</b>
HSMICINN	GNDRFA	VGATEDRV	VCS	VCHG_ISENSE	VBATT_AVDD	VDDPEXT2	VUSB	VBATT_BST	VBATT_BK	PMU_BSTSW	GNDBK2	PMU_BSTGATE	<b>A E</b>
	RFREFN	RFREFP		VREFEXT	GND_A		VABB1	VABB2		VBKOUT2	PMU_BKSW2	PMU_DFTMD	<b>A F</b>
<b>14</b>	<b>15</b>	<b>16</b>	<b>17</b>	<b>18</b>	<b>19</b>	<b>20</b>	<b>21</b>	<b>22</b>	<b>23</b>	<b>24</b>	<b>25</b>	<b>26</b>	

Figure 2: MSW8535N Ball Out

## 6. DEVICE PIN LIST

Table 1: Device Pin List

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
<b>RF Digital Interface (DigRF &amp; RFIC)</b>							
U19	SPI_RF_CLK	-	D	O	VDIGRF	RFIC: CtrlClk	O/L
K25	SPI_RF_EN	-	D	O	VDIGRF	RFIC: CtrlEn	O/H
M22	SPI_RF_OUT	CD	D	I/O	VDIGRF	RFIC: CtrlData I/O	I/L
N21	SPI_RF_IN	CD	D	I	VDIGRF	RFIC: CtrlData Input	I/L
H25	SYSCLKEN	-	D	O	VDIGRF	RFIC: CHIPEN	O/H
J25	RXTXEN	CD	D	I/O	VDIGRF	DIGRF: RxTxEn	I/L
M21	RXTXDATA	CD	D	I/O	VDIGRF	DIGRF: RxTxData	I/L
V19	EXT_IQ_CLK	-	D	I	VDIGRF	Digital RF Data Clock for DigRF Mode (MAIN_CLK can also be used)	I/HiZ
W19	TBU00	-	D	O	VDD_GPIO_B	Time Base Unit Output 0	O/L
J26	TBU01	-	D	O	VDD_GPIO_B	Time Base Unit Output 1	O/L
T21	TBU02	-	D	O	VDD_GPIO_B	Time Base Unit Output 2	O/L
G25	TBU03	-	D	O	VDD_GPIO_B	Time Base Unit Output 3	O/L
T19	TBU04	-	D	O	VDD_GPIO_B	Time Base Unit Output 4	O/L
F26	TBU05	CUD	D	O	VDD_GPIO_B	Time Base Unit Output 5	I/H
R21	TBU06	CUD	D	O	VDD_GPIO_B	Time Base Unit Output 6	I/HiZ
H26	TBU07	CD	D	O	VDD_GPIO_B	Time Base Unit Output 7	I/L
<b>RF Analog Interface</b>							
AF15	RFREFN	-	A	O	2.8	ABB RF REF-	-
AF16	RFREFP	-	A	O	2.8	ABB RF REF+	-
R26	QM	-	A	O	2.8	RX,TX Q-	-
T26	QP	-	A	O	2.8	RX,TX Q+	-
T25	IM	-	A	O	2.8	RX,TX I-	-
U25	IP	-	A	O	2.8	RX,TX I+	-
V26	AFCOUT	-	A	O	2.8	AFC Output	-
V25	APCOUT	-	A	O	2.8	APC Output	-
<b>GPIO Interface</b>							
H9	GPIO[4]	CUD	D	I/O	VDD_GPIO_C	General Purpose Input Output 4	I/HiZ

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
F12	GPIO[15]	CD	D	I/O	VDD_GPIO_A2	General Purpose Input Output 15	I/L
E11	GPIO[16]	CD	D	I/O	VDD_GPIO_A2	General Purpose Input Output 16	I/L
L22	GPIO[17]	CD	D	I/O	VDD_GPIO_B	General Purpose Input Output 17	I/L
F25	GPIO[18]	CD	D	I/O	VDD_GPIO_B	General Purpose Input Output 18	I/L
K11	GPIO[19]	CD	D	I/O	VDD_GPIO_A2	General Purpose Input Output 19	I/HiZ
E12	GPIO[20]	CD	D	I/O	VDD_GPIO_A2	General Purpose Input Output 20	I/L
H12	GPIO[21]	CD	D	I/O	VDD_GPIO_A2	General Purpose Input Output 21	I/L
B8	GPIO[22]	CD	D	I/O	VDD_GPIO_C	General Purpose Input Output 22	I/L
E7	GPIO[23]	CUD	D	I/O	VDD_GPIO_C	General Purpose Input Output 23	I/L
F19	MGPIO[1]	CUD	D	I/O	VDD_EMI	General Purpose Input Output M1	I/H
E19	MGPIO[79]	CUD	D	I/O	VDD_MPIF1	General Purpose Input Output M79	I/H
F18	MGPIO[80]	CUD	D	I/O	VDD_MPIF1	General Purpose Input Output M80	I/H
C17	MGPIO[81]	CUD	D	I/O	VDD_MPIF1	General Purpose Input Output M81	I/H
F17	MGPIO[82]	CUD	D	I/O	VDD_MPIF1	General Purpose Input Output M82	I/H
E17	MGPIO[83]	CUD	D	I/O	VDD_MPIF1	General Purpose Input Output M83	I/H
H16	MGPIO[84]	CUD	D	I/O	VDD_MPIF1	General Purpose Input Output M84	O/L
B15	MGPIO[89]	CUD	D	I/O	VDD_MPIF1	General Purpose Input Output M89	I/HiZ
F9	MGPIO[90]	CUD	D	I/O	VDD_MPIF2	General Purpose Input Output M90	I/HiZ



Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
F10	MGPIO[91]	CUD	D	I/O	VDD_MPIF2	General Purpose Input Output M91	I/HiZ
K12	MGPIO[92]	CUD	D	I/O	VDD_MPIF2	General Purpose Input Output M92	I/HiZ
F11	MGPIO[93]	CUD	D	I/O	VDD_MPIF2	General Purpose Input Output M93	I/HiZ
K14	MGPIO[94]	CUD	D	I/O	VDD_MPIF2	General Purpose Input Output M94	I/HiZ
H11	MGPIO[95]	CUD	D	I/O	VDD_MPIF2	General Purpose Input Output M95	I/HiZ
<b>External Interrupt Interface</b>							
H9	GPIO[4]	CUD	D	I/O	VDD_GPIO_C	General Purpose Input Output 4, also can be used as Interrupt 0	I/HiZ
E12	GPIO[20]	CD	D	I/O	VDD_GPIO_A2	General Purpose Input Output 20, also can be used as Interrupt 1	I/L
H12	GPIO[21]	CD	D	I/O	VDD_GPIO_A2	General Purpose Input Output 21, also can be used as Interrupt 2	I/L
E7	GPIO[23]	CUD	D	I/O	VDD_GPIO_C	General Purpose Input Output 23, also can be used as Interrupt 2	I/L
B8	GPIO[22]	CD	D	I/O	VDD_GPIO_C	General Purpose Input Output 22, also can be used as Interrupt 3	I/L
L22	GPIO[17]	CD	D	I/O	VDD_GPIO_B	General Purpose Input Output 17, also can be used as Interrupt 4	I/L
V19	EXT_IQ_CLK	-	D		VDIGRF	Digital RF Data Clock for DigRF Mode, also can be used as Interrupt 5	I/HiZ
F12	GPIO[15]	CD	D		VDD_GPIO_A2	General Purpose Input Output 15, also can be used as Interrupt 6	I/L
<b>UART/IrDA Interface</b>							

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
E13	UART1_TXD	CD	D	I/O	VDD_GPIO_A2	UART1, also can be used as GPIO	I/L
F13	UART1_RXD	CD	D	I/O	VDD_GPIO_A2	UART1, also can be used as GPIO	I/L
H14	UART1_RTS	CD	D	I/O	VDD_GPIO_A2	UART1, also can be used as GPIO	I/L
H13	UART1_CTS	CD	D	I/O	VDD_GPIO_A2	UART1, also can be used as GP10	I/L
E9	UART2_TXD	CUD	D	I/O	VDD_GPIO_C	UART2, also can be used as GPIO	O/L
A8	UART2_RXD	CUD	D	I/O	VDD_GPIO_C	UART2, also can be used as GPIO	O/L
E8	UART2_CTS	CUD	D	I/O	VDD_GPIO_C	UART2, also can be used as GPIO	I/L
F8	UART2_RTS	CUD	D	I/O	VDD_GPIO_C	UART2, also can be used as GPIO	I/H
<b>SDIO Interface</b>							
B13	SDIO_CLK	CUD	D	O	VDD_SDIO	SDIO Interface Clock	I/L
A15	SDIO_CMD	CUD	D	I/O	VDD_SDIO	SDIO Interface Command	I/L
K15	SDIO_PCTL	CUD	D	I/O	VDD_SDIO	SDIO Power Control	I/HiZ
E18	SDIO_D0	CUD	D	I/O	VDD_SDIO	SDIO Interface Data Bit [0]	I/L
K16	SDIO_D1	CUD	D	I/O	VDD_SDIO	SDIO Interface Data Bit [1]	I/L
B14	SDIO_D2	CUD	D	I/O	VDD_SDIO	SDIO Interface Data Bit [2]	I/L
B16	SDIO_D3	CUD	D	I/O	VDD_SDIO	SDIO Interface Data Bit [3]	I/L
<b>SPI Interface</b>							
A16	SPI_CLK	CUD	D	O	VDD_EMI	SPI Interface Clock	O/L
B18	SPI_DO	CUD	D	I	VDD_EMI	SPI Interface Data Output	I/H
A18	SPI_DI	CUD	D	O	VDD_EMI	SPI Interface Data Input	O/L
B17	SPI_CS0_N	CUD	D	O	VDD_EMI	SPI Interface Chip Select	O/H
<b>MPIF Interface</b>							
B19	MPIF1_CLK	CUD	D	O	VDD_MPIF1	MPIF1 Interface Clock	O/L
B22	MPIF1_CS0N	CUD	D	O	VDD_MPIF1	MPIF1 Interface Chip Select 0 (active low)	O/H

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
A19	MPIF1_CS1N	CUD	D	O	VDD_MPIF1	MPIF1 Interface Chip Select 1 (active low)	I/H
B21	MPIF1_BUSY	CUD	D	I	VDD_MPIF1	MPIF1 Interface Slave Busy	I/L
B20	MPIF1_D0	CUD	D	I/O	VDD_MPIF1	MPIF1 Interface Data Bit [0]	I/H
C20	MPIF1_D1	CUD	D	I/O	VDD_MPIF1	MPIF1 Interface Data Bit [1]	I/H
A22	MPIF1_D2	CUD	D	I/O	VDD_MPIF1	MPIF1 Interface Data Bit [2]	I/L
A21	MPIF1_D3	CUD	D	I/O	VDD_MPIF1	MPIF1 Interface Data Bit [3]	I/L
A9	MPIF2_CLK	CUD	D	O	VDD_MPIF2	MPIF2 Interface Clock	I/HiZ
B10	MPIF2_CS0N	CUD	D	O	VDD_MPIF2	MPIF2 Interface Chip Select 0 (active low)	I/H
B9	MPIF2_BUSY	CUD	D	I	VDD_MPIF2	MPIF2 Interface Chip Select 1 (active low)	I/HiZ
C10	MPIF2_D0	CUD	D	I/O	VDD_MPIF2	MPIF2 Interface Data Bit [0]	I/HiZ
B11	MPIF2_D1	CUD	D	I/O	VDD_MPIF2	MPIF2 Interface Data Bit [1]	I/HiZ
B12	MPIF2_D2	CUD	D	I/O	VDD_MPIF2	MPIF2 Interface Data Bit [2]	I/HiZ
A11	MPIF2_D3	CUD	D	I/O	VDD_MPIF2	MPIF2 Interface Data Bit [3]	I/HiZ
<b>Memory Card Interface</b>							
N10	SD_PCTL	CUD	D	O	VDD_MSD	SD Card Power Control	I/HiZ
T1	SD_D0	CUD	D	I/O	VDD_MSD	SD Card Data Bit [0]	I/L
R10	SD_D1	CUD	D	I/O	VDD_MSD	SD Card Data Bit [1]	I/L
T2	SD_D2	CUD	D	I/O	VDD_MSD	SD Card Data Bit [2]	I/L
R8	SD_D3	CUD	D	I/O	VDD_MSD	SD Card Data Bit [3]	I/L
T6	SD_CMD	CUD	D	I/O	VDD_MSD	SD Card Command	I/L
T5	SD_CLK	CUD	D	O	VDD_MSD	SD Card Clock	I/L
P10	SD_CDZ	CUD	D	I	VDD_MSD	SD Card Detect (active low)	I/H
U5	SD_WPT	CUD	D	I	VDD_MSD	SD Card Write Protect	I/L

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
M10	SD_MS_INS	CUD	D	I	VDD_MSD	Memory Stick Insertion Detect	I/H
<b>I2S/PCM Interface</b>							
E14	BTSDO	CD	D	I/O	VDD_GPIO_A2	PCM G711 Frame Data Output	I/L
F14	BTSDI	CD	D	I/O	VDD_GPIO_A2	PCM G711 Frame Data Input	I/L
C13	BTSCK	CD	D	I/O	VDD_GPIO_A2	PCM G711 Frame Bit Clock Signal	I/L
C14	BTWS	CD	D	I/O	VDD_GPIO_A2	PCM G711 Frame Synchronization Signal	I/L
E15	I2S_WS	CUD	D	I/O	VDD_SDIO	Word Select Input	I/L
E16	I2S_SDI	CUD	D	I/O	VDD_SDIO	Audio Serial Data Input	I/L
F16	I2S_SCL	CUD	D	I/O	VDD_SDIO	Audio Sample Clock Input	I/L
<b>Parallel/RGB LCD Interface</b>							
B26	LCD_D0	CUD	D	O	VDD_MLCD	LCD Data Bit [0]	O/H
R17	LCD_D1	CUD	D	O	VDD_MLCD	LCD Data Bit [1]	O/H
C25	LCD_D2	CUD	D	O	VDD_MLCD	LCD Data Bit [2]	O/H
H21	LCD_D3	CUD	D	O	VDD_MLCD	LCD Data Bit [3]	O/H
D24	LCD_D4	CUD	D	O	VDD_MLCD	LCD Data Bit [4]	O/H
K17	LCD_D5	CUD	D	O	VDD_MLCD	LCD Data Bit [5]	O/H
F21	LCD_D6	CUD	D	O	VDD_MLCD	LCD Data Bit [6]	O/H
L17	LCD_D7	CUD	D	O	VDD_MLCD	LCD Data Bit [7]	O/L
A26 B25	LCD_D8	CUD	D	O	VDD_MLCD	LCD Data Bit [8]	O/L
M17	LCD_D9	CUD	D	O	VDD_MLCD	LCD Data Bit [9]	O/L
C23	LCD_D10	CUD	D	O	VDD_MLCD	LCD Data Bit [10]	O/L
B24	LCD_D11	CUD	D	O	VDD_MLCD	LCD Data Bit [11]	O/L
A25	LCD_D12	CUD	D	O	VDD_MLCD	LCD Data Bit [12]	O/L
H19	LCD_D13	CUD	D	O	VDD_MLCD	LCD Data Bit [13]	O/L
A24	LCD_D14	CUD	D	O	VDD_MLCD	LCD Data Bit [14]	O/L
N17	LCD_D15	CUD	D	O	VDD_MLCD	LCD Data Bit [15]	O/L
E21	LCD_D16	CUD	D	O	VDD_MLCD	LCD Data Bit [16]	O/L

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
P17	LCD_D17	CUD	D	O	VDD_MLCD	LCD Data Bit [17]	O/L
E20	LCD_CS0_N	CUD	D	O	VDD_MLCD	LCD Device Select 0 (active low)	O/H
T17	LCD_CS1_N	CUD	D	O	VDD_MLCD	LCD Device Select 1 (active low)	O/H
U16	LCD_CMD	CD	D	O	VDD_MLCD	LCD Command	O/L
U17	LCD_WR	CUD	D	O	VDD_MLCD	LCD Write Enable / Scan Mode VSYNC	O/H
E22	LCD_RD	CUD	D	O	VDD_MLCD	LCD Read Enable / Scan Mode Data Enable	O/H
B23	LCD_CLK	CD	D	O	VDD_MLCD	LCD Control Clock	O/L
F20	LCD_PWM0	CUD	D	O	VDD_MLCD	Pulse Width Modulation Output 0	O/L
U15	LCD_PWM1	CUD	D	O	VDD_MLCD	Pulse Width Modulation Output 1	O/H
<b>Audio Interface</b>							
AA10	HPNR	-	A	O	3.2	Headset Speaker R	-
W11	HPNCM	-	A	O	3.2	Headset Speaker CM	-
AA9	HPNL	-	A	O	3.2	Headset Speaker L	-
W10	HDRN	-	A	O	3.2	Handset Receiver -	-
U10	HDRP	-	A	O	3.2	Handset Receiver +	-
AE9	LINEROUTP	-	A	O	3.2	Audio Line Out Driver R+	-
AF9	LINEROUTN	-	A	O	3.2	Audio Line Out Driver R-	-
AF8	LINELOUTP	-	A	O	3.2	Audio Line Out Driver L+	-
AE8	LINELOUTN	-	A	O	3.2	Audio Line Out Driver L-	-
U12	HSDET	-	A	I	3.2	Headset Detection Input	-
AB10	MICINP	-	A	I	2.5	Handset MIC In+	-
AB11	MICINN	-	A	I	2.5	Handset MIC In-	-
AE13	HSMICINP	-	A	I	2.5	Headset MIC In+	-
AE14	HSMICINN	-	A	I	2.5	Headset MIC In-	-
AE12	AUDREFP	-	A	O	2.5	ABB Audio REF+	-
AB12	AUDREFN	-	A	O	2.5	ABB Audio REF-	-
AA11	MICBIAS	-	A	O	3.2	Handset MIC Bias	-
W12	HSMBIAS	-	A	O	3.2	Headset MIC Bias	-

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
U11	SPKDET	-	A	I	3.2	Speaker Detection Input	-
AB20	PMU_SPKIP	-	A	I	3.2	Class D AMP Input+	-
AB21	PMU_SPKIN	-	A	I	3.2	Class D AMP Input-	-
AB18	PMU_SPKOP	-	A	O	4.2	Class D AMP Output+	-
AB17	PMU_SPKON	-	A	O	4.2	Class D AMP Output-	-
<b>Auxiliary Interface</b>							
AA12	PATEMP	-	A	I	3.2	Power Amp Temp Connection	-
AD13	BATTEMP	-	A	I	3.2	Battery Thermistor Connect	-
AA14	AUXADC0	-	A	I	3.2	Auxiliary ADC Input 0 / YN Touch Screen	-
AA13	AUXADC1	-	A	I	3.2	Auxiliary ADC Input 1 / XN Touch Screen	-
AB14	AUXADC2	-	A	I	3.2	Auxiliary ADC Input 2 / YP Touch Screen	-
W13	AUXADC3	-	A	I	3.2	Auxiliary ADC Input 3 / XP Touch Screen	-
<b>CMOS Sensor Interface</b>							
H22	SR_D0	CD	D	I	VDD_MSR	Sensor Data Bit [0]	I/H
C26	SR_D1	CD	D	I	VDD_MSR	Sensor Data Bit [1]	I/H
K19	SR_D2	CD	D	I	VDD_MSR	Sensor Data Bit [2]	I/H
L21	SR_D3	CD	D	I	VDD_MSR	Sensor Data Bit [3]	I/H
K21	SR_D4	CD	D	I	VDD_MSR	Sensor Data Bit [4]	I/H
G22	SR_D5	CD	D	I	VDD_MSR	Sensor Data Bit [5]	I/H
M19	SR_D6	CD	D	I	VDD_MSR	Sensor Data Bit [6]	I/H
D25	SR_D7	CD	D	I	VDD_MSR	Sensor Data Bit [7]	I/H
J21	SR_D8	CD	D	I	VDD_MSR	Sensor Data Bit [8]	I/H
F22	SR_D9	CD	D	I	VDD_MSR	Sensor Data Bit [9]	I/H
G24	SR_I2CSDA	CUD	D	I/O	VDD_MSR	I <sup>2</sup> C Control Data for Sensor Configuration	I/H
J19	SR_I2CSCL	CUD	D	O	VDD_MSR	I <sup>2</sup> C Control Clock for Sensor Configuration	I/H
J22	SR_MCLK	CD	D	O	VDD_MSR	Sensor Master Clock	O/L
E25	SR_PWRDN	CD	D	O	VDD_MSR	Sensor Power Down Control	O/L

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
E26	SR_HSYNC	CUD	D	I	VDD_MSR	Sensor Horizontal Synchronization Control	I/L
L19	SR_VSYNC	CUD	D	I	VDD_MSR	Sensor Vertical Synchronization Control	I/L
K22	SR_PCLK	CD	D	I	VDD_MSR	Sensor Pixel Clock	I/H
<b>Keypad Interface</b>							
U6	COL[0]	CU	D	I/O	VDD_GPIO_A1	Keypad Column 0 Scan	I/H
T8	COL[1]	CU	D	I/O	VDD_GPIO_A1	Keypad Column 1 Scan	I/H
U2	COL[2]	CU	D	I/O	VDD_GPIO_A1	Keypad Column 2 Scan	I/H
V6	COL[3]	CU	D	I/O	VDD_GPIO_A1	Keypad Column 3 Scan	I/H
U3	COL[4]	CU	D	I/O	VDD_GPIO_A1	Keypad Column 4 Scan	I/H
W5	COL[5]	CU	D	I/O	VDD_GPIO_A1	Keypad Column 5 Scan	I/H
V1	ROW[0]	CD	D	I/O	VDD_GPIO_A1	Keypad Row 0 Scan	O/L
U8	ROW[1]	CD	D	I/O	VDD_GPIO_A1	Keypad Row 1 Scan	O/L
W1	ROW[2]	CD	D	I/O	VDD_GPIO_A1	Keypad Row 2 Scan	O/L
V8	ROW[3]	CD	D	I/O	VDD_GPIO_A1	Keypad Row 3 Scan	O/L
V2	ROW[4]	CD	D	I/O	VDD_GPIO_A1	Keypad Row 4 Scan	O/L
W6	ROW[5]	CD	D	I/O	VDD_GPIO_A1	Keypad Row 5 Scan	O/L
<b>SIM Card Interface</b>							
Y2	USIM1DATA	CD	D	I/O	VDD_UIM1	USIM1 Serial Data	O/L
Y3	USIM1RST	CD	D	O	VDD_UIM1	USIM1 Reset	O/L
AA2	USIM1CLK	CD	D	O	VDD_UIM1	USIM1 Serial Clock	O/L
AA5	USIM2DATA	CD	D	I/O	VDD_UIM2	USIM1 Serial Data	I/HiZ
Y6	USIM2RST	CD	D	O	VDD_UIM2	USIM1 Reset	I/HiZ
Y5	USIM2CLK	CD	D	O	VDD_UIM2	USIM1 Serial Clock	I/HiZ
<b>USB Interface</b>							
AB1	USB_DP	-	A	I/O	AVDD_USB	USB Bus Data D+	-
AB2	USB_DM	-	A	I/O	AVDD_USB	USB Bus Data D-	-
AD20	USB_CID		A	I	3.2	USB CID	-
<b>RTC Interface</b>							
AE11	XOUT	-	A	O	2.5	32KHz XO Output	-
AF11	XIN	-	A	I	2.5	32KHz XO Input	-

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
<b>FM Interface</b>							
AE5	FM_RXP	-	A	I	3.2	FM RX+	-
AE4	FM_RXM	-	A	I	3.2	FM RX-	-
AE6	FM_REFP	-	A	O	3.2	FM ADC REF+	-
AE7	FM_REFN	-	A	O	3.2	FM ADC REF-	-
<b>DRAM Interface</b>							
H2	SDR_DQ[0]	-	-	-	-	DRAM Memory Data Bus	-
G2	SDR_DQ[1]	-	-	-	-	DRAM Memory Data Bus	-
F2	SDR_DQ[2]	-	-	-	-	DRAM Memory Data Bus	-
J3	SDR_DQ[3]	-	-	-	-	DRAM Memory Data Bus	-
F1	SDR_DQ[4]	-	-	-	-	DRAM Memory Data Bus	-
D2	SDR_DQ[5]	-	-	-	-	DRAM Memory Data Bus	-
G3	SDR_DQ[6]	-	-	-	-	DRAM Memory Data Bus	-
E2	SDR_DQ[7]	-	-	-	-	DRAM Memory Data Bus	-
H6	SDR_DQ[8]	-	-	-	-	DRAM Memory Data Bus	-
F6	SDR_DQ[9]	-	-	-	-	DRAM Memory Data Bus	-
H5	SDR_DQ[10]	-	-	-	-	DRAM Memory Data Bus	-
G5	SDR_DQ[11]	-	-	-	-	DRAM Memory Data Bus	-
G6	SDR_DQ[12]	-	-	-	-	DRAM Memory Data Bus	-
J5	SDR_DQ[13]	-	-	-	-	DRAM Memory Data Bus	-
F5	SDR_DQ[14]	-	-	-	-	DRAM Memory Data Bus	-
E5	SDR_DQ[15]	-	-	-	-	DRAM Memory Data Bus	-
R2	SDR_A[0]	-	-	-	-	DRAM Memory Address	-
R1	SDR_A[1]	-	-	-	-	DRAM Memory Address	-
L5	SDR_A[2]	-	-	-	-	DRAM Memory Address	-
M6	SDR_A[3]	-	-	-	-	DRAM Memory Address	-
L2	SDR_A[4]	-	-	-	-	DRAM Memory Address	-
K5	SDR_A[5]	-	-	-	-	DRAM Memory Address	-
K6	SDR_A[6]	-	-	-	-	DRAM Memory Address	-
R5	SDR_A[7]	-	-	-	-	DRAM Memory Address	-
R6	SDR_A[8]	-	-	-	-	DRAM Memory Address	-
L8	SDR_A[9]	-	-	-	-	DRAM Memory Address	-



Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
K3	SDR_A[10]	-	-	-	-	DRAM Memory Address	-
M5	SDR_A[11]	-	-	-	-	DRAM Memory Address	-
P5	SDR_A[12]	-	-	-	-	DRAM Memory Address	-
N3	SDR_BA[0]	-	-	-	-	DRAM Memory Bank Address	-
P3	SDR_BA[1]	-	-	-	-	DRAM Memory Bank Address	-
L1	SDR_DQM[0]	-	-	-	-	Data Mask for Low Byte; active high	-
J6	SDR_DQM[1]	-	-	-	-	Data Mask for Low Byte; active high	-
P2	SDR_MCLK	-	-	-	-	DRAM Memory Clock	-
P6	SDR_CKE	-	-	-	-	DRAM Memory Clock Enable	-
M8	SDR_CSZ	-	-	-	-	Chip Select; active low	-
N5	SDR_WEZ	-	-	-	-	Write Enable; active low	-
N6	SDR_CASZ	-	-	-	-	Column Address Strobe; active low	-
N8	SDR_RASZ	-	-	-	-	Row Address Strobe; active low	-
<b>NAND Flash Interface</b>							
B6	F_CLE	CUD	D	O	VDD_MNAND	NAND Flash Command Latch Enable	I/L
B7	F_CEN	CUD	D	O	VDD_MNAND	NAND Flash Chip Enable (active low)	I/H
D3	F_ALE	CUD	D	O	VDD_MNAND	NAND Flash Address Latch Enable	I/L
E6	F_RDZ	CUD	D	O	VDD_MNAND	NAND Flash Read Enable (active low)	I/H
A6	F_WRZ	CUD	D	O	VDD_MNAND	NAND Flash Write Enable (active low)	I/H
F7	F_RBN	CUD	D	O	VDD_MNAND	NAND Flash Ready (Busy)	I/H
J8	F_WPT	CUD	D	O	VDD_MNAND	NAND Flash Write Protect (active low)	I/H

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
C7	F_CEN1	CUD	D	O	VDD_MNAND	NAND Flash Chip Enable (active low)	I/H
A5	F_DA0	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [0]	I/L
B5	F_DA1	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [1]	I/L
B4	F_DA2	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [2]	I/L
C4	F_DA3	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [3]	I/HiZ
A3	F_DA4	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [4]	I/L
B3	F_DA5	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [5]	I/L
A2	F_DA6	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [6]	I/L
B2	F_DA7	CUD	D	I/O	VDD_MNAND	NAND Flash Data Bus Bit [7]	I/L
<b>Ground</b>							
C2	GND_APLL	-	A	G	0	DDR APLL Ground	-
AC2	GND_USB	-	A	G	0	USB PHY Ground	-
AB5	GNDLNA_FM	-	A	G	0	FM LNA Ground	-
AB6	GND_FM	-	A	G	0	FM General Ground	-
W9	GNDPLL_FM	-	A	G	0	FM ADC, LO Ground	-
P12	GNDGSUB_FM	-	A	G	0	FM Substrate Ground	-
R14	GNDRTC	-	A	G	0	32KHz XO Ground	-
P14	GND_AUX	-	A	G	0	Auxiliary ADC Ground	-
R12	GND_AUDRV	-	A	G	0	ABB Audio Driver Ground	-
R13	GND_AUDA	-	A	G	0	ABB Audio Analog Ground	-
N13	GND_AUDD	-	A	G	0	ABB Audio Codec Ground	-
AE15	GND_RF_A	-	A	G	0	ABB RF Analog Ground	-
P15	GND_RF_D	-	A	G	0	ABB RF Codec Ground	-
N14 AF19	GND_A	-	A	G	0	ABB Analog Ground	-

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
R15	GND1	-	A	G	0	ABB Digital General Ground	-
M13 N12 N15 P13 AC3 AD2 AF3	GND1	-	A	G	0	Digital Core Ground	-
K10 K13 P25	GNDIO	-	A	G	0	Digital I/O Ground	-
AA25	GNDRF	-	A	G	0	RF1/RF2 LDO Ground	-
AA21	GNDAMP	-	A	G	0	Class D AMP Ground	-
AD25	GNDBST	-	A	G	0	Boost Ground	-
Y22	GNDBK1	-	A	G	0	Digital BUCK Ground	-
AE25	GNDBK2	-	A	G	0	MI BUCK Ground	-
D1 H1 J2 M1	GND_SDR	-	D	G	0	DRAM Ground	-
<b>Power</b>							
M12 M14 U13	VDDC	-	A	P	1.2	Digital Core Supply	-
B1	VDD_APLL	-	A	P	3.2	DDR APLL Supply	-
AA1	VDD_USB	-	A	P	3.2	USB Transceiver Supply	-
AD4	VDD_FM	-	A	P	3.2	FM RF Supply	-
AF6	VDDPLL_FM	-	A	P	3.2	FM LO Supply	-
AD7	VDDADC_FM	-	A	P	2.5	FM ADC Supply	-
AF5	VLNACAP_FM	-	A	P	2.5	FM LNA LDO Output	-
AD10	VDDAUD	-	A	P	3.2	Audio Driver Supply	-
AE10	VABBAUD	-	A	P	2.5	ABB Audio LDO Output	-
AF12	VRTCCAP	-	A	P	2.5	RTC Supply	-
AB13	VAUXLDO	-	A	P	2.5	AUX LDO Output	-
AD14	VABBRF	-	A	P	2.5	ABB RF LDO Output	-

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
AA20	VDD1	-	A	P	3.2	ABB General Supply 1	-
AA19	VDD2	-	A	P	3.2	ABB General Supply 2	-
L26	VDD3	-	A	P	3.2	ABB General Supply 3	-
U22	VA	-	A	P	1.8	Analog LDO Output	-
U24	VSIM1	-	A	P	1.8	SIM LDO Output	-
W22	VSIM2	-	A	P	2.9	SIM2 LDO Output	-
R25	VIO1	-	A	P	2.8	DBB IO LDO Output	-
T22	VIO2	-	A	P	2.8	MMP LCD LDO Output	-
W21	VDIGRF	-	A	P	2.8	DIGRF LDO Output	-
V22	VDIG	-	A	P	1.2	ABB Digital LDO Output	-
R22	VPER1	-	A	P	2.5	Peripheral LDO1 Output	-
P24	VPER2	-	A	P	2.8	Peripheral LDO2 Output	-
N25	VPER3	-	A	P	1.8	Peripheral LDO3 Output	-
N24	VPER4	-	A	P	2.8	Peripheral LDO4 Output	-
R19	VDDPEXT1	-	A	P	3.2	Peripheral LDO Supply 1	-
AE20	VDDPEXT2	-	A	P	3.2	Peripheral LDO Supply 2	-
AC24	VRF1	-	A	P	2.8	VRF1 LDO Output	-
AB25	VRF2	-	A	P	2.8	VRF2 LDO Output	-
AE19	VBATT_AVDD	-	A	P	4.2	Battery Source	-
AE23	VBATT_BK	-	A	P	4.2	Buck Supply	-
AD21 AD22	VBATT_ABB	-	A	P	4.2	ABB LDO Supply	-
AE22	VBATT_BST	-	A	P	4.2	Boost Supply	-
AC25	VBSTFB	-	A	p	4.2	Boost Feedback Voltage	-
AD26	VBATT_RF	-	A	P	4.2	VRF LDO Supply	-
AB19	VBATT_AMP	-	A	P	4.2	Class D AMP Supply	-
AA22	VINUSB	-	A	P	4.2	USB LDO Supply	-
AE21	VUSB	-	A	P	3.2	USB LDO Supply	-
AF21	VABB1	-	A	P	3.2	ABB1 LDO Supply Output	-
AF22	VABB2	-	A	P	3.2	ABB2 LDO Supply Output	-
AD23	VSTDLDO2	-	A	P	1.8	Standby LDO Output	-
Y25	VBKOUT1	-	A	P	1.2	Buck 1 Output	-
AF24	VBKOUT2	-	A	P	1.8	Buck 2 Output	-

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
AA24	VBUSIN	-	A	P	4.2	Boost Supply 2	-
AE17	VCS	-	A	P	5	Charger Supply	-
V5	VDD_GPIO_A1	-	A	P	1.8/2.8	Digital I/O Supply	-
A12	VDD_GPIO_A2	-	A	P	1.8/2.8	Digital I/O Supply	-
H18	VDD_GPIO_B	-	A	P	1.8/2.8	Digital I/O Supply	-
H10	VDD_GPIO_C	-	A	P	1.8/2.8	Digital I/O Supply	-
W2	VDD_USIM1	-	A	P	1.8/2.8	Digital I/O Supply	-
AA6	VDD_USIM2	-	A	P	1.8/2.8	Digital I/O Supply	-
L10	VDD_MSD	-	A	P	1.8/2.8	Digital I/O Supply	-
N19	VDD_MSR	-	A	P	1.8/2.8	Digital I/O Supply	-
G21	VDD_MLCD	-	A	P	1.8/2.8	Digital I/O Supply	-
H17	VDD_BJTAG	-	A	P	1.8/2.8	Digital I/O Supply	-
H15	VDD_MPIF1	-	D	P	1.8/2.8	Digital I/O Supply	-
E10	VDD_MPIF2	-	D	P	1.8/2.8	Digital I/O Supply	-
F15	VDD_SDIO	-	D	P	1.8/2.8	Digital I/O Supply	-
H8	VDD_MNAND	-	D	P	1.8/2.8	Digital I/O Supply	-
C1 J1 M2	VDD_SDR	-	D	P	1.8	DRAM I/O Supply	-
<b>Power Management</b>							
AB7	ONOFF	-	D	I	3.2	Power On/Off	-
AA8	PMU_PWREN	-	D	I/O	3.2	Power Enable Signal	-
L25	PMU_BATON	-	D	I/O	3.2	Battery Level Detection	-
AB22	PMU_INT	-	D	I/O	3.2	Power Unit Interrupt	-
M26	PMU_CLK	-	D	I/O	3.2	Power Unit Clock	-
K24	PMU_SCLK	PU	D	I	3.2	Power Unit I2C Clock	-
P19	PMU_SDIO	PU	D	I	3.2	Power Unit I2C I/O	-
W26	PMU_CHGDET	-	D	I/O	3.2	Charger Detection	-
W25	PMU_BKEN	-	D	I	3.2	Buck Enable	-
Y24	PMU_BKSW1	-	A	O	4.2	Buck1 Switching Node	-
AF25	PMU_BKSW2	-	A	O	4.2	Buck2 Switching Node	-
AE26	PMU_BSTGATE	-	A	O	4.2	Boost External MOS Gate Driving	-

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
AE24	PMU_BSTSW	-	A	O	5	Boost Switching Node	-
AD17	VADAIN	-	A	O	4.2	Adaptor Divided Voltage	-
AE16	VGATEDRV	-	A	O	5	Charger External MOS Gate Driving	-
AB26	VBST_ISENSE	-	A	O	4.2	Boost Current Sense Node	-
AE18	VCHG_ISENSE	-	A	O	4.2	Charger Current Sense Node	-
AC21	PMU_BSTEN	-	D	I	3.2	Boost Enable	-
AA26	PMU_OVPEXT	-	D	I	3.2	Boost Over Voltage Protection Enable	-
<b>JTAG Port</b>							
AA17	JTAG_NTRST	-	D	I	VDD_BJTAG	JTAG Reset	I/H
U14	JTAG_TCK	-	D	I	VDD_BJTAG	JTAG Clock	I/H
W17	JTAG_TMS	-	D	I	VDD_BJTAG	JTAG Mode	I/L
W16	JTAG_TDI	-	D	I	VDD_BJTAG	JTAG Input	I/H
W15	JTAG_TDO	-	D	O	VDD_BJTAG	JTAG Output	I/H
M15	MCP_HIZ	-	D	I	VDD_BJTAG	Put all pads in High Impedance state, for multi-chip-package testing	I/L
W18	RTCK	-	D	O	VDD_BJTAG	ARM9 Core JTAG Return Clock (for Software Debugger)	I/HiZ
<b>Miscellaneous</b>							
AF18	VREFEXT	-	A	I/O	3.2	Power Unit Reference Voltage	-
Y21	VREFSYS	-	A	O	3.2	System Reference Voltage	-
V21	MAIN_MCLK	-	A	I	3.2	MPLL Input	-
AB16	RLEDOD	-	A	O	5	Red LED Driver	-
AA16	GLEDOD	-	A	O	5	Green LED Driver	-
AA15	BLEDOD	-	A	O	5	Blue LED Driver	-
AB15	KEYPAD1	-	A	O	5	Keypad LED Driver 1	-
W14	KEYPAD2	-	A	O	5	Keypad LED Driver 2	-
<b>Test Pin</b>							
N22	I2CLK	-	D	I/O	3.2	I <sup>2</sup> C Clock	I/HiZ

Ball #	Pin Name	CU/CD/ PU/PD/ CUD/ None	Analog/ Digital/ Power/ Ground	I/O	Voltages (V)	Description	Reset
P21	I2CDATA	-	D	I/O	3.2	I <sup>2</sup> C Data	I/HiZ
AB9	PMTEST	-	D	I	3.2	PM Test Mode	I/L
M25	ABB_TEST	-	D	I	3.2	ABB Test Mode	I/L
AB8	ABBRESETB	-	D	I	3.2	ABB Reset B	I/H
U21	MPLL_BYPASS	-	D	I	3.2	MPLL Bypass Enable	I/L
P22	MCLKSEL	-	D	I	3.2	Master Clock Selection	I/HiZ
AF26	PMU_DFTMD	-	D	I	3.2	Power Unit Digital Test Mode	-
W8	FM_TST1	-	A	O	3.2	FM Test Pad 1	-
AA7	FM_TST2	-	A	O	3.2	FM Test Pad 2	-
<b>No Connection</b>							
T10	NC	-	-	-	-	-	-
AD1							
AE1							
AE2							
AE3							
AF1							
AF2							

**Notes:****1. Abbreviations used in column CU/CD/PU/PD/CUD/None:**

CU	Configurable Pull-Up and Hi-Z
CD	Configurable Pull-Dow and Hi-Z
PU	Permanent Pull-Up
PD	Permanent Pull-Down
CUD	Configurable Pull-Up, Pull-Down and Hi-Z
-	None

**2. Abbreviations used in column Analog/Digital/Power/Ground:**

A	Analog
D	Digital
P	Power Pin
G	Ground

**3. Abbreviations used in column I/O:**

I	Input
O	Output
I/O	Input/Output

**4. Abbreviations used in column Reset:**

O/L	Output Low
O/H	Output High
I/L	Input Low
I/H	Input High
I/HiZ	Input High Impedance
-	None



## 7. ELECTRICAL SPECIFICATIONS

### 7.1. Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Operating Battery Supply Voltages	$V_{vbat}$			4.2	V
Operating Charger Supply Voltages	$V_{chg}$			5.5	V
LED Input Voltage	$V_{LED}$			$V_{vbat}$	V
Voltages on "MCLK" Pin	$V_{MCLK}$			3.2	V
Voltages on RFIC Control Pins	$V_{RFIC}$			3.2	V
Voltage on digital IO under 2.8V power supply	$V_{dig2p8}$			3.1	V
Voltage on digital IO under 1.8V power supply	$V_{dig1p8}$			2.1	V
Voltages on LDO Output Pins	$V_{LDO}$			3.1	V
Voltage on HVLDO output pins	$V_{HVLDO}$			3.3	V
Voltages on LVLDO Output Pins	$V_{LVLDO}$			1.31	V
Voltages on other Analog Pins	$V_{analog}$			3.2	V
Ambient Operating Temperature	$T_A$	-25		85	°C
Storage Temperature	$T_{STG}$	-40		150	°C
Junction Temperature	$T_J$			125	°C
Thermal Resistance (Junction to Air) Natural Convection	$\theta_{JA}$		45		°C/W

**Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.**

## 8. ORDERING GUIDE

Table 3: Ordering Guide

Part Number	Temperature Range	Package Description	Package Option
MSW8535N-LF	-25 °C to +85°C	LFBGA	411-ball

## 9. MARKING INFORMATION

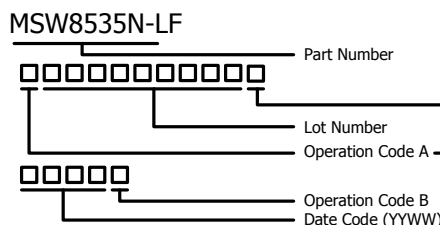


Figure 3: Package Marking

## 10. DISCLAIMER

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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MSW8535N comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

## 11. REVISION HISTORY

Document	Description	Date
MSW8535N_pb_v01	• Initial release	Oct 2009

## 12. MECHANICAL DIMENSIONS

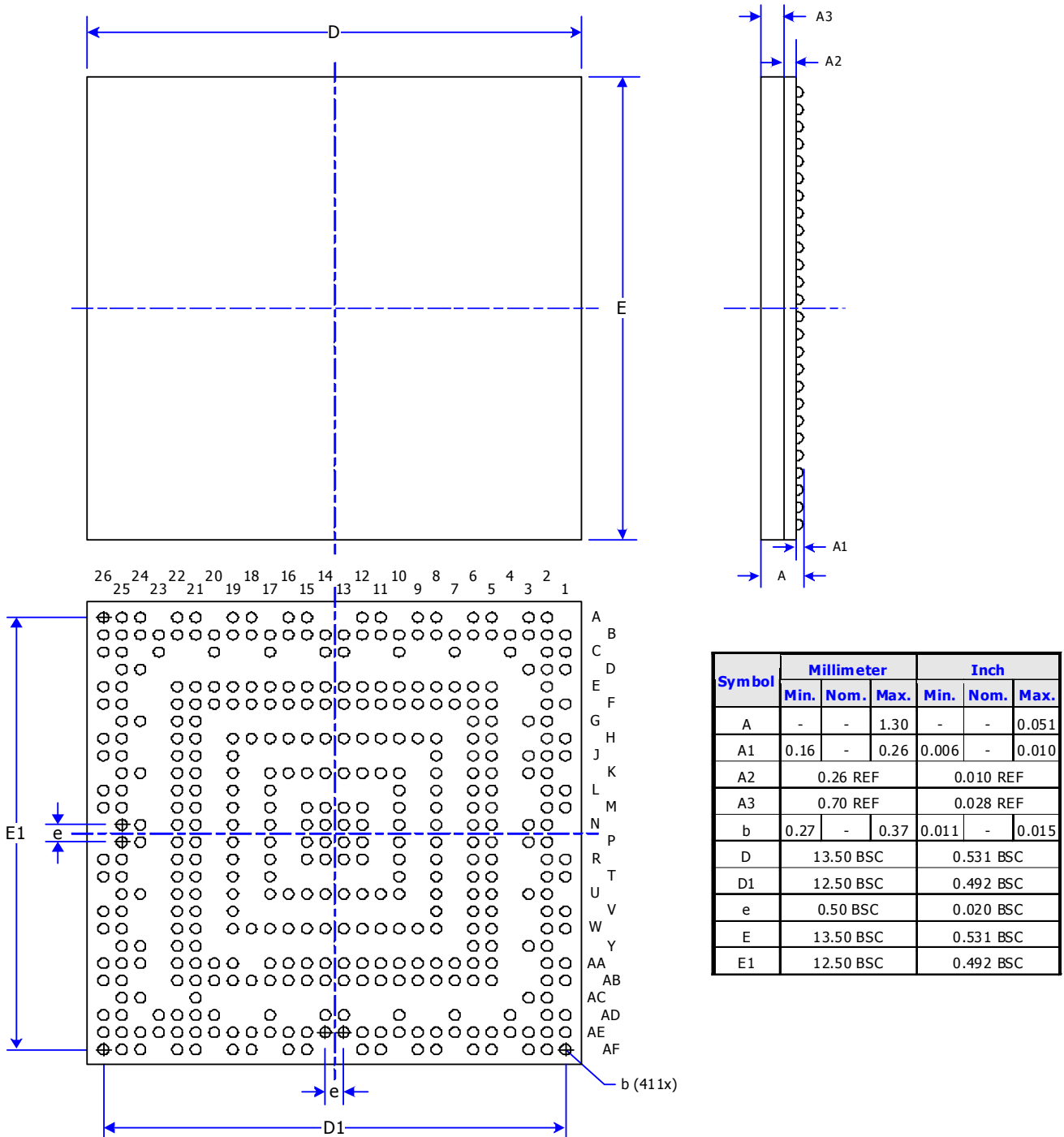


Figure 4: Mechanical Dimensions