AIT8328(13mm X 13mm BGA, 277-pins)

Hardware Application Note

Rev. 0.1

1. Revision History

Release	Date	Modification
R0.1	2014/08/27	Initial Release

AIT CONFIDENTIAL

NO DISCLOSURE

2. AIT8328 system connection reference

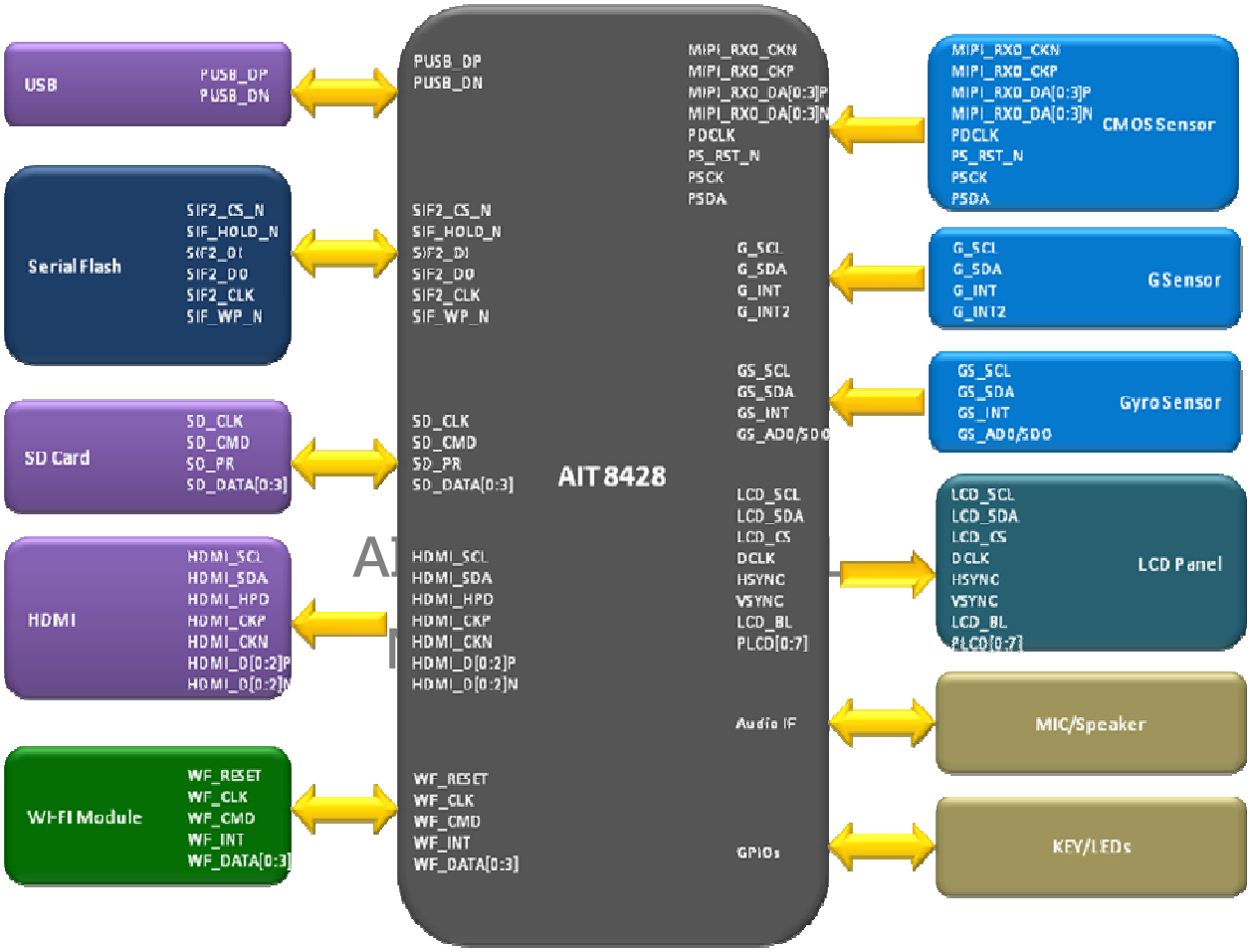


Figure.1 AIT8328 system connection reference

3. Power pin

- Main chip part description:

Pin Name	Pin Description
VDD_CORE	Core power (19 pins)
VDD_CLK	IO PAD power for Clock
VDD_SEN	IO PAD power for SENSOR
VDD_I2S	IO PAD power for I2S
VDD_LCD	IO PAD power for LCD
VDD_AGPIO	IO PAD power for GPIO groupA
VDD_BGPIO	IO PAD power for GPIO groupB
VDD_CGPIO	IO PAD power for GPIO groupC
VDD_DGPIO	IO PAD power for GPIO groupD
VDD_DRAM	IO PAD power for DRAM
VDD_DDR	DDR3 chip power
VDD_DRAM_CORE	DRAM core power
VDD_USB_1V1	USB 1.1V power
VDD_USB_3V3	USB 3.3V power
VSS_USB	USB ground
AVDD_PLL	DPLL power
AVSS_PLL	DPLL ground
AVDD_MIPI_RX0	MIPI_RX0 power
AVDD_MIPI_RX1	MIPI_RX1 power
AVDD_AUDIO	Audio power
AVSS_AUDIO	Audio ground
AVDD_TV	Video DAC power
AVSS_TV	Video DAC ground
VDD11_TMDS	HDMI transmitter 1.1V power
VDD33_TMDS	HDMI transmitter 3.3V power
VDD33_HDMI	HDMI analog 3.3V power
VSS_TMDS	HDMI transmitter ground
VDD_RTC	RTC power
VSS_RTC	RTC ground
VDD_POR_1V8	POR detect 1.8V input power
VDD_SADC	SAR ADC power
VSS	Common ground

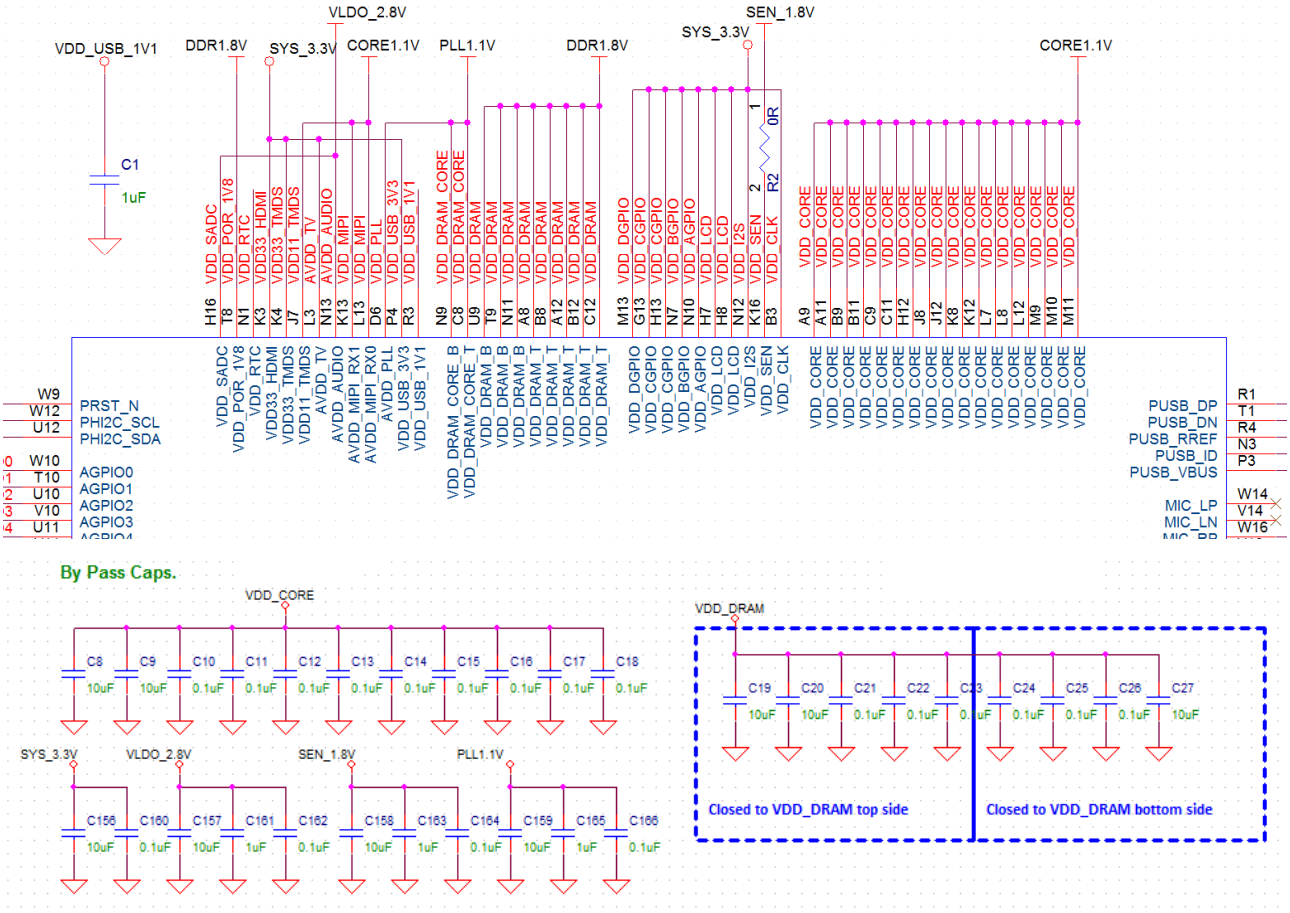


Figure.2 Reference circuit for power module

Note:

1. The 0 ohm resistor added on the power path was designed to measure the current and power consumption. Please reserve those resisters for software/hardware engineer to easy debug the power consumption.
2. Reserve option: can add an independent LDO on AVDD_AUDIO (VLDO_2.8V) for better audio noise immunity.

3.1. Power on sequence

Symbol	Parameter	Min	Max	Unit
t_{PUD}	Core power up to IO power up delay	100	-	ns
t_{RUD}	IO power on to reset assert delay	1	-	ms
t_{POD}	IO power off to Core power off delay	100	-	ns
t_{ROD}	Reset de-assert to IO power delay	0	-	ns
t_{CKRST}	Clock on to reset assert delay	8T	-	T=42ns(24MHz)

Table 1. Power On/Off Timing Characteristics

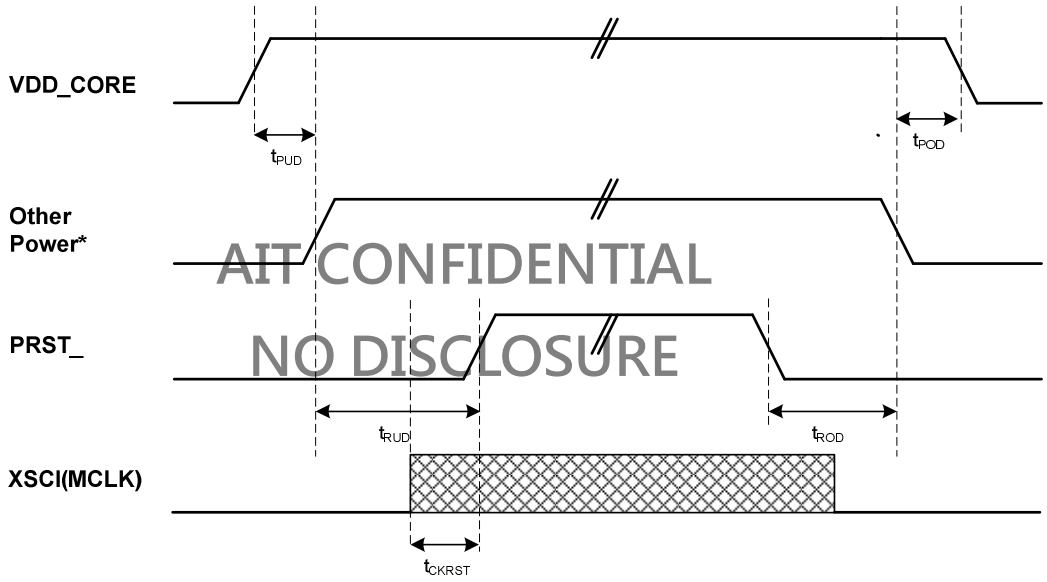


Figure 1. Power On/Off Timing Diagram

SIF interface

Pin Name	Pin Description	Reset State
SIF_CLK	SIF_CLK	LZ
SIF_CS#	SIF_CS#	HZ
SIF_DO	SIF_DO	LZ
SIF_DI	SIF_DI	LZ

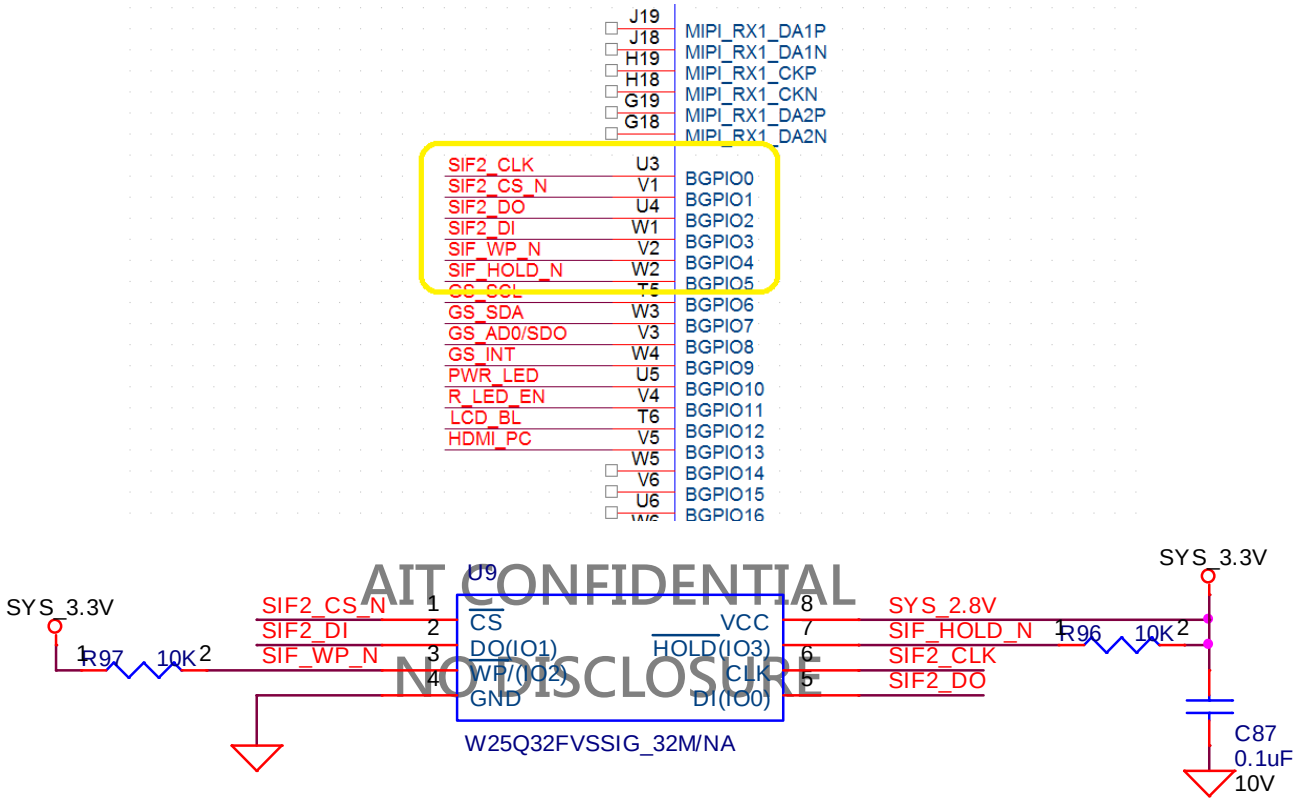


Figure.4 System boot circuit

4. Sensor interface

5.1 Parallel Sensor Interface

Pin Name	Function PAD	Description	Reset State
PS_RST_N	PS_RST_N	Sensor reset	LZ
PDCLK	PDCLK	Sensor clock	LZ
PSCK	PSCK	Sensor serial interface clock. Need to pull high if the sensor request.	HZ
PSDA	PSDA	Sensor serial interface data. Need to pull high if the sensor request.	HZ
PSEN	PSEN	Sensor enable	LZ
PIXCLK	PPXL_CLK	Sensor pixel clock	LZ
PVSYNC	PVSYNC	Sensor VSYNC	LZ
PHSYNC	PHSYNC	Sensor HSYNC	LZ
MIPI_RX0_DA3N	PSNR_D6	Sensor raw data [0]	LZ
MIPI_RX0_DA3P	PSNR_D7	Sensor raw data [1]	LZ
MIPI_RX0_DA2N	PSNR_D8	Sensor raw data [2]	LZ
MIPI_RX0_DA2P	PSNR_D9	Sensor raw data [3]	LZ
MIPI_RX0_CKN	PSNR_D10	Sensor raw data [4]	LZ
MIPI_RX0_CKP	PSNR_D11	Sensor raw data [5]	LZ
MIPI_RX0_DA1N	PSNR_D12	Sensor raw data [6]	LZ
MIPI_RX0_DA1P	PSNR_D13	Sensor raw data [7]	LZ
MIPI_RX0_DA0N	PSNR_D14	Sensor raw data [8]	LZ
MIPI_RX0_DA0P	PSNR_D15	Sensor raw data [9]	LZ

How to setting the sensor standby mode?

[1] Setting the sensor standby pin with AIT8328 GPIO pin with power supply still applied on sensor. The AIT8328 sensor interface pin need to set to the same state as sensor standby mode..

[2] Turns off the sensor power supply directly. All the AIT8328 sensor control and data pins need to set to “0” when the sensor power is off.

5.2 MIPI Sensor Interface

Pin Name	Function PAD	Description	Reset State
PSCK	PSCK	Sensor serial interface clock. Need to pull high if the sensor request.	HZ
PSDA	PSDA	Sensor serial interface data. Need to pull high if the sensor request.	HZ
PS_RST_N	PS_RST_N	Sensor reset for MIPI IF RX0	LZ
PSEN	PSEN	Sensor enable for MIPI IF RX0	LZ
PDCLK	PDCLK	Sensor clock for MIPI IF RX0	LZ
MIPI_RX0_CKN	MIPI_RX0_CKN	MIPI RX0 D-PHY negative clock lane input	LZ
MIPI_RX0_CKP	MIPI_RX0_CKP	MIPI RX0 D-PHY positive clock lane input	LZ
MIPI_RX0_DA0N	MIPI_RX0_DA0N	MIPI RX0 D-PHY negative data lane0 input	LZ
MIPI_RX0_DA0P	MIPI_RX0_DA0P	MIPI RX0 D-PHY positive data lane0 input	LZ
MIPI_RX0_DA1N	MIPI_RX0_DA1N	MIPI RX0 D-PHY negative data lane1 input	LZ
MIPI_RX0_DA1P	MIPI_RX0_DA1P	MIPI RX0 D-PHY positive data lane1 input	LZ
MIPI_RX0_DA2N	MIPI_RX0_DA2N	MIPI RX0 D-PHY negative data lane2 input	LZ
MIPI_RX0_DA2P	MIPI_RX0_DA2P	MIPI RX0 D-PHY positive data lane2 input	LZ
MIPI_RX0_DA3N	MIPI_RX0_DA3N	MIPI RX0 D-PHY negative data lane3 input	LZ
MIPI_RX0_DA3P	MIPI_RX0_DA3P	MIPI RX0 D-PHY positive data lane3 input	LZ
PS_RST_N_1	PS_RST_N_1	Sensor reset for MIPI IF RX1	LZ
PSEN_1	PSEN_1	Sensor enable for MIPI IF RX1	LZ
PDCLK_1	PDCLK_1	Sensor clock for MIPI IF RX1	LZ
MIPI_RX1_CKN	MIPI_RX1_CKN	MIPI RX1 D-PHY negative clock lane input	LZ
MIPI_RX1_CKP	MIPI_RX1_CKP	MIPI RX1 D-PHY positive clock lane input	LZ
MIPI_RX1_DA1N	MIPI_RX1_DA1N	MIPI RX1 D-PHY negative data lane1 input	LZ
MIPI_RX1_DA1P	MIPI_RX1_DA1P	MIPI RX1 D-PHY positive data lane1 input	LZ
MIPI_RX1_DA2N	MIPI_RX1_DA2N	MIPI RX1 D-PHY negative data lane2 input	LZ
MIPI_RX1_DA2P	MIPI_RX1_DA2P	MIPI RX1 D-PHY positive data lane2 input	LZ

Note:
1. MIPI sensor interface is high-speed differential interface. Please be careful when implementing MIPI layout, some general layout rules are listed in PCB layout guide section.
2. PSCK, PSDA I2C pull high resistors depend on the sensor specification requirement

5. LCD interface

Pin Name	Pin Description	Reset State
PLCD0~15	LCD data bus.	LZ
PLCD_WE#	LCD write enable.	HZ
PLCD_A0	LCD command / data selection.	LZ
PLCD_RD#	LCD read enable.	HZ
PLCD1_CS#	Main LCD panel chip selection.	HZ
PLCD2_CS#	Sub LCD panel chip selection.	HZ
PLCD_FLM	LCD_FLM	LZ
PLCD_GPIO	LCD GPIO	LZ

5.1. LCD Interface – CPU Type

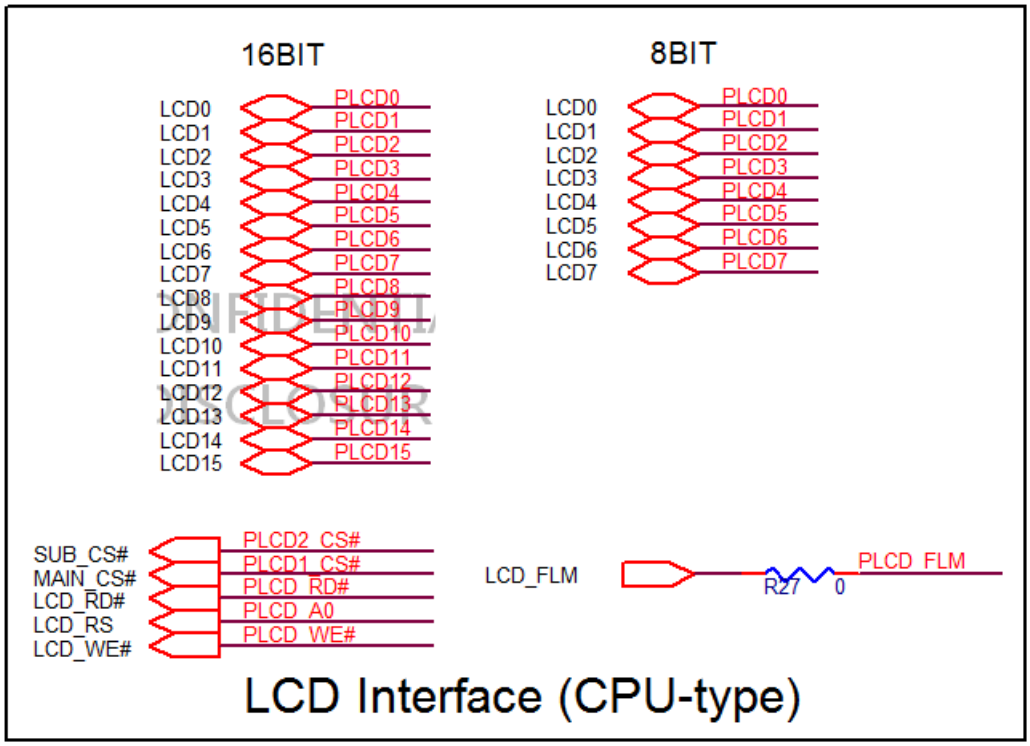


Figure.6-1 Reference circuit for LCD interface (CPU-type)

5.2. LCD Interface – RGB Type

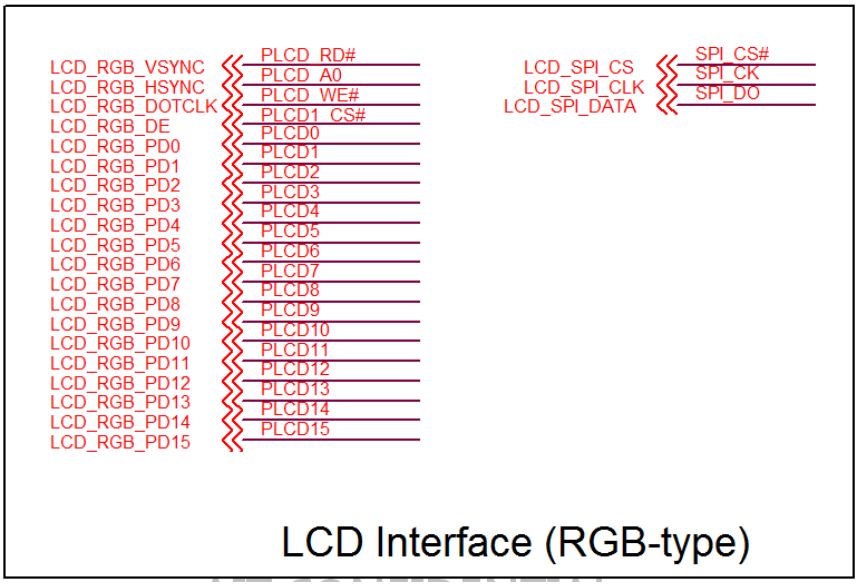


Figure.6-2 Reference circuit for LCD interface (RGB-type support up to 16-bit)

5.3. LCD Interface – As CCIR Output to Baseband Camera Input

AIT LCD Interface can be programmed as CCIR output to baseband camera input as following figure. By this configuration, it can be simply functioned as a video/camera co-processor of baseband.

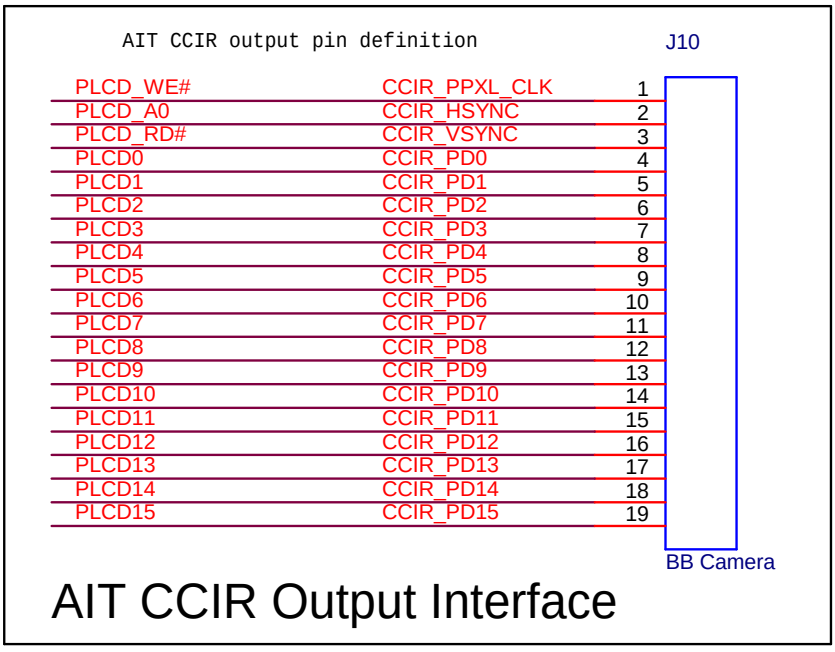


Figure.6-3 Reference circuit for parallel sensor interface

6. GPIO pinNote:

Pin Name	Pin Description			Reset State
AGPIO0	AGPIO0	UART0_TX_0		LZ
AGPIO1	AGPIO1	PWM0		LZ
AGPIO2	AGPIO2	PWM1_0		LZ
AGPIO3	AGPIO3	PWM2_0		LZ
AGPIO4	AGPIO4	PWM3_0		LZ
AGPIO5	AGPIO5			LZ
AGPIO6	AGPIO6	UART0_RX_0		HZ
AGPIO7	AGPIO7			LZ

Pin Name	Pin Description			Reset State
BGPIO0	BGPIO0			LZ
BGPIO1	BGPIO1			LZ
BGPIO2	BGPIO2			LZ
BGPIO3	BGPIO3			LZ
BGPIO4	BGPIO4	UART1_TX_1		LZ
BGPIO5	BGPIO5	UART1_RX_1		LZ
BGPIO6	BGPIO6	I2CM3_SCK_3	PWM4_0	LZ
BGPIO7	BGPIO7	I2CM3_SDA_3	PWM5_0	LZ
BGPIO8	BGPIO8	PWM6_0		LZ
BGPIO9	BGPIO9	PWM7_0		LZ
BGPIO10	BGPIO10	UART2_TX_2	PWM8_0	LZ
BGPIO11	BGPIO11	UART2_RX_2	PWM9_0	LZ
BGPIO12	BGPIO12	SD1 DAT4_1	UART1_TX_2	LZ
BGPIO13	BGPIO13	SD1 DAT5_1	UART1_RX_2	LZ
BGPIO14	BGPIO14	SD1 DAT6_1	I2CM1_SCK_3	LZ
BGPIO15	BGPIO15	SD1 DAT7_1	I2CM1_SDA_3	LZ
BGPIO16	BGPIO16	SD1 CLK_1		LZ
BGPIO17	BGPIO17	SD1 CMD_1		LZ
BGPIO18	BGPIO18	SD1 DAT0_1		LZ
BGPIO19	BGPIO19	SD1 DAT1_1		LZ
BGPIO20	BGPIO20	SD1 DAT2_1		LZ
BGPIO21	BGPIO21	SD1 DAT3_1		LZ

Pin Name	Pin Description			Reset State
CGPIO0	CGPIO0	SD0 CLK_0		LZ
CGPIO1	CGPIO1	SD0 CMD_0		LZ
CGPIO2	CGPIO2	SD0 DAT0_0		LZ
CGPIO3	CGPIO3	SD0 DAT1_0		LZ
CGPIO4	CGPIO4	SD0 DAT2_0		LZ
CGPIO5	CGPIO5	SD0 DAT3_0		LZ
CGPIO6	CGPIO6	SD1 CLK_0		LZ
CGPIO7	CGPIO7	SD1 CMD_0	I2CM1_SCK_0	LZ
CGPIO8	CGPIO8	SD1 DAT0_0		LZ
CGPIO9	CGPIO9	SD1 DAT1_0	I2CM1_SDA_0	LZ
CGPIO10	CGPIO10	SD1 DAT2_0	UART1_TX_3	LZ
CGPIO11	CGPIO11	SD1 DAT3_0	UART1_RX_3	LZ
CGPIO12	CGPIO12	SD2 CLK_0	PWM4_1	LZ
CGPIO13	CGPIO13	SD2 CMD_0	PWM5_1	LZ

CGPIO14	CGPIO14	SD2 DAT0_0	PWM6_1	LZ
CGPIO15	CGPIO15	SD2 DAT1_0	PWM7_1	LZ
CGPIO16	CGPIO16	SD2 DAT2_0	PWM8_1	LZ
CGPIO17	CGPIO17	SD2 DAT3_0	PWM9_1	LZ
CGPIO18	CGPIO18	I2CM1_SCK_2		LZ
CGPIO19	CGPIO19	I2CM1_SDA_2		LZ
CGPIO20	CGPIO20			LZ
CGPIO21	CGPIO21			LZ
CGPIO22	CGPIO22	UART1_TX_0		LZ
CGPIO23	CGPIO23	UART1_RX_0		LZ
CGPIO24	CGPIO24	I2CM2_SCK_0		LZ
CGPIO25	CGPIO25	I2CM2_SDA_0		LZ
CGPIO26	CGPIO26	UART2_TX_0	UART3_CTS_0	LZ
CGPIO27	CGPIO27	UART2_RX_0	UART3_RTS_0	LZ
CGPIO28	CGPIO28	UART3_TX_0		LZ
CGPIO29	CGPIO29	UART3_RX_0		LZ

Pin Name	Pin Description		Reset State
DGPIO0	DGPIO0	ARM_TCK_1	LZ
DGPIO1	DGPIO1	ARM_TMS_1	LZ
DGPIO2	DGPIO2	ARM_TDI_1	LZ
DGPIO3	DGPIO3	ARM_TRST_1	LZ
DGPIO4	DGPIO4	ARM_TDO_1	LZ
DGPIO5	DGPIO5	ARM_RTCK_1	LZ

Note:

1. After reset, the default state of some GPIO pin is weakly pull-high and some weakly pull-down. Be careful that the circuit controlled by GPIO pins may be triggered if it is in corresponding active state. (For example: Flash light.)
2. Please add a test point on UART_TX for AIT8328 UART debug print function.
3. Please add test points on BGPIO10~15 for ARM EJTAG Debug Interface.
4. There are four GPIO power domains –AGPIO, BGPIO, CGPIO and CGPIO. It allow flexible GPIO power group design.

6.1. SD Interface

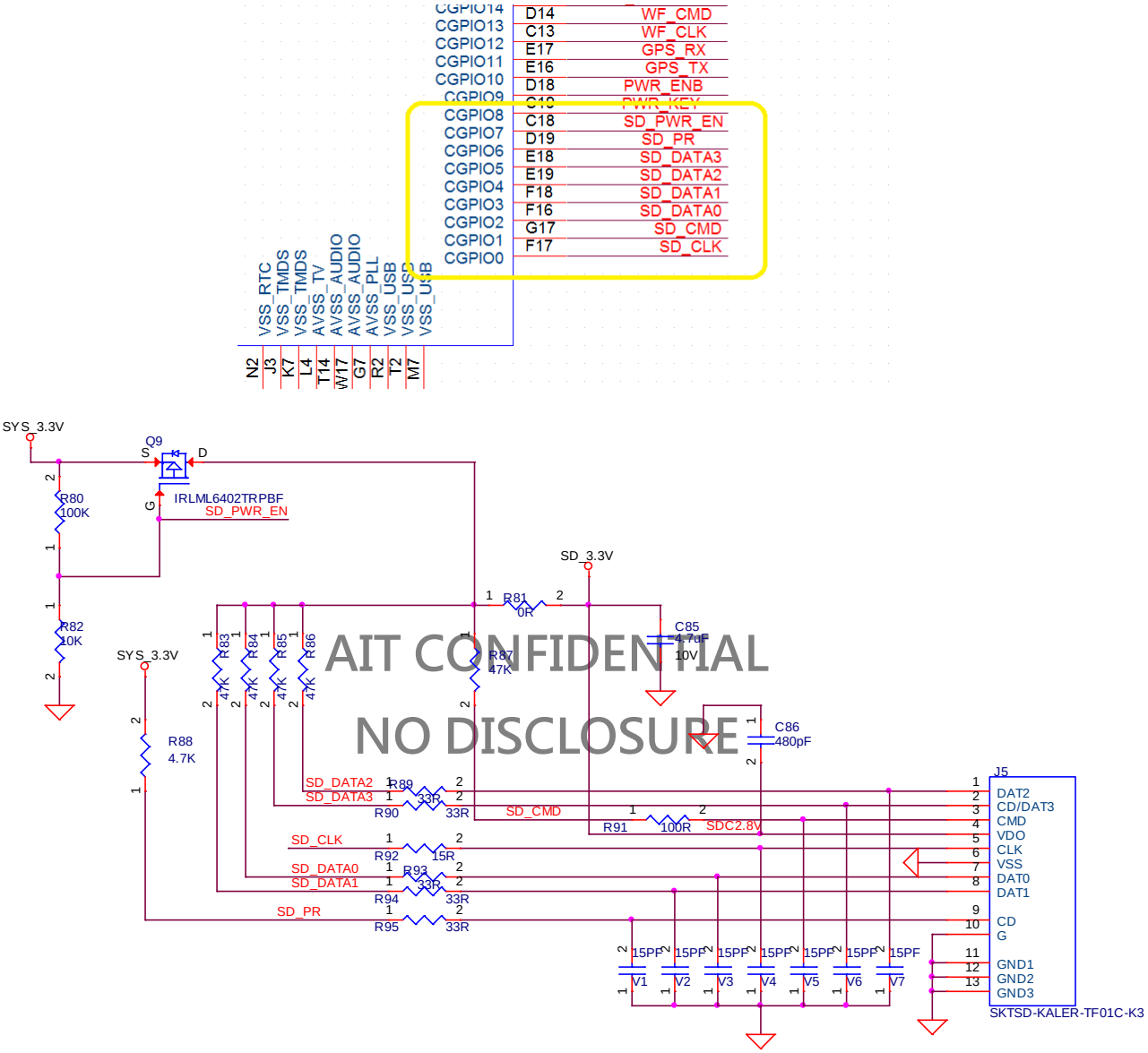


Figure.8 Reference circuit for SD card interface

Note:

1. Because the SD pin power group is same as the VDD_CGPIO . The power of the SD must be also same as the VDD_CGPIO to prevent power consumption current leakage.
2. SD power is recommended to be 3.3V to have best card compatibility. (T-flash card normal operation range is from 2.7V~3.6V, the tolerance margin will be too small if using 2.8V SD power.)
3. To achieve best power consumption, it is recommended to disable SD power supply when not used. shown as above figure.

4. There are Four sets of SD interface inside AIT8328 which pin-maping is shown as following table.

Pin Name	Pin Description	Reset State
BGPIO12	SD1 DAT4_1	LZ
BGPIO13	SD1 DAT5_1	LZ
BGPIO14	SD1 DAT6_1	LZ
BGPIO15	SD1 DAT7_1	LZ
BGPIO16	SD1 CLK_1	LZ
BGPIO17	SD1 CMD_1	LZ
BGPIO18	SD1 DAT0_1	LZ
BGPIO19	SD1 DAT1_1	LZ
BGPIO20	SD1 DAT2_1	LZ
BGPIO21	SD1 DAT3_1	LZ
CGPIO0	SD0 CLK_0	LZ
CGPIO1	SD0 CMD_0	LZ
CGPIO2	SD0 DAT0_0	LZ
CGPIO3	SD0 DAT1_0	LZ
CGPIO4	SD0 DAT2_0	LZ
CGPIO5	SD0 DAT3_0	LZ
CGPIO6	SD1 CLK_0	LZ
CGPIO7	SD1 CMD_0	LZ
CGPIO8	SD1 DAT0_0	LZ
CGPIO9	SD1 DAT1_0	LZ
CGPIO10	SD1 DAT2_0	LZ
CGPIO11	SD1 DAT3_0	LZ
CGPIO12	SD2 CLK_0	LZ
CGPIO13	SD2 CMD_0	LZ
CGPIO14	SD2 DAT0_0	LZ
CGPIO15	SD2 DAT1_0	LZ
CGPIO16	SD2 DAT2_0	LZ
CGPIO17	SD2 DAT3_0	LZ

7. Audio and voice interface

7.1. Analog audio and voice interface

Pin Name	Pin Description	Reset State
MIC_LP	Left differential microphone positive input	Z
MIC_LN	Left differential microphone negative input	Z
MIC_RP	Right differential microphone positive input	Z
MIC_RN	Right differential microphone negative input	Z
PAUXL	Left channel single-ended auxiliary input	Z
PAUXR	Right channel single-ended auxiliary input	Z
MICBIAS_L	Left microphone bias output	Z
MICBIAS_R	Right microphone bias output	Z
LINEOUT	Line amplifier positive output	Z
PVREF	Band-gap reference voltage output (A 10uF capacitor is recommended to connect to this pin)	Z

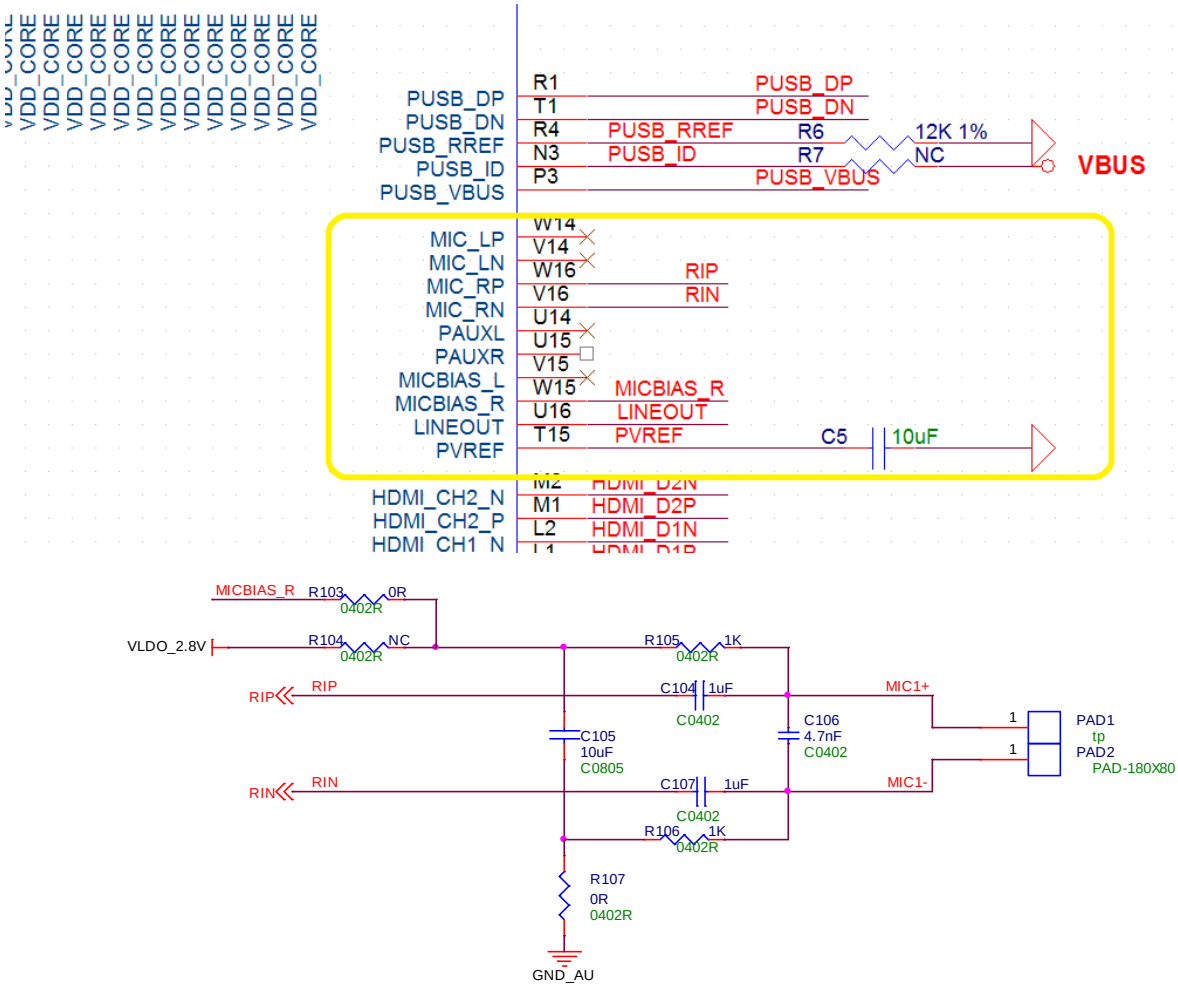


Figure.9 Reference circuit for analog audio/voice input interface

Speaker

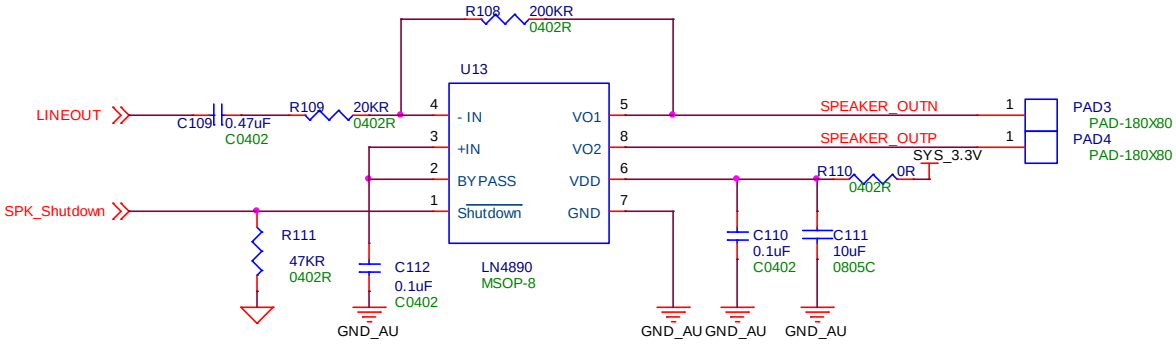


Figure.10 Reference circuit for analog audio output (Speaker) interface

Note:

1. Reserve option: Can add an independent LDO on AVDD_AUDIO (VLDO_2.8V) for better audio noise immunity.

7.2. Digital audio interface - I2S (Optional)

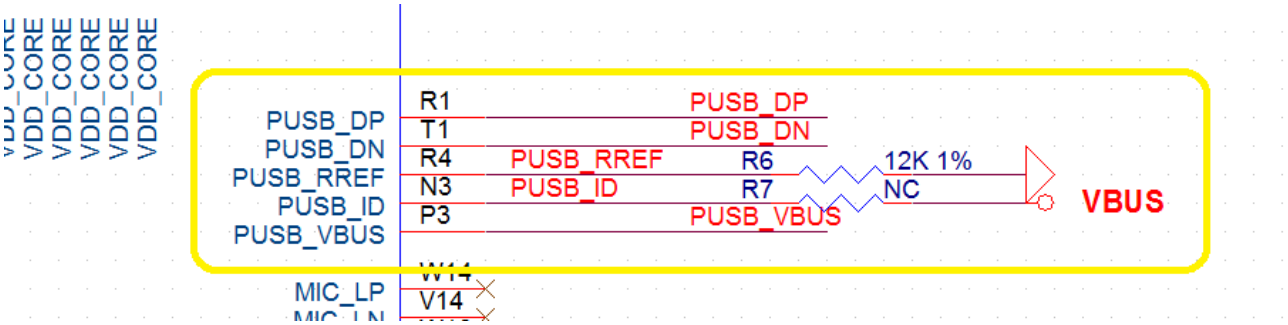
Pin Name	Pin Description	Reset State
PI2S_SCK	I2S serial clock	LZ
PI2S_WS	I2S word clock	LZ
PI2S_SDI	I2S data input	LZ
PI2S_MCLK	I2S master clock	LZ
PI2S_SDO	I2S data output	LZ

Note:

1. Except internal audio CODEC, AIT8328 also support for digital I2S interface to easily connect to other external device.

8. USB interface

Pin Name	Pin Description	Reset State
PUSB_DP	USB2.0 D+	Z
PUSB_DN	USB2.0 D-	Z
PUSB_RREF	USB PHY external reference resistor (12K ohm +/-1%)	Z
PUSB_ID	USB plug indicator	Z
PUSB_VBUS	USB bus power	Z



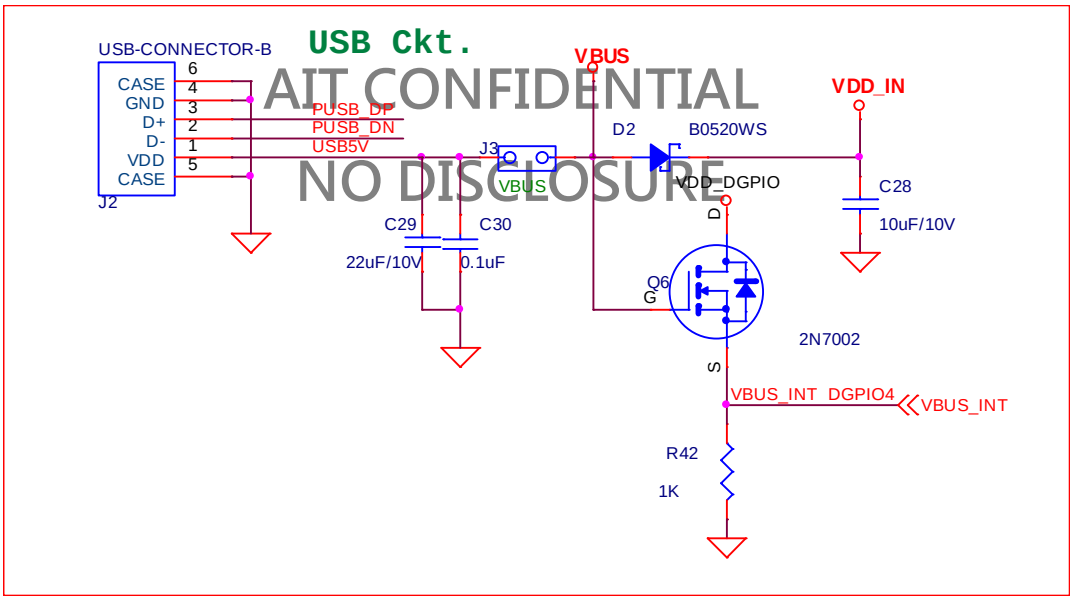


Figure.12 Reference circuit for USB interface

Note:

1.USB_RREF resistor must be precision resistor with 12K +/-1%.

2.AIT8328 can support USB2.0 HS.

9. TV-OUT interface

Pin Name	Pin Description	Reset State
TVOUTC	TV composite current out	Z
TV_FSRES	TV_FSRES out	Z

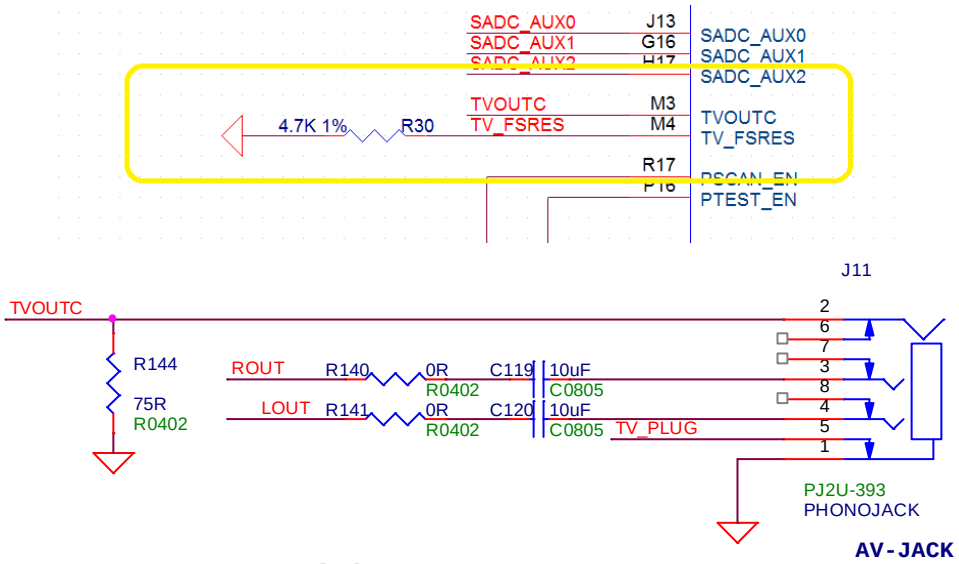


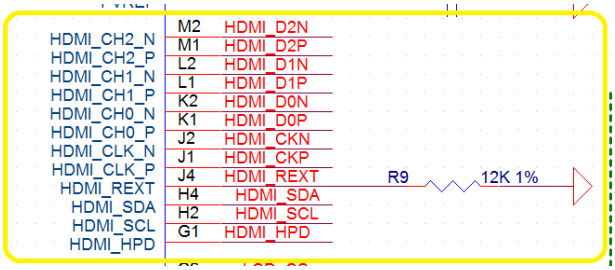
Figure.14 Reference circuit for TV-OUT interface

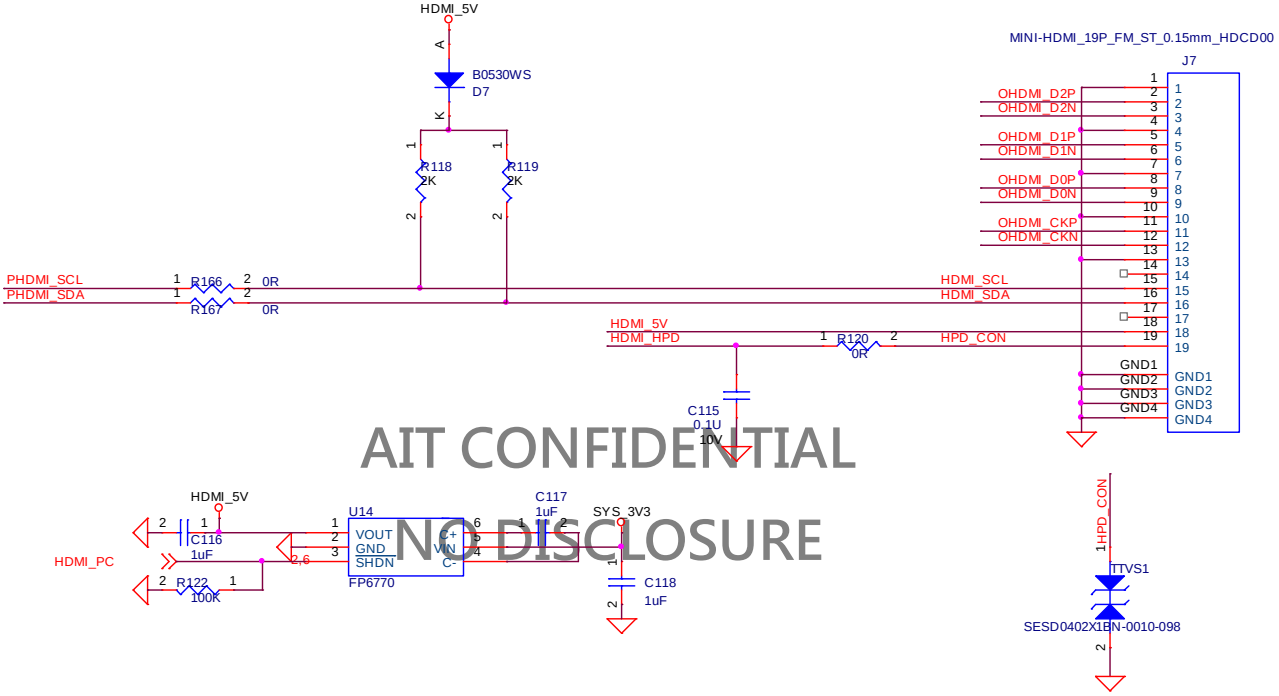
Note:

1. Need to add GPIO for cable plug-in detection(TV_PLUG).
2. Connect TV_FSRES with 4.7K-ohm to ground.
3. Please use 1% precise resistor for R33 (75-ohm) and TV_FSRES (4.7K-ohm).

10. HDMI interface

Pin Name	Pin Description	Reset State
HDMI_HPD	HDMI hot plug detect	Z
HDMI_SCL	HDMI serial interface clock	Z
HDMI_SDA	HDMI serial interface data	Z
HDMI_REXT	Connect to external 12Kohm resistor	Z
HDMI_CLK_P	HDMI differential CLK positive output	Z
HDMI_CLK_N	HDMI differential CLK negative output	Z
HDMI_CH0_P	HDMI differential CH0 positive output	Z
HDMI_CH0_N	HDMI differential CH0 negative output	Z
HDMI_CH1_P	HDMI differential CH1 positive output	Z
HDMI_CH1_N	HDMI differential CH1 negative output	Z
HDMI_CH2_P	HDMI differential CH2 positive output	Z
HDMI_CH2_N	HDMI differential CH2 negative output	Z





Note:

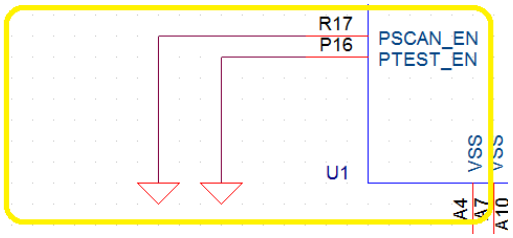
1.Please add the Voltage level shifter design in different Voltage level from 3.3V to 5V.

2.Need to add the ESD component near the HDMI Connector Side.

3.Need to add the Charge pump IC for HDMI 5V power source.

11. TEST pin

Pin Name	Pin Description	Reset State
PTEST_EN	For test mode only	LZ
PSCAN_EN	For test mode only	LZ



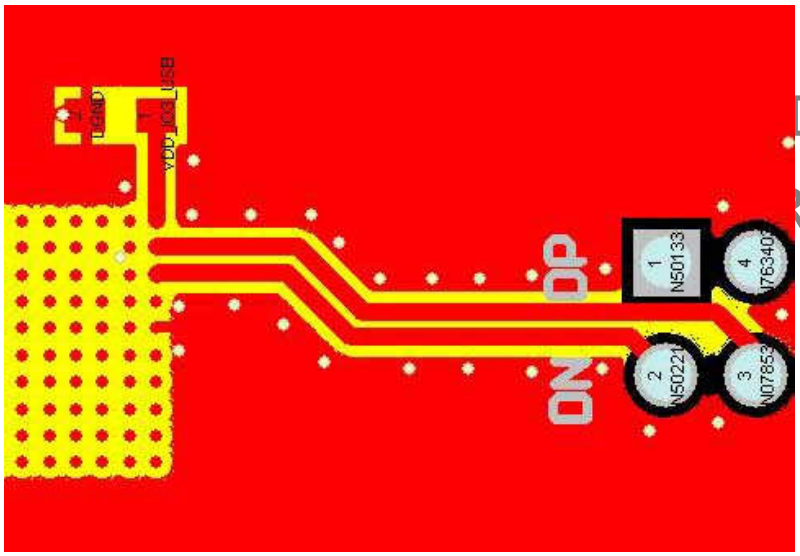
Note:

1.Please Short these TEST pins to GND.

12. PCB Layout Guide

12.1. USB 2.0 Part PCB Layout Guide

1. The DP / DM signal pair must be routed together parallel to each other on the same layer.
2. To decrease crosstalk and EMI, designers can adopt the ground guard in the DP / DM signal.
3. The DP / DM signal traces must be the same length and the traces must be as short as possible. This minimizes the common mode current effect on EMI.
4. Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
5. The trace impedance for the DP / DM signals should be 45Ω±10% (Microstrip or Stripline). The impedance is 90Ω±10% between the differential signal pairs DP and DM.
6. Layout example:



12.2. Audio Part PCB Layout Guide

1. The audio signal pairs must be routed together parallel to each other on the same layer.
2. Use ground guard traces with shorting vias on the ends and throughout the length.
3. Increase the space of the audio traces (refer to the 3-W rule).

12.3. HDMI Layout Guide

1) Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.

2) Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering

correction along the signal path. Use chamfered corners with a length-to-trace width ratio of 3 to 5. The distance between bends should be at least 8 to 10 times the trace width.

3) Use 45o bends (chamfered corners), instead of right-angle (90o) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating a small discontinuity. A 45o bends is seen as an even smaller discontinuity.

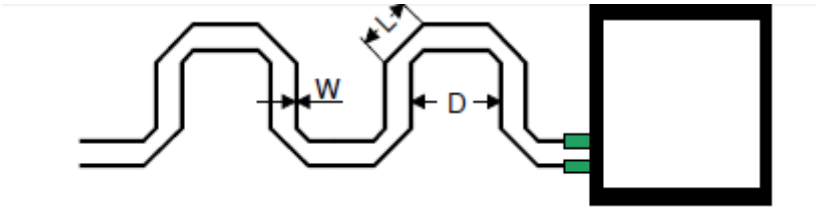


Fig. 1. Skew reduction via meandering using chamfered corners

4) When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.

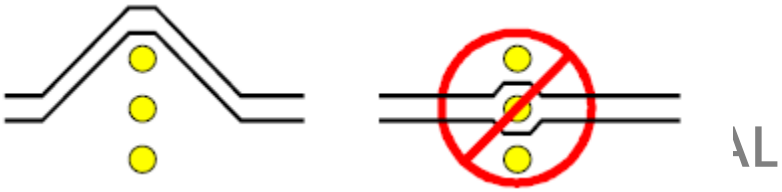


Fig. 2. Routing around an object

5) Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) does create wider trace spacing than in b); however, the resulting discontinuity is limited to a far narrower electrical length.

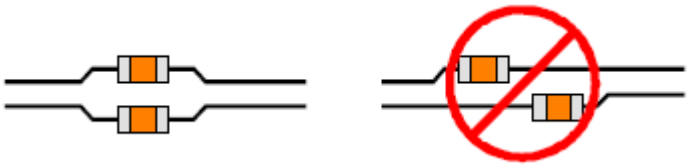


Fig.3. Lumping discontinuities

6) When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.

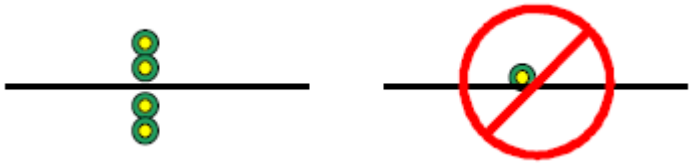


Fig. 4. Avoiding via clearance sections

7) Avoid metal layers and traces underneath or between the pads of the HDMI connectors for better impedance matching. Otherwise they may cause the differential impedance to drop below 75 _ and fail

your board during TDR testing.

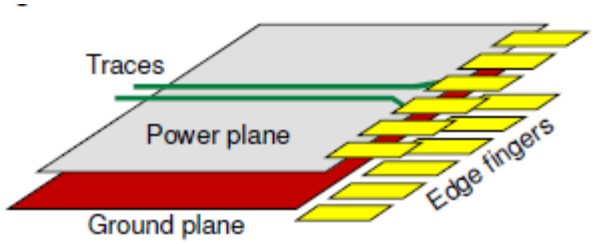


Fig. 5. Keeping planes out of the area between edge-fingers

8) Use the smallest size possible for signal trace vias and HDMI connector pads as they have less impact on the 100 _ differential impedance. Large vias and pads can cause the impedance to drop below 85 _.

9) Use solid power and ground planes for 100 _ impedance control and minimum power noise.