SSC337DE
High-Integrated IP Camera SoC Processor

Preliminary Product Brief Version 0.2

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REVISION HISTORY

Revision No.	Description	Date
0.1	• Initial release	12/02/2019
0.2	• Updated encoder spec.	12/16/2019

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FEATURES

- High Performance Processor Core
  - ARM Cortex-A7 Single Core
  - Neon and FPU
  - Memory Management Unit for Linux support
  - DMA Engine
- Image/Video Processor
  - Supports 10/12-bit parallel interface for raw data input
  - Supports MIPI interface with four data lanes and one clock lane
  - Supports 8/10-bit CCIR656 interface
  - Supports 5M (2560x1920) pixels video recording and image snapshot
  - Bad pixel compensation
  - Noise Reduction (NR)
  - Optical black correction
  - Lens shading compensation
  - Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
  - CFA color interpolation
  - Color correction
  - Gamma correction
  - Wide Dynamic Range (WDR)
  - Fully programmable multi-function scaling engines
  - High Dynamic Range (HDR) with two exposure frames
- H.265/HEVC Encoder
  - Supports H.265/HEVC main profile encoding
  - Supports MVs 32x32, 16x16, and 8x8
  - Supports up to quarter-pixel
  - Supports frame level and MB level rate control
  - Supports ROI (Intra map or ZMV map)
  - Supports max. 5M + D1 + CIF @ 20fps or 4M + D1 + CIF @ 25fps encoding
- H.264 Encoder
  - Supports H.264 baseline and main profile encoding
  - Supports MVs 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, and 4x4
  - Supports up to quarter-pixel
  - Supports frame level and MB level rate control
  - Supports ROI (Intra map or ZMV map)
  - Supports max. 5M + D1 + CIF @ 20fps or 4M + D1 + CIF @ 25fps encoding
- JPEG Encoder
  - Supports JPEG baseline encoding
  - Supports YUV422 or YUV420 format
  - Supports max. 5M @ 20fps encoding
  - Supports real-time mode and frame encode mode
- Video Encoding Performance
  - Supports 5M + D1 + CIF @ 20fps or 4M + D1 + CIF @ 25fps H.265/HEVC or H.264 encoding
  - Supports MJPEG up to 5M @ 20fps encoding
- Audio Processor
  - One stereo ADC for microphone inputs
  - Two DACs for lineout
  - Supports 8K/16K/32KHz sampling rate audio recording
  - Digital and analog gain adjustment
- SPI NOR/NAND Flash Interface
  - Compliant with standard, dual and quad SPI flash memory components
- SD Card Interface
  - Compatible with SD spec. 2.0, data bus 1/4-bit mode
  - Compatible with SDIO spec. 2.0, data bus 1/4-bit mode
- SDIO 2.0 Interface
  - Compatible with SDIO spec. 2.0, data bus 1/4-bit mode
  - Compatible with SD spec. 2.0, data bus 1/4-bit mode

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- USB 2.0 Interface
  - One USB 2.0 configurable host or device
    - Host mode supports EHCI specifications
    - Device mode supports 3 endpoints
- DRAM Memory
  - Embedded 128MB DDR3
- Connectivity
  - Built-in 10/100M Ethernet MAC and Ethernet PHY
  - One USB 2.0 Host Controller could be used for USB Wi-Fi dongle or module
  - Two SDIO 2.0 Host Controllers could be used for SDIO Wi-Fi module
- Security Engines
  - Supports AES128/AES192/AES256/ DES/3DES/RSA/SHA-I/SHA-256
  - Supports secure booting
- Real Time Clock (RTC)
  - Built-in RTC working with 32.768 KHz crystal
  - Alarm interrupt for wakeup
  - Tick time interrupt (millisecond)
  - Built-in regulator
  - Support low leakage RTC-mode for long battery application
- Boot Options
  - SPI NOR
  - SPI NAND
  - SD Card
- Peripherals
  - Dedicated GPIOs for system control
  - Supports 11 PWM outputs (shared with GPIOs)
  - Three generic UARTs including one fast UART with flow control
  - Three generic timers and one watchdog timer
  - Two SPI masters
  - Two I2C Masters
  - Built-in 10-bit SAR ADC with 4-channel analog inputs for different kinds of application
  - Supports internal temperature sensor
  - Supports ISP sensor clock 12MHz, 24MHz, 37.125MHz
- Operating Voltage Range
  - Core: 0.9 ~ 1.0V
  - I/O: 1.8 ~ 3.3V
  - DRAM: 1.5V
  - Power Consumption: TBD
- Package
  - 128-pin QFN, 12.3mm x 12.3mm

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GENERAL DESCRIPTIONS

The SSC337DE is a highly integrated SoC. Based on ARM Cortex-A7, the application processor integrates Image Signal Processor (ISP), Video (H.264/H.265/MJPEG) Encoders and other useful peripherals for IP camera applications.

A typical utilization of the SSC337DE application processor is demonstrated in the following block diagram. The complete system includes a camera module (CMOS sensor), a connectivity module (Wi-Fi or Ethernet), and a non-volatile storage (SPI NOR/NAND flash or SD card). The ISP handles images captured from the camera sensor, and the video stream is composed of a large amount of images. There are pre- and post- video processing stages. The pre-video processing reduces noises, enhances signals and translates color domains. The post-video processing adjusts color quality, and generates multiple video streams with different resolutions. Multimedia Encoders can compress those video streams with different compressing standards at the same time. The well compressed video/audio streams could be streamed or stored in the cloud server through Wi-Fi or Ethernet or stored in a local SD card. The SPI NOR/NAND flash is usually reserved for operating system and application software. Moreover, other peripherals such as SAR ADC, Audio ADC/DAC, UARTs, PWMs, GPIOs and SPI are supported to realize applications with maximal flexibility.

The SSC337DE supports secure booting and personalization authentication mechanism for system security. The AES/DES/3DES cipher engines could further help encrypt the compressed video/audio streams to enhance privacy.

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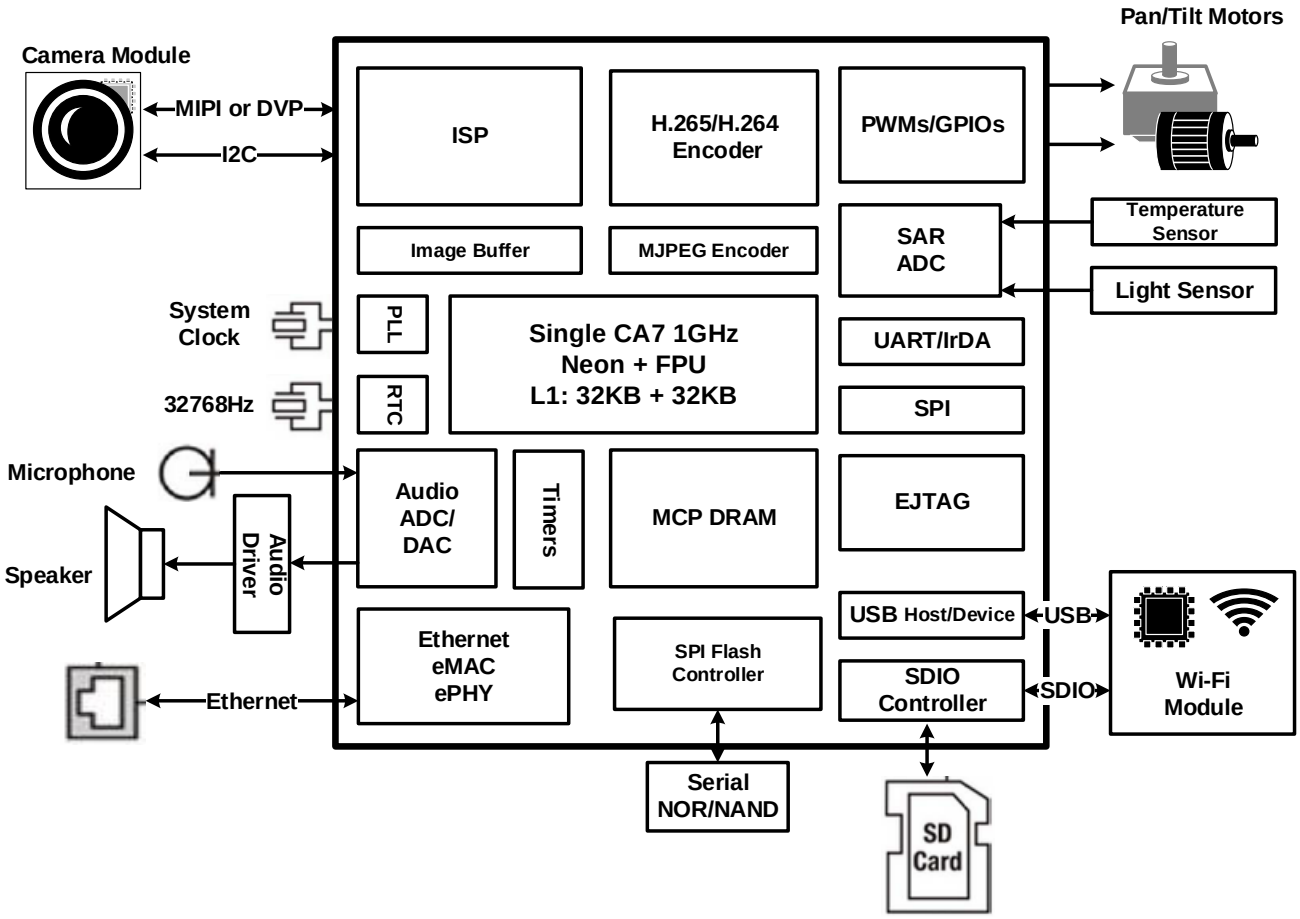
BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Video Encoder

I. JPE Feature Description

- Supports JPEG encoding 5M @ 20fps
  - Frame mode
  - IMI row mode
- Supports YUYV input format
- Supports NV12 input format
- Supports DCT mode to accelerate SW encoding

II. H.264/H.265 Feature Description

H.264/H.265 engine (abbr. as VEN) is a hardware encoder for H.264/H.265 baseline/main profile. It encodes image data from frame buffer (DRAM) in YUV420 format and generates bit-streams to memory. Maximum resolution of 5M (2560x1920) with 20fps or 4M (2592x1520) with 25fps is supported.

In IP-CAM application, the bitrate is very important due to limited storage space in long time recording. Consequently, VEN implements bitrate control mechanism in frame level or macro-block (MB) level. Both variable bitrate (VBR) and constant bitrate (CBR) are supported. In general, VBR encoding will produce better image quality than CBR.

To save memory bandwidth, VEN provides data compression/decompression option when accessing DRAM. Besides, internal SRAM is used as a cache architecture to reduce DRAM read/write operations. It is very helpful in complex system application where HDR, and/or fisheye correction are enabled simultaneously.

Another feature called Region of Interest (ROI) Encoding is supported to provide the highest image quality on the areas or scene or objects of most interest while reducing the quality level in uninteresting areas to provide the highest quality/lowest bandwidth results.

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ISP

I. Brief Feature Description

The ISP design is used to transfer raw sensor data output to YUV data. It also supports YUV sensor at ISP bypass mode default.

- Supports up to 5M (2560x1920) @25Hz
- HDR
- WDR
- Bad pixel compensation
- Green equal
- Supports rgbir2x2 or rgbir4x4 mode input
- Optical black correction
- Lens shading compensation
- Asymmetric lens shading compensation
- Statistic for AWB/AE/AF
- Supports de-noise 3DNR/2DNR
- White Balance PreGain and PostGain can be enabled at the same time
- CFA color interpolation
- Gamma correction
- Edge enhancement
- Supports menuload for ALSC_gain/DefectPxl/Gamma table

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Peripheral

I. USB Brief Feature Description

One port of host/OTG controller is fully compliant with the USB 2.0 specification and the Enhanced Host Controller Interface (EHCI) specification. This Host/OTG Controller can support FS/LS transactions, Interrupt/Control/Bulk transfers and split/preamble transactions for hub.

II. MIPI CSI Interface

The features are listed below:

- CSI-2 1.1/D-PHY 1.1 compliant receiver with maximum Input Frequency 1.5GHz
- Supports 1 clock lane, 4 data lanes
- Supports YUV422 8-bit, Raw8, Raw10, Raw12, Generic 8-bit long packet and User defined byte-based data type
- Supports 1-bit error correction/2-bit error detection for packet header
- Supports checksum error detection for payload data
- Supports timing generation for Vsync and Hsync

III. Ethernet MAC Brief Feature Description

- IEEE Std 802.3 compatible
- Supports 10/100 Mbit/s operation.
- Full/Half duplex support.
- Automatic pad and CRC generation on transmitted packet.
- Supports transmit packet(IP/TCP/UDP) checksum generate
- Receiver & Transmitter Packet management by internal storage with descriptor header control
- Internal async-FIFO for receiver & transmitter frame wire speed operation
- Supports Tagged frame
- Supports IPV6 check-sum
- Supports IEEE802.3az EEE function

IV. EPHY Brief Feature Description

The Ethernet PHY (EPHY) is an IEEE 802.3 compliant single-port Ethernet Transceiver for both 100Mbps and 10Mbps operations. The EPHY acts as an interface between the physical signaling and the Media Access Controller (MAC). It supports the Auto-Negotiation function to simplify the network installation and maintenance.

The major functions of EPHY included:

- 10/100Mbps TX/RX
- Full-duplex or half duplex
- Supports IEEE 802.3u auto-negotiation
- DSP-based PHY Transceiver technology
- Supports WOL (Wake on Lan) feature (Magic Packet only)
- Supports IEEE 802.3az EEE function

V. Encryption Brief Feature Description

AESDMA is a secure IP for Secure Boot and HDMI Key Authentication. There are three engines inside this IP:

- AES: ECB, CBC (dvs042), ECB_CTS, CBC_CTS, CTR
- SHA: SHA_1, SHA_256
- RSA: RSA_2048 in HW key mode, programmable size in SW key mode

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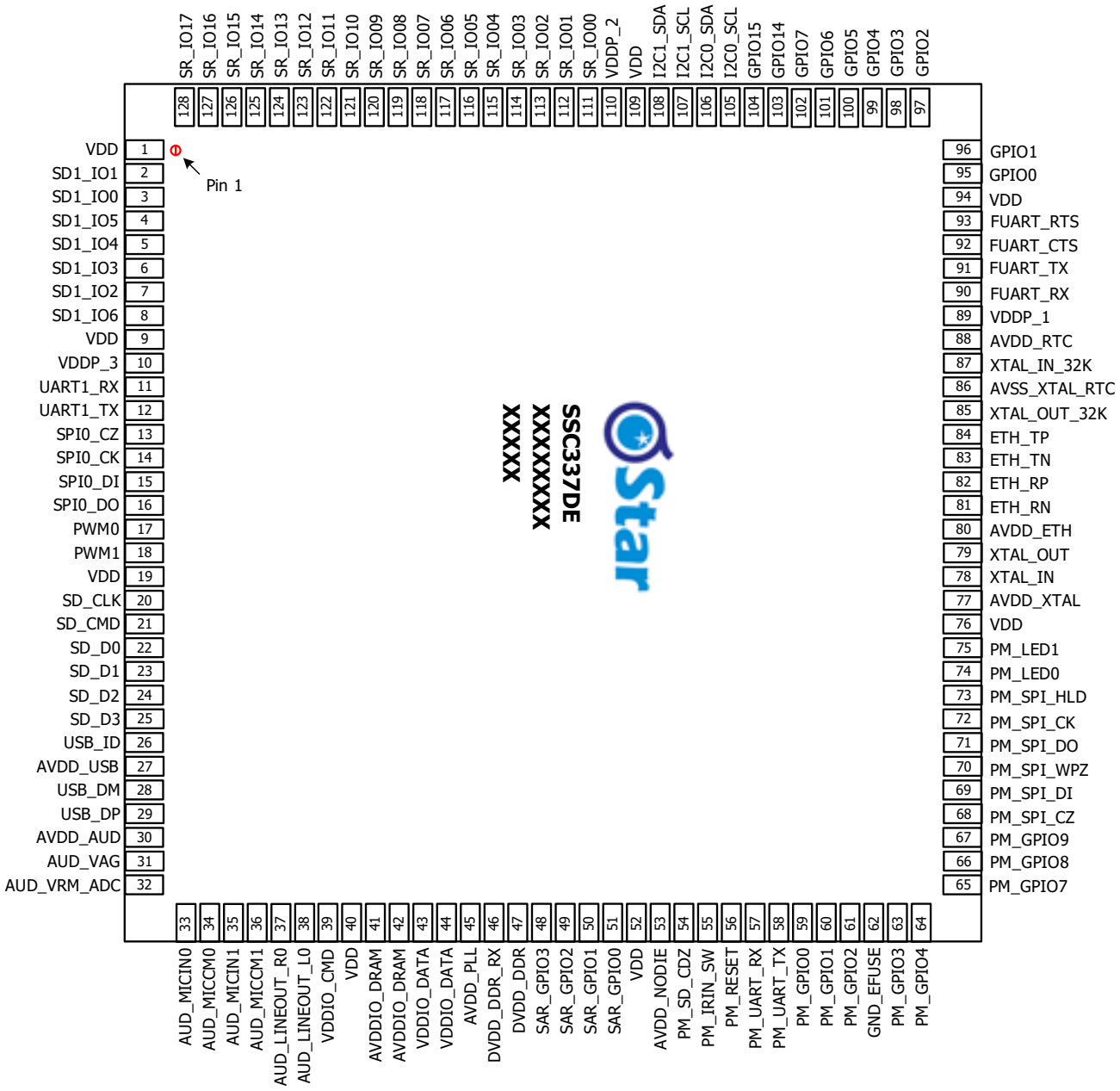
PIN DIAGRAM



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SIGNAL DESCRIPTION

Signal Name	Signal Type	Function	QFN128 (12.3 x 12.3) Pin Location
System Reset Interface			
PM_RESET	I	System Reset (Active High)	56
Debug UART Interface			
PM_UART_RX	I	Debug UART Receive Data Input with Pull Up Resistor / Slave I2C Serial Clock	57
PM_UART_TX	O	Debug UART Transmit Data Output with Pull Up Resistor / Slave I2C Serial Data	58
System Interface			
XTAL_IN	I	24MHz Crystal Input	78
XTAL_OUT	O	24MHz Crystal Output	79
XTAL_IN_32K	I	32.768KHz Crystal Input	87
XTAL_OUT_32K	O	32.768KHz Crystal Output	85
SPI Flash Interface			
PM_SPI_CZ	O	SPI Flash Chip Select (Active Low)	68
PM_SPI_DI	O	SPI Flash Serial Data To Device (MOSI)	69
PM_SPI_WPZ	O	SPI Flash Write Protect	70
PM_SPI_DO	I	SPI Flash Serial Data From Device (MISO)	71
PM_SPI_CK	O	SPI Flash Clock	72
PM_SPI_HLD	O	SPI Flash Hold	73
PM GPIO Interface			
PM_GPIO0	I/O	Power Manage Group General Purpose Input/Output 0	59
PM_GPIO1	I/O	Power Manage Group General Purpose Input/Output 1	60
PM_GPIO2	I/O	Power Manage Group General Purpose Input/Output 2	61
PM_GPIO3	I/O	Power Manage Group General Purpose Input/Output 3	63
PM_GPIO4	I/O	Power Manage Group General Purpose Input/Output 4	64

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Signal Name	Signal Type	Function	QFN128 (12.3 x 12.3) Pin Location
PM_GPIO7	I/O	Power Manage Group General Purpose Input/Output 7	65
PM_GPIO8	I/O	Power Manage Group General Purpose Input/Output 8	66
PM_GPIO9	I/O	Power Manage Group General Purpose Input/Output 9	67
PM_IRIN_SW	I	General Purpose Input/Output Software Mode Infrared Input from IR Receiver	55
SAR ADC Interface			
SAR_GPIO0	I	General Purpose Input/Output or Muxed to SARADC Input Channel 0	51
SAR_GPIO1	I	General Purpose Input/Output or Muxed to SARADC Input Channel 1	50
SAR_GPIO2	I	General Purpose Input/Output or Muxed to SARADC Input Channel 2	49
SAR_GPIO3	I	General Purpose Input/Output or Muxed to SARADC Input Channel 3	48
GPIO Interface			
GPIO0	I/O	General Purpose Input/Output 0	95
GPIO1	I/O	General Purpose Input/Output 1	96
GPIO2	I/O	General Purpose Input/Output 2	97
GPIO3	I/O	General Purpose Input/Output 3	98
GPIO4	I/O	General Purpose Input/Output 4	99
GPIO5	I/O	General Purpose Input/Output 5	100
GPIO6	I/O	General Purpose Input/Output 6	101
GPIO7	I/O	General Purpose Input/Output 7	102
GPIO14	I/O	General Purpose Input/Output 14	103
GPIO15	I/O	General Purpose Input/Output 15	104
Master I2C Interface			
I2C0_SCL	O	I2C 0 Master Mode I2C Clock	105
I2C0_SDA	I	I2C 0 Master Mode I2C Data	106
I2C1_SCL	O	I2C 1 Master Mode I2C Clock (for Sensor)	107
I2C1_SDA	I	I2C 1 Master Mode I2C Data (for Sensor)	108

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Signal Name	Signal Type	Function	QFN128 (12.3 x 12.3) Pin Location
Master SPI Interface			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	13
SPI0_CK	O	Master SPI 0 Serial Clock	14
SPI0_DI	O	Master SPI 0 Serial Data To Device (MOSI)	15
SPI0_DO	I	Master SPI 0 Serial Data From Device (MISO)	16
UART Interface			
UART1_RX	I	UART 1 Receive Data Input	11
UART1_TX	O	UART 1 Transmit Data Output	12
Fast UART Interface			
FUART_RX	I	Fast UART Receive Data Input	90
FUART_TX	O	Fast UART Transmit Data Output	91
FUART_CTS	I	Fast UART Clear to Send	92
FUART_RTS	O	Fast UART Request to Send	93
PWM Interface			
PWM0	O	PWM 0 Output	17
PWM1	O	PWM 1 Output	18
Image Sensor Interface			
SR_IO00	I/O	Sensor General Purpose Input/Output 0	111
SR_IO01	I/O	Sensor General Purpose Input/Output 1	112
SR_IO02	I/O	Sensor General Purpose Input/Output 2	113
SR_IO03	I/O	Sensor General Purpose Input/Output 3	114
SR_IO04	I/O	Sensor General Purpose Input/Output 4	115
SR_IO05	I/O	Sensor General Purpose Input/Output 5	116
SR_IO06	I/O	Sensor General Purpose Input/Output 6	117
SR_IO07	I/O	Sensor General Purpose Input/Output 7	118
SR_IO08	I/O	Sensor General Purpose Input/Output 8	119
SR_IO09	I/O	Sensor General Purpose Input/Output 9	120
SR_IO10	I/O	Sensor General Purpose Input/Output 10	121
SR_IO11	I/O	Sensor General Purpose Input/Output 11	122
SR_IO12	I/O	Sensor General Purpose Input/Output 12	123
SR_IO13	I/O	Sensor General Purpose Input/Output 13	124
SR_IO14	I/O	Sensor General Purpose Input/Output 14	125

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Signal Name	Signal Type	Function	QFN128 (12.3 x 12.3) Pin Location
SR_IO15	I/O	Sensor General Purpose Input/Output 15	126
SR_IO16	I/O	Sensor General Purpose Input/Output 16	127
SR_IO17	I/O	Sensor General Purpose Input/Output 17	128
10/100M Ethernet Interface			
ETH_RN	I	10/100M Ethernet Differential Pair of Receiver Signal Negative	81
ETH_RP	I	10/100M Ethernet Differential Pair of Receiver Signal Positive	82
ETH_TN	O	10/100M Ethernet Differential Pair of Transmitter Signal Negative	83
ETH_TP	O	10/100M Ethernet Differential Pair of Transmitter Signal Positive	84
PM_LED0	O	10/100M Ethernet LED0 Control Driven Active When Linked	74
PM_LED1	O	10/100M Ethernet LED1 Control Driven Active When Linked in 100 Base-TX and Blinking When Transmitting or Receiving Data	75
SD 2.0 Card Interface			
SD_CLK	O	SD 2.0 Clock	20
SD_CMD	O	SD 2.0 Command	21
SD_D0	I/O	SD 2.0 Data Bus 0	22
SD_D1	I/O	SD 2.0 Data Bus 1	23
SD_D2	I/O	SD 2.0 Data Bus 2	24
SD_D3	I/O	SD 2.0 Data Bus 3	25
PM_SD_CDZ	I	Power Manage SD 2.0 Card Detect	54
SDIO 2.0 Interface			
SD1_IO0	I/O	SDIO 2.0 Card Data Bus 0	3
SD1_IO1	I/O	SDIO 2.0 Card Data Bus 1	2
SD1_IO2	I/O	SDIO 2.0 Card Data Bus 2	7
SD1_IO3	I/O	SDIO 2.0 Card Data Bus 3	6
SD1_IO4	O	SDIO 2.0 Card Command	5
SD1_IO5	O	SDIO 2.0 Card Clock	4
SD1_IO6	I	SDIO 2.0 Card Detect (Active Low)	8

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Signal Name	Signal Type	Function	QFN128 (12.3 x 12.3) Pin Location
Line Out Interface			
AUD_LINEOUT_L0	O	Audio Left Channel Line Output	38
AUD_LINEOUT_R0	O	Audio Right Channel Line Output	37
AUD_VAG	O	Audio Reference Voltage from 1/2 AVDD_AUD	31
AUD_VRM_ADC	I	Audio Reference Voltage for ADC	32
Analog Microphone Interface			
AUD_MICIN0	I	Audio Left Channel Microphone Positive Input	33
AUD_MICCM0	I	Audio Left Channel Microphone Negative Input	34
AUD_MICIN1	I	Audio Right Channel Microphone Positive Input	35
AUD_MICCM1	I	Audio Right Channel Microphone Negative Input	36
USB 2.0 Interface			
USB_ID	I	USB 2.0 ID (High: Slave Mode, Low: Host Mode)	26
USB_DM	I/O	USB 2.0 Differential Pair, Negative	28
USB_DP	I/O	USB 2.0 Differential Pair, Positive	29
Power Pins			
VDD	Core Power	Digital Core Power	1, 9, 19, 40, 52, 76, 94, 109
VDDP_1	3.3V Power	Digital Power for VDDP_1 Group	89
VDDP_2	1.8/3.3V Power	Digital Power for VDDP_2 Group (Sensor IO Power)	110
VDDP_3	3.3V Power	Digital Power for VDDP_3 Group	10
DVDD_DDR_RX	Core Power	Digital Power for DDR RX	46
DVDD_DDR	Core Power	Digital Power for DDR TX	47
VDDIO_DATA	DDR Power	Analog Power for DDR MCLK/DATA	43, 44
VDDIO_CMD	DDR Power	Analog Power for DDR CMD	39
AVDDIO_DRAM	DDR Power	Stack DRAM Power	41, 42
AVDD_NODIE	3.3V Power	Analog Power for PM	53
AVDD_PLL	3.3V Power	Analog Power for PLL	45
AVDD_XTAL	3.3V Power	Analog Power for XTAL	77
AVDD_RTC	3.3V Power	Analog Power for RTC	88

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Signal Name	Signal Type	Function	QFN128 (12.3 x 12.3) Pin Location
AVDD_USB	3.3V Power	Analog Power for USB	27
AVDD_ETH	3.3V Power	Analog Power for Ethernet	80
AVDD_AUD	3.3V Power	Analog Power for Audio	30
GND_EFUSE	I	Power Source if eFuse is Burnt (Connected to Ground)	62
AVSS_XTAL_RTC	GND	Analog Ground for RTC Crystal	86
GND	GND	Digital Ground	ePad

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PIN CHARACTERISTICS

QFN128 (12.3 x 12.3) Pin Location	Ball/Pin Name	Default Value after Reset	5V-tolerance	Driving Control
54	PM_SD_CDZ	Input, pull-up	Yes	
55	PM_IRIN	Input, pull-up	Yes	
59	PM_GPIO0	Input, pull-down	Yes	
60	PM_GPIO1	Input, pull-down	Yes	
61	PM_GPIO2	Input, pull-down	Yes	
63	PM_GPIO3	Input, pull-down	Yes	
64	PM_GPIO4	Input, pull-up	Yes	
65	PM_GPIO7	Input, pull-up	Yes	
66	PM_GPIO8	Input, pull-up	Yes	
67	PM_GPIO9	Input, pull-up	Yes	
68	PM_SPI_CZ	Output	Yes	Yes
69	PM_SPI_DI	Output	Yes	Yes
70	PM_SPI_WPZ	Output	Yes	Yes
71	PM_SPI_DO	Input, pull-up	Yes	Yes
72	PM_SPI_CK	Output	Yes	Yes
73	PM_SPI_HLD	Output	Yes	Yes
74	PM_LED0	Input, pull-down	Yes	Yes
75	PM_LED1	Input, pull-down	Yes	Yes
48	SAR_GPIO3	-	Yes	
49	SAR_GPIO2	-	Yes	
50	SAR_GPIO1	-	Yes	
51	SAR_GPIO0	-	Yes	
81	ETH_RN	-	No	
82	ETH_RP	-	No	
83	ETH_TN	-	No	
84	ETH_TP	-	No	
105	I2C0_SCL	Input, pull-up	Yes	
106	I2C0_SDA	Input, pull-up	Yes	
95	GPIO0	Input, pull-up	Yes	

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QFN128 (12.3 x 12.3) Pin Location	Ball/Pin Name	Default Value after Reset	5V-tolerance	Driving Control
96	GPIO1	Input, pull-up	Yes	
97	GPIO2	Input, pull-up	Yes	
98	GPIO3	Input, pull-up	Yes	
99	GPIO4	Input, pull-up	Yes	
100	GPIO5	Input, pull-up	Yes	
101	GPIO6	Input, pull-up	Yes	
102	GPIO7	Input, pull-up	Yes	
103	GPIO14	Input, pull-up	Yes	
104	GPIO15	Input, pull-up	Yes	
90	FUART_RX	Input, pull-up	Yes	
91	FUART_TX	Input, pull-up	Yes	
92	FUART_CTS	Input, pull-up	Yes	
93	FUART_RTS	Input, pull-up	Yes	
107	I2C1_SCL	Input, pull-up	Yes	Yes
108	I2C1_SDA	Input, pull-up	Yes	Yes
111	SR_IO00	Input, pull-up	No	Yes
112	SR_IO01	Input, pull-up	No	Yes
113	SR_IO02	Input, pull-up	No	Yes
114	SR_IO03	Input, pull-up	No	Yes
115	SR_IO04	Input, pull-up	No	Yes
116	SR_IO05	Input, pull-up	No	Yes
117	SR_IO06	Input, pull-up	No	Yes
118	SR_IO07	Input, pull-up	No	Yes
119	SR_IO08	Input, pull-up	No	Yes
120	SR_IO09	Input, pull-up	No	Yes
121	SR_IO10	Input, pull-up	No	Yes
122	SR_IO11	Input, pull-up	No	Yes
123	SR_IO12	Input, pull-down	No	Yes
124	SR_IO13	Input, pull-down	No	Yes

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QFN128 (12.3 x 12.3) Pin Location	Ball/Pin Name	Default Value after Reset	5V-tolerance	Driving Control
125	SR_IO14	Input, pull-up	No	Yes
126	SR_IO15	Input, pull-up	No	Yes
127	SR_IO16	Input, pull-up	No	Yes
128	SR_IO17	Input, pull-up	No	Yes
3	SD1_IO0	Input, pull-up	Yes	Yes
2	SD1_IO1	Input, pull-up	Yes	Yes
7	SD1_IO2	Input, pull-up	Yes	Yes
6	SD1_IO3	Input, pull-up	Yes	Yes
5	SD1_IO4	Input, pull-up	Yes	Yes
4	SD1_IO5	Input, pull-down	Yes	Yes
8	SD1_IO6	Input, pull-up	Yes	Yes
11	UART1_RX	Input, pull-up	Yes	Yes
12	UART1_TX	Input, pull-up	Yes	Yes
13	SPI0_CZ	Input, pull-up	No	Yes
14	SPI0_CK	Input, pull-down	No	Yes
15	SPI0_DI	Input, pull-down	No	Yes
16	SPI0_DO	Input, pull-down	No	Yes
17	PWM0	Input, pull-down	Yes	Yes
18	PWM1	Input, pull-down	Yes	Yes
20	SD_CLK	Input, pull-down	Yes	Yes
21	SD_CMD	Input, pull-up	Yes	Yes
22	SD_D0	Input, pull-up	Yes	Yes
23	SD_D1	Input, pull-up	Yes	Yes
24	SD_D2	Input, pull-up	Yes	Yes
25	SD_D3	Input, pull-up	Yes	Yes
28	USB_DM	-	No	
29	USB_DP	-	No	

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MULTI-FUNCTION TABLE

Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
Image Sensor (Parallel/BT656)			
SR_IO00	I	Parallel Input Data Bit 0	111
SR_IO01	I	Parallel Input Data Bit 1	112
SR_IO02	I	Parallel Input Data Bit 2 BT656 Input Data Bit 0	113
SR_IO03	I	Parallel Input Data Bit 3 BT656 Input Data Bit 1	114
SR_IO04	I	Parallel Input Data Bit 4 BT656 Input Data Bit 2	115
SR_IO05	I	Parallel Input Data Bit 5 BT656 Input Data Bit 3	116
SR_IO06	I	Parallel Input Data Bit 6 BT656 Input Data Bit 4	117
SR_IO07	I	Parallel Input Data Bit 7 BT656 Input Data Bit 5	118
SR_IO08	I	Parallel Input Data Bit 8 BT656 Input Data Bit 6	119
SR_IO09	I	Parallel Input Data Bit 9 BT656 Input Data Bit 7	120
SR_IO10	I	Parallel Input Data Bit 10 BT656 Input Data Bit 8	121
SR_IO11	I	Parallel Input Data Bit 11 BT656 Input Data Bit 9	122
Parallel /BT656 Control			
SR_IO12	O	SNR Power Down Control	123
SR_IO13	O	SNR Reset	124
SR_IO14	I	Parallel HSYNC Input	125
SR_IO15	I	Parallel / BT656 Pixel Clock Input	126
SR_IO16	I	Parallel VSYNC Input	127
SR_IO17	O	SNR Master Clock Output	128
Image Sensor (4 lane MIPI_Mode1)			
SR_IO01	I	MIPI Data Input (Differential Pair 0, Negative)	112
SR_IO02	I	MIPI Data Input (Differential Pair 0, Positive)	113

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
SR_IO03	I	MIPI Data Input (Differential Pair 1, Negative)	114
SR_IO04	I	MIPI Data Input (Differential Pair 1, Positive)	115
SR_IO05	I	MIPI Clock Input (Differential Clock Pair, Negative)	116
SR_IO06	I	MIPI Clock Input (Differential Clock Pair, Positive)	117
SR_IO07	I	MIPI Data Input (Lane2) (Differential Pair 2, Negative)	118
SR_IO08	I	MIPI Data Input (Lane2) (Differential Pair 2, Positive)	119
SR_IO09	I	MIPI Data Input (Lane3) (Differential Pair 3, Negative)	120
SR_IO10	I	MIPI Data Input (Lane3) (Differential Pair 3, Positive)	121
Image Sensor (2 lane MIPI_Mode2)			
SR_IO03	I	MIPI Data Input (Differential Pair 0, Negative)	114
SR_IO04	I	MIPI Data Input (Differential Pair 0, Positive)	115
SR_IO05	I	MIPI Clock Input (Differential Clock Pair, Negative)	116
SR_IO06	I	MIPI Clock Input (Differential Clock Pair, Positive)	117
SR_IO07	I	MIPI Data Input (Differential Pair 1, Negative)	118
SR_IO08	I	MIPI Data Input (Differential Pair 1, Positive)	119
Image Sensor (2 lane MIPI_Mode3)			
SR_IO01	I	MIPI Data Input (Differential Pair 0, Negative)	112
SR_IO02	I	MIPI Data Input (Differential Pair 0, Positive)	113
SR_IO03	I	MIPI Data Input (Differential Pair 1, Negative)	114
SR_IO04	I	MIPI Data Input (Differential Pair 1, Positive)	115
SR_IO05	I	MIPI Clock Input (Differential Clock Pair, Negative)	116
SR_IO06	I	MIPI Clock Input (Differential Clock Pair, Positive)	117
MIPI Control			
SR_IO12	O	SNR Power Down Control	123
SR_IO13	O	SNR Reset	124
SR_IO17	O	SNR Master Clock Output	128
DMIC Mode1			
DMIC_L	I	Digital Left Channel Line Input	99
DMIC_R	I	Digital Right Channel Line Input	100
DMIC_CLK	O	DMIC Output Clock	101

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
DMIC Mode2			
DMIC_L	I	Digital Left Channel Line Input	8
DMIC_R	I	Digital Right Channel Line Input	5
DMIC_CLK	O	DMIC Output Clock	4
I2S Mode1			
I2S_WCK	O	I2S Word Clock	95
I2S_BCK	O	I2S Bit Clock	96
I2S_SDI	I	I2S Data Input	97
I2S_SDO	O	I2S Data Output	98
I2S Mode2			
I2S_WCK	O	I2S Word Clock	3
I2S_BCK	O	I2S Bit Clock	2
I2S_SDI	I	I2S Data Input	7
I2S_SDO	O	I2S Data Output	6
JTAG Mode1			
EJ_TCK	I	CA7 JTAG Clock	90
EJ_TMS	I	CA7 JTAG Mode Select	91
EJ_TDO	O	CA7 JTAG Data Out	92
EJ_TDI	I	CA7 JTAG Data In	93
JTAG Mode2			
EJ_TCK	I	CA7 JTAG Clock	13
EJ_TMS	I	CA7 JTAG Mode Select	14
EJ_TDO	O	CA7 JTAG Data Out	15
EJ_TDI	I	CA7 JTAG Data In	16
I2C 0 Mode1			
I2C0_SCL	O	Master I2C 0 Serial Clock	105
I2C0_SDA	I/O	Master I2C 0 Serial Data	106
I2C 0 Mode2			
I2C0_SCL	O	Master I2C 0 Serial Clock	17
I2C0_SDA	I/O	Master I2C 0 Serial Data	18
I2C 0 Mode3			
I2C0_SCL	O	Master I2C 0 Serial Clock	112
I2C0_SDA	I/O	Master I2C 0 Serial Data	113

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
I2C 0 Mode4			
I2C0_SCL	O	Master I2C 0 Serial Clock	11
I2C0_SDA	I/O	Master I2C 0 Serial Data	12
I2C 1 Mode1			
I2C1_SCL	O	Master I2C 1 Serial Clock (for Sensor)	107
I2C1_SDA	I/O	Master I2C 1 Serial Data (for Sensor)	108
I2C 1 Mode2			
I2C1_SCL	O	Master I2C 1 Serial Clock	17
I2C1_SDA	I/O	Master I2C 1 Serial Data	18
I2C 1 Mode3			
I2C1_SCL	O	Master I2C 1 Serial Clock	112
I2C1_SDA	I/O	Master I2C 1 Serial Data	113
UART 0 Mode2			
UART0_RX	I	UART 0 Receiver	90
UART0_TX	O	UART 0 Transmitter	91
UART 0 Mode3			
UART0_RX	I	UART 0 Receiver	99
UART0_TX	O	UART 0 Transmitter	100
UART 1 Mode1			
UART1_RX	I	UART 1 Receiver	11
UART1_TX	O	UART 1 Transmitter	12
UART 1 Mode2			
UART1_RX	I	UART 1 Receiver	92
UART1_TX	O	UART 1 Transmitter	93
UART 1 Mode3			
UART1_RX	I	UART 1 Receiver	101
UART1_TX	O	UART 1 Transmitter	102
PM UART 1 Mode			
UART1_RX	I	UART 1 Receiver	63
UART1_TX	O	UART 1 Transmitter	64
FUART Mode1			
FUART_RX	I	Fast UART Receiver	90
FUART_TX	O	Fast UART Transmitter	91

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
FUART_CTS	I	Fast UART Clear to Send	92
FUART_RTS	O	Fast UART Request to Send	93
FUART Mode2			
FUART_RX	I	Fast UART Receiver	99
FUART_TX	O	Fast UART Transmitter	100
FUART_CTS	I	Fast UART Clear to Send	101
FUART_RTS	O	Fast UART Request to Send	102
FUART Mode3			
FUART_RX	I	Fast UART Receiver	90
FUART_TX	O	Fast UART Transmitter	91
FUART_CTS	I	Fast UART Clear to Send	92
FUART_RTS	O	Fast UART Request to Send	104
FUART Mode4			
FUART_RX	I	Fast UART Receiver	3
FUART_TX	O	Fast UART Transmitter	2
FUART_CTS	I	Fast UART Clear to Send	7
FUART_RTS	O	Fast UART Request to Send	6
FUART Mode5			
FUART_RX	I	Fast UART Receiver	90
FUART_TX	O	Fast UART Transmitter	91
FUART Mode6			
FUART_RX	I	Fast UART Receiver	3
FUART_TX	O	Fast UART Transmitter	2
SPI 0 Mode1			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	13
SPI0_CK	O	Master SPI 0 Serial Clock	14
SPI0_DI	O	Master SPI 0 Serial Data In (MOSI)	15
SPI0_DO	I	Master SPI 0 Serial Data Out (MISO)	16
SPI 0 Mode2			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	99
SPI0_CK	O	Master SPI 0 Serial Clock	100
SPI0_DI	O	Master SPI 0 Serial Data In (MOSI)	101

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
SPI0_DO	I	Master SPI 0 Serial Data Out (MISO)	102
SPI 0 Mode3			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	90
SPI0_CK	O	Master SPI 0 Serial Clock	91
SPI0_DI	O	Master SPI 0 Serial Data In (MOSI)	92
SPI0_DO	I	Master SPI 0 Serial Data Out (MISO)	93
SPI 0 Mode4			
SPI0_CZ	O	Master SPI 0 Chip Select (Active Low)	3
SPI0_CK	O	Master SPI 0 Serial Clock	2
SPI0_DI	O	Master SPI 0 Serial Data In (MOSI)	7
SPI0_DO	I	Master SPI 0 Serial Data Out (MISO)	6
SPI 1 Mode3			
SPI1_CZ	O	Master SPI 1 Chip Select (Active Low)	22
SPI1_CK	O	Master SPI 1 Serial Clock	23
SPI1_DI	O	Master SPI 1 Serial Data In (MOSI)	24
SPI1_DO	I	Master SPI 1 Serial Data Out (MISO)	25
SPI 1 Mode4			
SPI1_CZ	O	Master SPI 1 Chip Select (Active Low)	95
SPI1_CK	O	Master SPI 1 Serial Clock	96
SPI1_DI	O	Master SPI 1 Serial Data In (MOSI)	97
SPI1_DO	I	Master SPI 1 Serial Data Out (MISO)	98
PWM Mode1			
PWM0	O	PWM 0 Output	17
PWM1	O	PWM 1 Output	18
PWM2	O	PWM 2 Output	103
PWM3	O	PWM 3 Output	104
PWM4	O	PWM 4 Output	7
PWM5	O	PWM 5 Output	6
PWM6	O	PWM 6 Output	5
PWM7	O	PWM 7 Output	4

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
PWM8	O	PWM 8 Output	95
PWM9	O	PWM 9 Output	96
PWM10	O	PWM 10 Output	97
PWM Mode2			
PWM0	O	PWM 0 Output	103
PWM1	O	PWM 1 Output	104
PWM2	O	PWM 2 Output	92
PWM3	O	PWM 3 Output	93
PWM4	O	PWM 4 Output	13
PWM5	O	PWM 5 Output	14
PWM6	O	PWM 6 Output	15
PWM7	O	PWM 7 Output	16
PWM9	O	PWM 9 Output	17
PWM10	O	PWM 10 Output	18
PWM Mode3			
PWM0	O	PWM 0 Output	90
PWM1	O	PWM 1 Output	91
PWM2	O	PWM 2 Output	3
PWM3	O	PWM 3 Output	2
PWM4	O	PWM 4 Output	99
PWM5	O	PWM 5 Output	100
PWM6	O	PWM 6 Output	101
PWM7	O	PWM 7 Output	102
PWM9	O	PWM 9 Output	103
PWM10	O	PWM 10 Output	104
PWM Mode4			
PWM0	O	PWM 0 Output	95
PWM1	O	PWM 1 Output	96
PWM2	O	PWM 2 Output	97
PWM3	O	PWM 3 Output	98
PWM4	O	PWM 4 Output	6
PWM5	O	PWM 5 Output	5
PWM6	O	PWM 6 Output	4

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
PWM7	O	PWM 7 Output	8
PWM8	O	PWM 8 Output	125
PWM9	O	PWM 9 Output	126
PWM10	O	PWM 10 Output	127
PWM Mode5			
PWM0	O	PWM 0 Output	3
PWM1	O	PWM 1 Output	2
PWM2	O	PWM 2 Output	7
PWM3	O	PWM 3 Output	6
PM PWM Mode1			
PWM0	O	PWM 0 Output	59
PWM1	O	PWM 1 Output	60
PWM2	O	PWM 2 Output	61
PWM3	O	PWM 3 Output	63
PWM4	O	PWM 4 Output	74
PWM5	O	PWM 5 Output	75
PWM8	O	PWM 8 Output	67
PWM9	O	PWM 9 Output	74
PWM10	O	PWM 10 Output	75
PM PWM Mode2			
PWM2	O	PWM 2 Output	67
PWM3	O	PWM 3 Output	65
RGB 565			
TTL_R3	O	Parallel LCD Data R3	59
TTL_R4	O	Parallel LCD Data R4	60
TTL_R5	O	Parallel LCD Data R5	61
TTL_R6	O	Parallel LCD Data R6	63
TTL_R7	O	Parallel LCD Data R7	64
TTL_G2	O	Parallel LCD Data G2	90
TTL_G3	O	Parallel LCD Data G3	91
TTL_G4	O	Parallel LCD Data G4	92
TTL_G5	O	Parallel LCD Data G5	95
TTL_G6	O	Parallel LCD Data G6	96

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Signal Name	Signal Type	Function (QFN128)	QFN128 (12.3 x 12.3) Pin Location
TTL_G7	O	Parallel LCD Data G7	97
TTL_B3	O	Parallel LCD Data B3	98
TTL_B4	O	Parallel LCD Data B4	99
TTL_B5	O	Parallel LCD Data B5	100
TTL_B6	O	Parallel LCD Data B6	101
TTL_B7	O	Parallel LCD Data B7	102
TTL_PCLK	O	Parallel LCD Pixel Clock	103
TTL_VS	O	Parallel LCD Vertical Sync	104
TTL_HS	O	Parallel LCD Horizontal Sync	105
TTL_DE	O	Parallel LCD Data Enable	106

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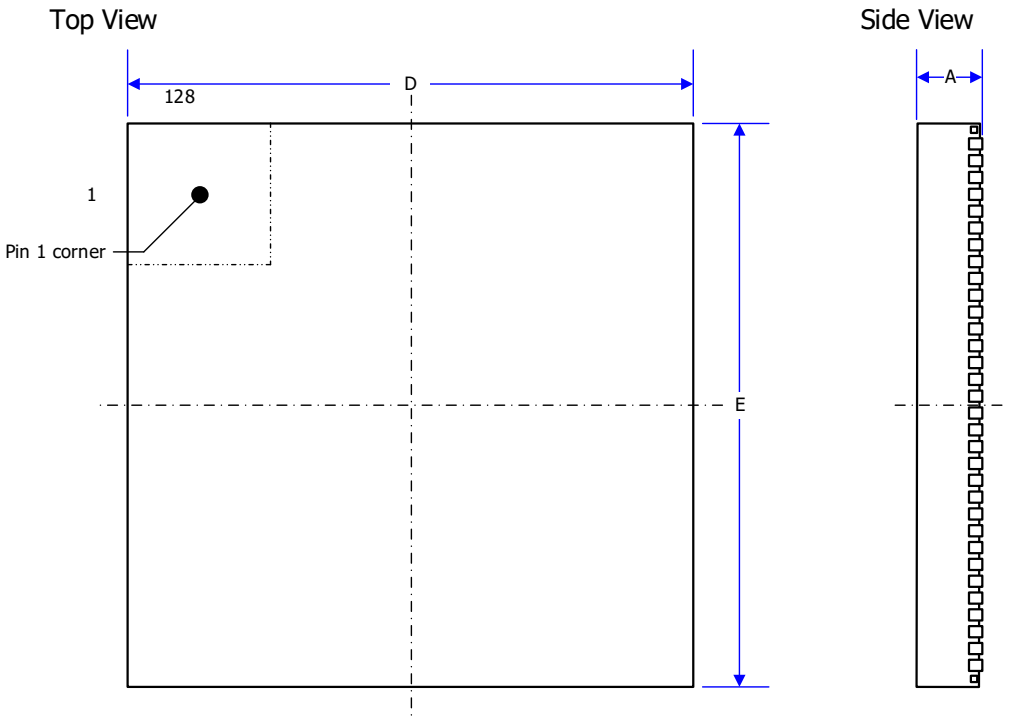
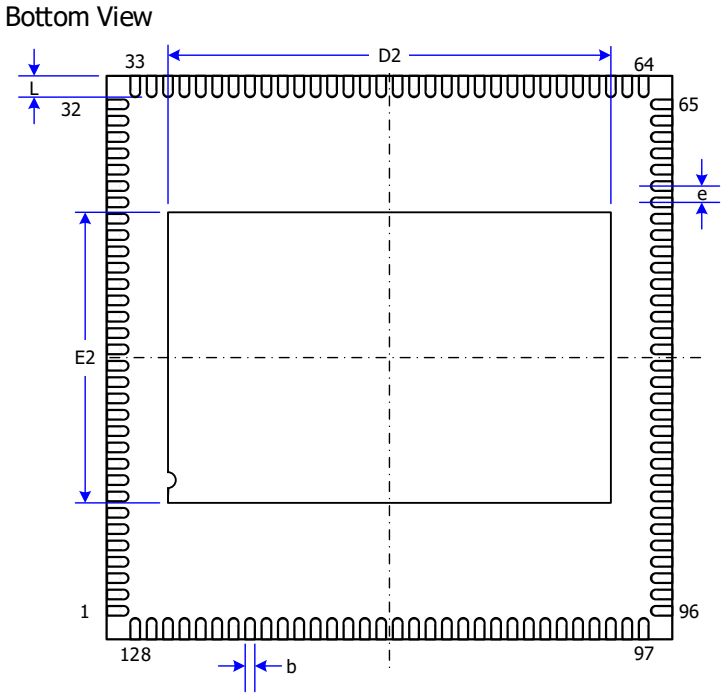
MECHANICAL DIMENSIONS





Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	0.90	0.031	0.033	0.035
D	12.20	12.30	12.40	0.480	0.484	0.488
E	12.20	12.30	12.40	0.480	0.484	0.488
D2	9.40	9.50	9.60	0.370	0.374	0.378
E2	6.10	6.20	6.30	0.240	0.244	0.248
b	0.10	0.15	0.20	0.004	0.006	0.008
e	--	0.35	--	--	0.014	--
L	0.30	0.40	0.50	0.012	0.016	0.020

Note: E-pad has to connect to system GND net.

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ELECTRICAL SPECIFICATIONS

Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	V_{IH}	2.5			V
Input Voltage, Low	V_{IL}			0.8	V
Input Current, High	I_{IH}			-1.0	uA
Input Current, Low	I_{IL}			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	V_{OH}	VDDP-0.1[Note]			V
Output Voltage, Low	V_{OL}			0.1	V
SAR ADC Input		0		V_{VDD_33}	V
AUDIO OUTPUTS					
Line-Out			2.54		Vp-p
XTAL Specifications					
Input Voltage, High	V_{IH}	2.0		3.6	V
Input Voltage, Low	V_{IL}	-0.3		0.8	V
Clock frequency			24		MHz
Crystal accuracy			+/-30		ppm
Long-term jitter			+/-500		ps

Note: 1. VDDP can be V_{VDD_33}, V_{VDD_15}

2. 0.9Vrms @10Kohm load

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}	3.14	3.3	3.46	V
1.5V Supply Voltage (DDR III)	V_{VDD_15}	1.45	1.5	1.55	V
Core Power Supply Voltage (Core)	V_{VDD_core}	0.87	0.9	0.93	V
Ambient Operation Temperature	T_A	-20		70	°C
Junction Temperature	T_J			125	°C

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}	2.97	3.30	3.63	V
1.5V Supply Voltage (DDR III)	V_{VDD_15}	1.35	1.5	1.65	V
Core Power Supply Voltage (Core)	V_{VDD_core}			1.26	V
Storage Temperature	T_{STG}	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

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HARDWARE POWER SEQUENCE PROCEDURE

The timing requirements of the hardware reset signal are shown as below:

Hardware Reset

HWRESET: Chip Reset; High Reset (Level)

The HWRESET pin is suggested to connect with 3.3V standby as shown in Figure 1. The VIH is 2V (Typ) +/- 10% (2.2V~1.8V); the VIL is 1.2V (Typ) +/- 10% (1.08V~1.32V). The power sequence is as shown in Figure 2.

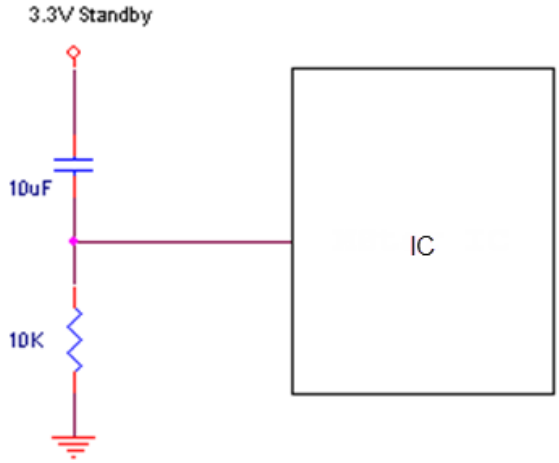

Figure 1: Reset Application Circuit

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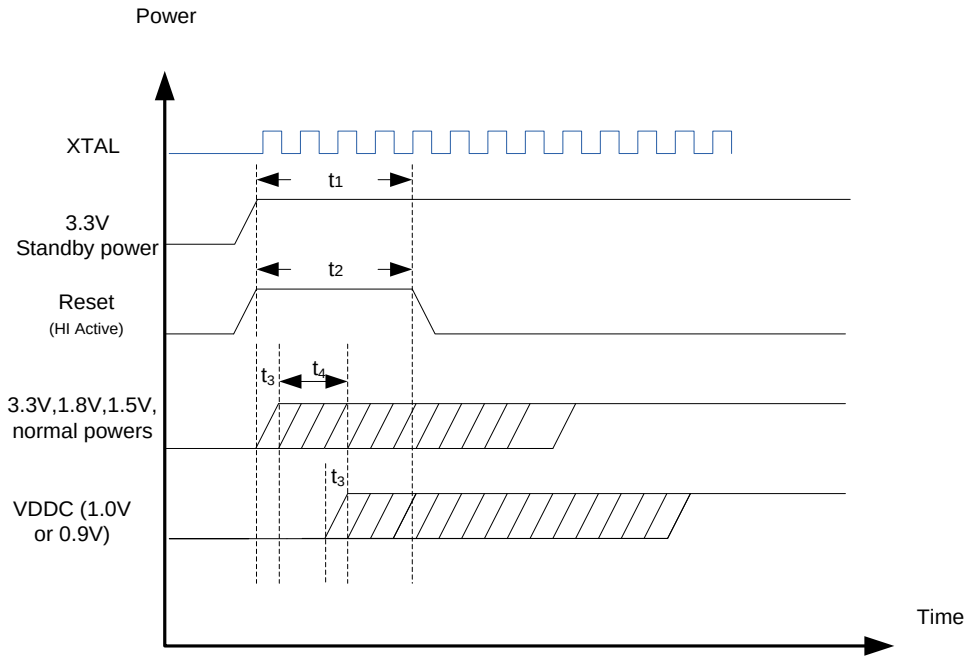
External Reset IC with External LDO

The timing is shown as Figure 2. The RST and power waveform must satisfy Figure 2 with parameters listed in Table 1.



Note:

***3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)**

***1.0V/0.9V (VDD, DVDD_DDR_RX)**

***1.5V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD)**

***1.8V (VDDP_2)**

***3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)**

Figure 2: Power on Sequence

Table 1: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	XTAL stable to Reset falling	5	—	—	ms
t_2	Reset pulse width	5	—	—	ms
t_3	Normal 3.3V, 1.8V, 1.5V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t_4	Normal 3.3V, 1.8V, and 1.5V to VDDC lead time	1	—	—	ms

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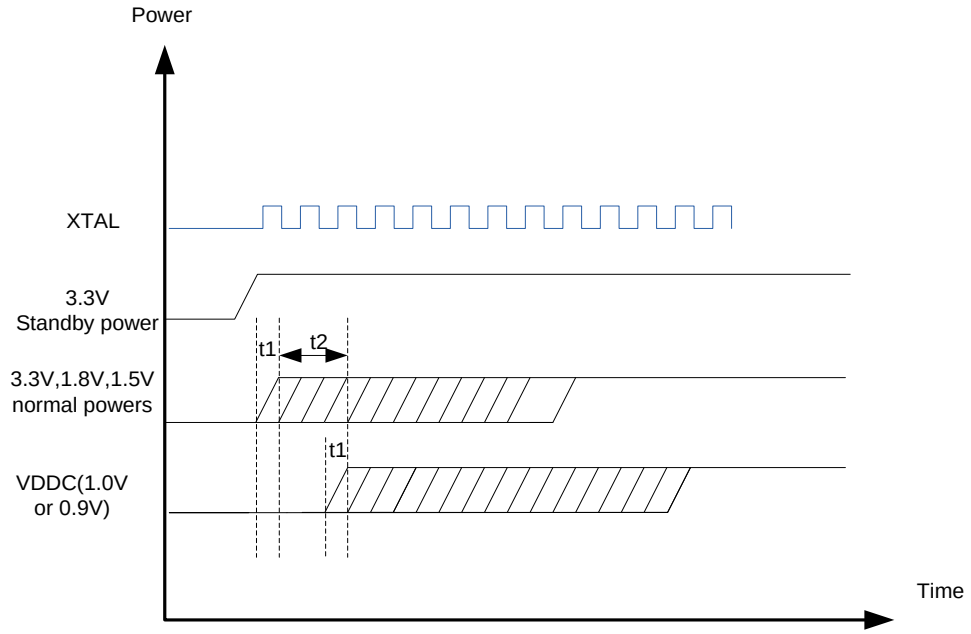
Without External Reset IC with External LDO

The timing is shown as Figure 3. The power waveform must satisfy Figure 3 with parameters listed in Table 1.



Note:

***3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)**

***1.0V/0.9V (VDD, DVDD_DDR_RX)**

***1.5V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD)**

***1.8V (VDDP_2)**

***3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)**

Figure 3: Power on Sequence

Table 2: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	Normal 3.3V, 1.8V, 1.5V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t_2	Normal 3.3V, 1.8V, and 1.5V to VDDC lead time	1	—	—	ms

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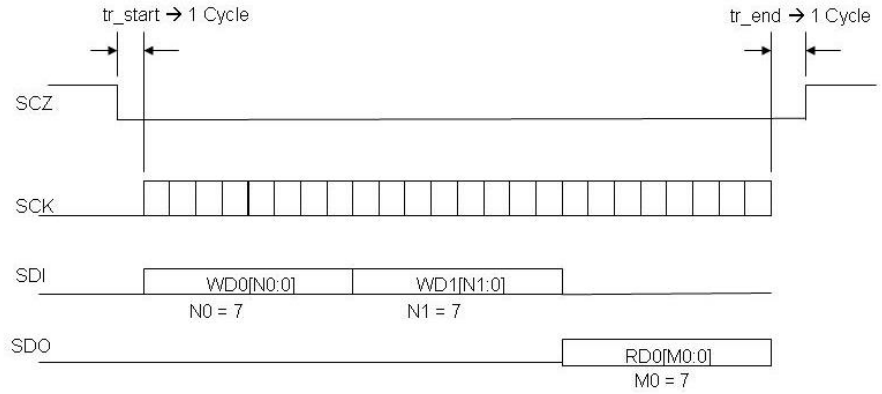
MSPI OPERATION EXAMPLE

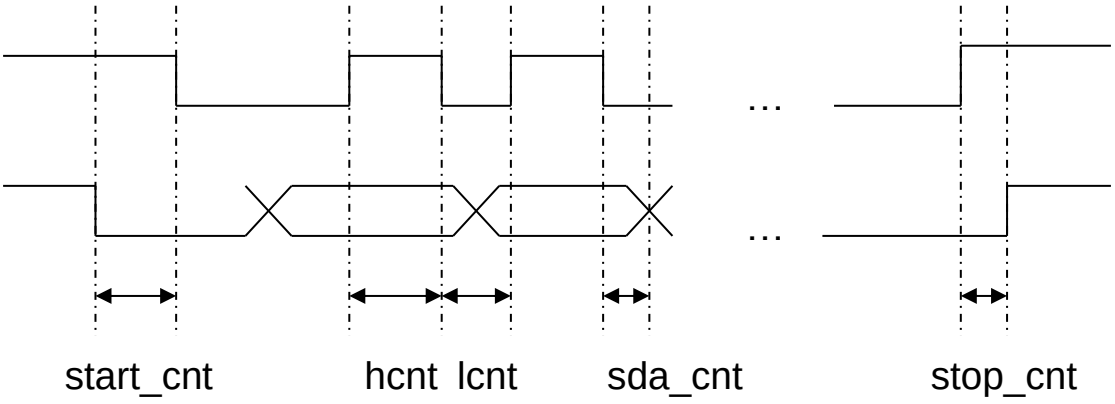
This section describes an example of MSPI operation.

(0). Initial
(1). CS goes low
(2). Write 2Bytes data
(3). Read 1Bytes data
(4). CS goes high



I2C clock frequency configurable is between 100Khz ~ 400Khz

Set MIIC Speed



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clk_miic	12MHz	24MHz
lcnt (>1.3us)	>16T	>31T
hcnt (>0.6us)	>8T	>15T
start (>0.6us)	>8T	>15T
stop (>0.6us)	>8T	>15T
between start and stop (>1.3us)	>16T	>31T
data_latch (>0us)	>0T	>0T
sda change (<0.9us)	<11T	<22T

Register name	Address	Description
reg_stop_cnt	'h08[15:0]	Sets the SCL and SDA count for stop
reg_hcnt	'h09[15:0]	Sets the SCL clock high-period count
reg_lcnt	'h0a[15:0]	Sets the SCL clock low-period count
reg_sda_cnt	'h0b[15:0]	Sets the clock count between falling edge SCL and SDA
reg_start_cnt	'h0c[15:0]	Sets the SCL and SDA count for start
reg_data_lat_cnt	'h0d[15:0]	Sets the data latch timing

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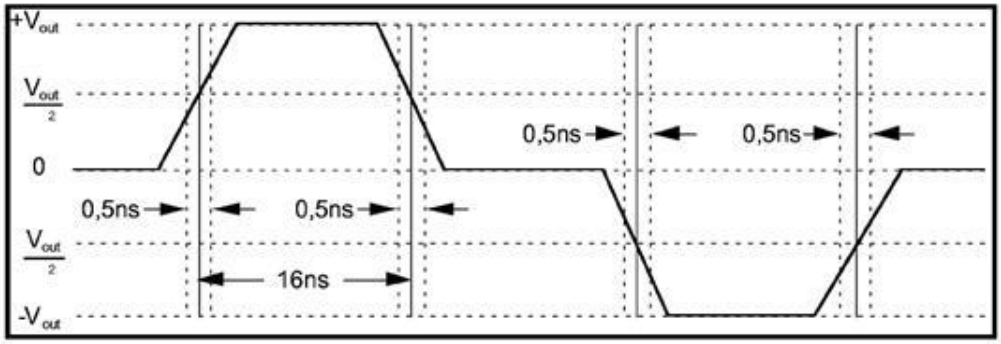
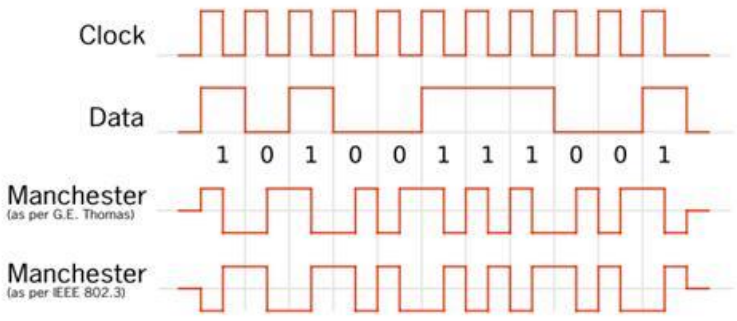
EPHY INTERFACE

Parameter	Min	Typ	Max	Unit
ETHERNET ANALOG INTERFACE (10BASE-T)				
Analog Input Range	4.4	5	5.6	Vdp-p
Differential Input Impedance		100		ohm
ETHERNET ANALOG INTERFACE (100BASE-TX)				
Analog Input Range	1.9	2	2.1	Vdp-p
Differential Input Impedance		100		ohm
Rise/Fall Time	3	4	5	ns
Rise/Fall Time Symmetry			0.5	ns
Duty Cycle Distortion	-0.25		0.25	ns
Amplitude Symmetry	98	100	102	%
Overshoot			5	%

100BASE-TX



10BASE-T



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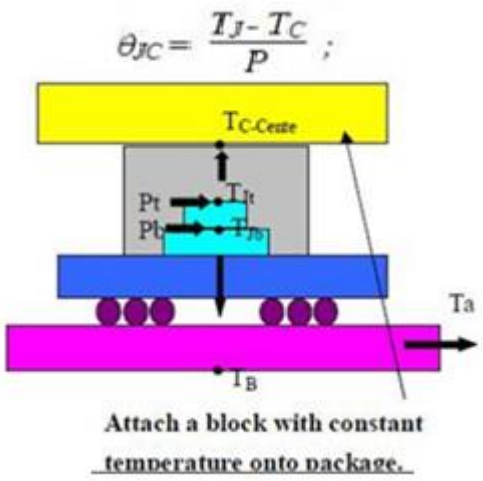
THERMAL RESISTANCE (°C/W)

Thermal simulation mode

PCB condition: JEDEC JESD51-5
PCB layers: 4 (2S2P)
PCB dimensions: 76.2 x 114.3 (mm x mm)
PCB thickness: 1.6 (mm)

Part Number	Manufacture/ Vendor	Package		Thermal Resistance (°C/W)		
			PCB Layer	θ_{JA}	θ_{JC}	θ_{JB}
SSC337DE		QFN128_12.3x12.3	4L PCB	19.8	6.5	5.56



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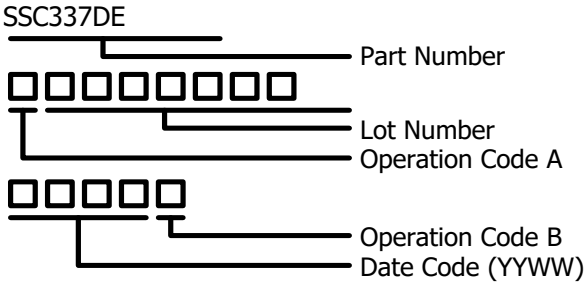
ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
SSC337DE	-20°C to +70°C	QFN	128-pin

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. SSC337DE comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

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