MSC318
High-Integrated IP Camera SoC Processor

Preliminary Product Brief Version 0.3

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REVISION HISTORY

Revision No.	Description	Date
Draft	Ÿ Initial release	11/15/2016
0.1	Ÿ Updated for clarity	01/16/2017
0.2	Ÿ Updated Electrical Specifications	04/13/2017
0.3	Ÿ Updated I2S Description Ÿ Updated Electrical Specifications	05/05/2017

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FEATURES

- High Performance Processor Core
  - ARM Cortex-A7 Single Core
  - Neon and FPU
  - Memory Management Unit for Linux support
  - DMA Engine
- Image/Video Processor
  - Supports 10/12-bit parallel interface for raw data input
  - Supports MIPI interface with 2 data lanes and 1 clock lane
  - Supports 8/10-bit CCIR656 interface
  - Supports 5M (2560x2048) pixels video recording and image snapshot
  - Bad pixel compensation
  - Noise Reduction (NR)
  - Optical black correction
  - Lens shading compensation
  - Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
  - CFA color interpolation
  - Color correction
  - Gamma correction
  - Video stabilization
  - Wide Dynamic Range (WDR)
  - Rotation with 90 or 270 degree
  - Lens distortion correction
  - Fully programmable multi-function scaling engines
- MStar Advanced Color Engine (MStarACE)
  - Luma gain/offset adjustment
  - Supports 2D peaking
  - Horizontal noise masking
  - Direct Luma Correction (DLC)
  - Black/White Level Extension (BLE/WLE)
  - IHC/ICC/IBC for chroma adjustment
  - Histogram statistics
- H.265/HEVC Encoder
  - Supports H.265/HEVC baseline and main profile encoding
  - Supports MVs: 32x32, 16x16, 8x8
  - Supports up to quarter-pixel
  - Supports one reference frame
  - Supports Max. 3Mp/30fps or 5Mp/15fps encoding
- H.264 Encoder
  - Supports H.264 baseline and main profile encoding
  - Supports MVs: 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, 4x4
  - Supports up to quarter-pixel
  - Supports two reference frames
  - Supports rate control and ROI
  - Supports Max. 3Mp/25fps or 5Mp/15fps encoding
- JPEG Encoder
  - Supports JPEG baseline encoding
  - Supports YUV422 or YUV420 formats
  - Supports Max. 5Mp6fps encoding
- Video Encoding Performance
  - Supports 3Mp30 + VGAp30 + QCIFp30 H.265/HEVC or H.264 encoding
  - Supports 5Mp15 + D1p15 + QCIFp15 H.265/HEVC or H.264 encoding
  - Supports MJPEG up to 5Mp6fps encoding
- Audio Processor
  - One stereo ADC for microphone inputs
  - One stereo DAC for lineouts
  - Supports 8K/16K/32KHz sampling rate audio recording
  - Digital and analog gain adjustment
  - I2S digital audio input
- NOR Flash Interface
  - Compliant with standard, dual and quad SPI Flash memory components

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- NAND Flash and SD Card Interface
  - Supports SLC NAND Flash (8-bit interface, and 8-bit ECC)
  - Compatible with SD spec. 2.0, data bus 1/4 bit mode
- SDIO 2.0 Interface
  - Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
  - Compatible with SD spec. 2.0, data bus 1/4 bit mode
- USB 2.0 Interface
  - One USB 2.0 configurable host or device
    - Host mode supports EHCI specification
    - Device mode supports 7 endpoints
  - One USB2.0 host
- DRAM Memory
  - Support external 16bit DDR interface
- Connectivity
  - Built-in 10/100M Ethernet MAC and Ethernet PHY
  - Two USB 2.0 Host Controller could be used for USB Wi-Fi Dongle or Module
  - One SDIO 2.0 Host Controller could be used for SDIO Wi-Fi module
  - Supports Wakeup on LAN (WOL)
- Security Engines
  - Supports AES/DES/TDES
  - Supports secure booting
- Real Time Clock (RTC)
  - Built-in RTC working with 32.768 KHz crystal
  - Alarm interrupt for wakeup
  - Tick time interrupt (millisecond)
  - Built-in regulator
- Peripherals
  - Dedicated GPIOs for system control
  - Support 8 PWM outputs
  - Two generic UARTs and one fast UART with flow control
  - Three generic timers and one watchdog timer
  - Two SPI masters
  - Two I2C Masters
  - Built-in SAR ADC with 3 channels analog inputs for different kinds of applications
  - One IR input
- Operating Voltage Range
  - Core: 0.9V
  - I/O: 1.8 ~ 3.3V
  - DRAM: 1.5V
  - Power Consumption: TBD
- Package
  - BGA, 12mmx12mm

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GENERAL DESCRIPTIONS

The MSC318 is a highly integrated SOC. Based on ARM Cortex-A7, it integrates Image Signal Processor (ISP), Color Engine, Video (H.264/H.265/MJPEG) Encoders and other useful peripherals for IP camera applications.

A typical utilization of the MSC318 application processor is demonstrated in the following block diagram. The complete system includes a camera module (CMOS sensor), a connectivity module (WiFi or Ethernet), and a non-volatile storage (NOR flash, NAND flash or SD card). External crystal of 32KHz frequency is used to drive the Real Time Clock (RTC), which can keep time scale when the main system clock is off. The ISP and Color Engine handle images captured from the camera sensor, and the video stream is composed of lots images. There are pre- and post- video processing stages. The pre-video processing rotates images, reduces noises, enhances signals and translates color domains. The post-video processing corrects lens distortion, adjusts color quality, and generates multiple video streams with different resolutions. Multimedia Encoders can compress those video streams with different compressing standards at the same time. The well compressed video/audio streams could be streamed or stored in the cloud server through Wi-Fi or Ethernet or stored in a local SD Card. The NOR or NAND flash is usually reserved for operating system and application software. Moreover, other peripherals like SAR ADC, Audio ADC/DAC, UARTs, PWMs, GPIOs and SPI are supported to realize applications with maximal flexibility.

Besides, the MSC318 supports secure booting and personalization authentication mechanism for securing system. The AES/DES/3DES cipher engines could also help encrypt the compressed video/audio streams to protect privacy.

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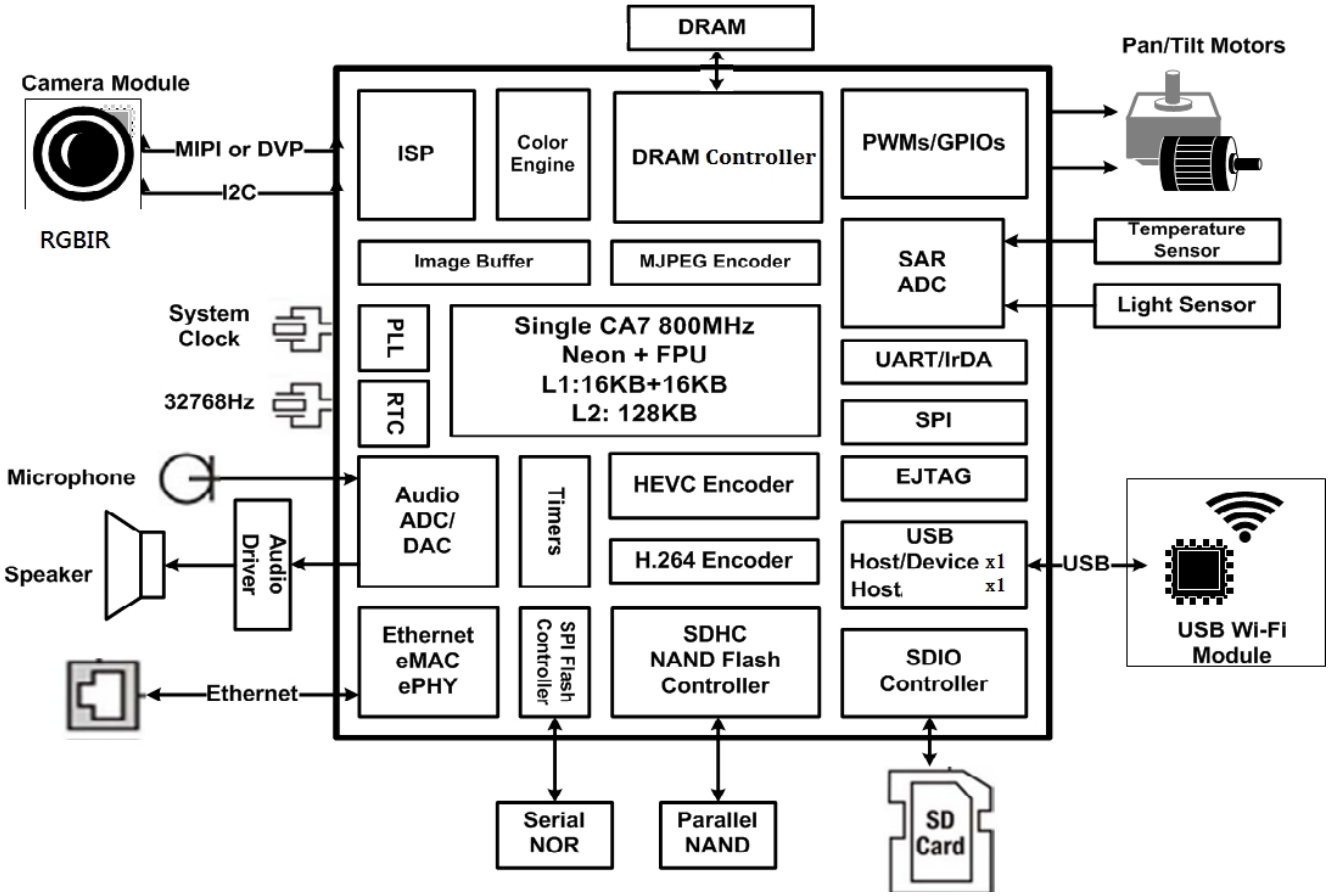
BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Video Encoder

I. JPE Feature Description

JPE features:

- Supports JPEG encoding 5M(2560x2048) @ 6fps
  - Frame mode
- IMI row mode
- Supports YUYV input format
- Supports NV12 input format
- Supports DCT mode to accelerate SW encoding

II. H264/H265 Feature Description

- H264 features
  - Supports H264 baseline encoding
  - Baseline profile, level 3.0
  - Supports MVs: 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, 4x4
  - Supports up to quarter-pel
  - Supports up to two reference frames
  - Max resolutions
  - H264 supported are 5M (2560x2048)
    - Other resolution: 4M (2688x1520)
  - frame-level & mb-level rate control
  - Supports YUYV input format
  - Supports NV12 input format
  - Supports 16/235 and 0/255 Range Converter
  - Supports cost-penalty adjustment
  - Supports force zero-motion
  - Supports intra16x16 planar mode
- H264 Stream combination
  - 5M@15fps+ D1@15fps
  - 4M@20fps+D1@20fps
  - 3M@25fps+CIF@25fps
  - 3M@25fps+D1@25fps
  - 2M@30fps+VGA@30fps+CIF@30fps
- H265 Stream combination
  - 5M@15fps+ D1@15fps
  - 4M@20fps+D1@20fps
  - 3M@30fps+CIF@30fps
  - 3M@25fps+D1@25fps
  - 2M@30fps+VGA@30fps+CIF@30fps

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ISP

I. Brief Feature Description

ISP design is used to transfer raw sensor data output to YUV data and also supports YUV sensor at ISP bypass mode default.

- Support to FHD@30Hz, 3M@30, 4M@20, 5M@15 sensor input
- Fix pattern noise correction
- Bad pixel compensation
- Green equal
- Support rgbir2x2 or rgbir4x4 mode input
- Optical black correction
- Len shading compensation
- Asymmetric Lens shading compensation
- Statistic for AWB/AE/AF
- Bayer domain de-noise
- Support Bayer domain rotation
- White Balance PreGain and PostGain can be enable at the same time.
- CFA color interpolation
- Gamma correction
- Video stabilization statistic
- Support menuload for ALSC_gain/DefectPxl/Gamma table

Peripheral

I. USB Brief Feature Description

One port of host/OTG controller and one port of host only controller, are fully compliant with the USB 2.0 specification and the Enhanced Host Controller Interface (EHCI) specification. This Host/OTG Controller can support FS/LS transactions, Interrupt/Control/Bulk transfers and split/preamble transactions for hub.

II. MIPI CSI Interface

The features are listed below:

- CSI-2 1.1/D-PHY 1.1 compliant receiver with maximum Input Frequency 1GHz
- Supports 1 clock lane, 2 data lanes
- Supports YUV422 8-bit, Raw8, Raw10, Raw12, Generic 8-bit long packet and User defined byte-based data type
- Supports 1-bit error correction/2-bit error detection for packet header
- Supports checksum error detection for payload data
- Supports timing generation for Vsync and Hsync

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III. Ethernet MAC Brief Feature Description

- IEEE Std 802.3 compatible
- Support 10/100 Mbit/s operation.
- Full/Half duplex support.
- Automatic pad and CRC generation on transmitted packet.
- Supports transmit packet(IP/TCP/UDP) checksum generate
- Receiver & Transmitter Packet management by internal storage with descriptor header control
- Internal async-FIFO for receiver & transmitter frame wire speed operation
- Supports Tagged frame
- Supports IPV6 check-sum
- Supports IEEE802.3az EEE function

IV. EPHY Brief Feature Description

The Ethernet PHY (EPHY) is an IEEE 802.3 compliant single-port Ethernet Transceiver for both 100Mbps and 10Mbps operations. EPHY acts as an interface between physical signaling and Media Access Controller (MAC). It supports Auto-Negotiation function to simplify the network installation and maintenance.

The major functions of EPHY included:

- 10/100Mbps TX/RX
- Full-duplex or half duplex
- Supports IEEE 802.3u auto-negotiation
- DSP-based PHY Transceiver technology
- Supports WOL (Wake on Lan) feature (Magic Packet only)
- Supports IEEE 802.3az EEE function

V. Encryption Brief Feature Description

AESDMA is a secure IP for Secure Boot and HDMI Key Authentication. There are three engines inside this IP:

- AES: ECB, CBC (dvs042), ECB_CTS, CBC_CTS, CTR
- SHA: SHA_1, SHA_256
- RSA: RSA_2048 in HW key mode, programmable size in SW key mode

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BALL ASSIGNMENT (MSC318)

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		AUD_LINEOUT_R0		AUD_MICCM1	AUD_MICCM0	AUD_VAG		DM_P1	USB_DM	SD_D2			UART0_TX	NAND_DA7		NAND_DA2	NAND_DA0		A
B	IO[1] A0	GND	AUD_LINEOUT_L0	AUD_MICIN1	AUD_MICIN0	AUD_VRM_DAC	GND	DP_P1	USB_DP	SD_D3	SD_CLK	SD_D1	UART1_RX	NAND_DA6	NAND_DA4	NAND_DA1	NAND_REZ	NAND_CEZ	B
C	IO[9] A9	IO[0] A2	GND	GND	GND	AUD_VRM_ADC	GND	GND	GND	SD_CMD	SD_D0	UART1_TX	UART0_RX	NAND_DA5	NAND_DA3	NAND_REZ	NAND_CLE	NAND_ALE	C
D	IO[4] A7	IO[7] A13	IO[26] CKE	IO[5] A14	GND	AVDD_AUD	USB_VBUS	AVDD_USB	GND	USB_CID	SPI1_CZ	PWM0	PWM1	SPI0_CK	SPI0_CZ	NAND_WEZ	NAND_WPZ		D
E	GND	IO[3] RESETZ	IO[6] A11	IO[8] A8	GND			GND	GND	SPI1_DO	SPI1_DI	SPI1_CK	SPI0_DI	SPI0_DO	GND		SR_IO15	SR_IO13	E
F	IO[11] A3	IO[10] A5	IO[13] A6	IO[12] A4	GND	GND	VDDIO_CMD	GND	GND	GND	GND	GND	GND		SR_IO12	SR_IO16	SR_IO14		F
G	IO[15] BA0	IO[14] BA2	IO[17] A1	IO[16] A12	GND	GND	VDDIO_CMD	VDDIO_CMD	GND	GND	VDD	VDD		GND	VDDP_3	SR_IO10	SR_IO17	SR_IO11	G
H	GND	IO[18] WEZ	IO[19] A15	IO[23] ODT		GND	VDDIO_DATA	VDDIO_DATA		GND	VDD	VDD	VDD	VDD	VDDP_2		GND	SR_IO09	H
J	GND	IO[24] CSB0	IO[21] RASZ	IO[20] BA1		GND	VDDIO_DATA	VDDIO_DATA		DVDD_DDR_RX	GND	VDD	VDD	VDD	VDDP_1	GND	SR_IO08	SR_IO07	J
K	IO[28] MCLK	IO[27] MCLKZ	IO[22] A10	IO[25] CASZ		GND	VDDIO_DATA	AVDD_PLL		DVDD_DDR	GND	VDD	VDD	VDD	GND		SR_IO06	SR_IO05	K
L	IO[29] DQ[4]	GND	IO[41] DQ[11]	IO[39] DQ[8]	GND	GND	GND	GND		GND	GND	VDD	VDD	VDD	GND	GND	SR_IO04	SR_IO03	L
M	IO[30] DQ[2]	IO[31] DQ[6]	IO[42] DQ[9]	IO[44] DQM[1]	GND	GND		DVDD_NODIE	AVDD_NODIE		GND	GND	GND	GND	GPIO5	SR_IO01	SR_IO02	GND	M
N	GND	IO[32] DQ[0]	IO[43] DQ[10]	IO[45] DQS[1]	GND		SAR_GPIO3	PM_GPIO0	PM_SPI_WPZ	PM_SPI_CK	GND	PM_LED1	PM_LED0	I2C0_SCL	GPIO4	I2C1_SDA	SR_IO00		N
P	IO[34] DQSB[0]	IO[33] DQS[0]	GND	IO[46] DQSB[1]	GND	GND	SAR_GPIO2	PM_GPIO1	PM_GPIO3	PM_SPI_HLD	GND_EFUSE		AVDD_ETH	I2C0_SDA	GPIO3	GPIO2	FUART_RTS	I2C1_SCL	P
R	IO[35] DQ[5]	IO[37] DQ[7]	IO[48] DQ[12]	IO[50] DQ[13]	GND	SAR_GPIO1	SAR_GPIO0		PM_GPIO2	GND	AVDD_XTAL	SE_XTAL_OUT	GND	GPIO0	GPIO1	GPIO15	FUART_CTS	FUART_TX	R
T	IO[36] DQ[3]	IO[38] DQ[1]	IO[47] DQ[14]	IO[49] DQ[15]	PM_UART_TX	PM_GPIO4	PM_GPIO6	PM_GPIO7	PM_SPI_CZ	GND	GND	GND	ETH_RP	GND	GPIO7	GPIO10	GPIO13	FUART_RX	T
U	GND	IO[40] DQM[0]	PM_RESET	RTC_OUT	GND	PM_UART_RX	PM_GPIO5	PM_GPIO10	PM_GPIO9	PM_SPI_DO	XTAL_OUT		ETH_RN	ETH_TN	GPIO6	GPIO8	GPIO12	GPIO14	U
V		PM_IRIN	PM_SD_CDZ	GND	RTC_IN			PM_GPIO8		PM_SPI_DI	XTAL_IN			ETH_TP		GPIO9	GPIO11		V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

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BALL CHARACTERISTICS

Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
U4	PAD_RTC_OUT	RTC_OUT	AVDD_NODIE				
V5	PAD_RTC_IN	RTC_IN	AVDD_NODIE				
N7	PAD_SAR_GPIO3	SAR_ASI3 SAR_GPIO[3]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
P7	PAD_SAR_GPIO2	SAR_ASI2 SAR_GPIO[2]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
R6	PAD_SAR_GPIO1	SAR_ASI1 SAR_GPIO[1]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
R7	PAD_SAR_GPIO0	SAR_ASI0 SAR_GPIO[0]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
V3	PAD_PM_SD_CDZ	SD_CDZ SD_CDZ_GPIO	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
V2	PAD_PM_IRIN	IRIN IRIN_GPIO	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U3	PAD_PM_RESET	HW_RESET	AVDD_NODIE		PD=64kohm (±15%)/52uA(±15%)	PD	Yes
U6	PAD_PM_UART_RX	UART_RX	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T5	PAD_PM_UART_TX	UART_TX	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
N8	PAD_PM_GPIO0	PWM0 GPIO_PM[0]	AVDD_NODIE	>4mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
P8	PAD_PM_GPIO1	PWM1 GPIO_PM[1]	AVDD_NODIE	>4mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
R9	PAD_PM_GPIO2	PWM2 GPIO_PM[2]	AVDD_NODIE	>4mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
P9	PAD_PM_GPIO3	PWM3 GPIO_PM[3]	AVDD_NODIE	>4mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
T6	PAD_PM_GPIO4	GPIO_PM[4]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U7	PAD_PM_GPIO5	PWM1 GPIO_PM[5]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T7	PAD_PM_GPIO6	PWM0 GPIO_PM[6]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T8	PAD_PM_GPIO7	GPIO_PM[7]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
V8	PAD_PM_GPIO8	SPI_CZ1 SPI_CZ2 GPIO_PM[8]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
U9	PAD_PM_GPIO9	PWM2 GPIO_PM[9]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U8	PAD_PM_GPIO10	PWM3 GPIO_PM[10]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T9	PAD_PM_SPI_CZ	SPI_CZ1 SPI_CZ2 SPI_GPIO[0]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
V10	PAD_PM_SPI_DI	SPI_DI SPI_GPIO[2]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
N9	PAD_PM_SPI_WPZ	SPI_WPZ SPI_GPIO[4]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U10	PAD_PM_SPI_DO	SPI_DO SPI_GPIO[3]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
N10	PAD_PM_SPI_CK	SPI_CK SPI_GPIO[1]	AVDD_NODIE	>4mA/8mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
P10	PAD_PM_SPI_HLD	SPI_HLDZ SPI_GPIO[5]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
N13	PAD_PM_LED0	ETH_LED0 LED_GPIO[0]	AVDD_NODIE	>4mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
N12	PAD_PM_LED1	ETH_LED1 LED_GPIO[1]	AVDD_NODIE	>4mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
V11	PAD_XTAL_IN	XTAL_IN	AVDD_XTAL				
R12	PAD_SE_XTAL_OUT	SE_XTAL_OUT	AVDD_XTAL				
U11	PAD_XTAL_OUT	XTAL_OUT	AVDD_XTAL				
U13	PAD_ETH_RN	ETH_RN ETH_GPIO[0]	AVDD_ETH				
T13	PAD_ETH_RP	ETH_RP ETH_GPIO[1]	AVDD_ETH				
U14	PAD_ETH_TN	ETH_TN ETH_GPIO[2]	AVDD_ETH				
V14	PAD_ETH_TP	ETH_TP ETH_GPIO[3]	AVDD_ETH				
R14	PAD_GPIO0	FUART_RX SPI1_CZ I2S_WCK GPIO[0]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
R15	PAD_GPIO1	FUART_TX SPI1_CK I2S_BCK GPIO[1]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
P16	PAD_GPIO2	FUART_CTS SPI1_DI I2S_SDI GPIO[2]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
P15	PAD_GPIO3	FUART_RTS SPI1_DO I2S_SDO GPIO[3]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
N15	PAD_GPIO4	UART0_RX DMIC_L GPIO[4]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
M15	PAD_GPIO5	UART0_TX DMIC_R GPIO[5]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U15	PAD_GPIO6	UART1_RX DMIC_CLK GPIO[6]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T15	PAD_GPIO7	UART1_TX ETH_COL GPIO[7]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U16	PAD_GPIO8	SPI0_CZ ETH_TXD1 GPIO[8]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
V16	PAD_GPIO9	SPI0_CK ETH_TXD0 GPIO[9]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T16	PAD_GPIO10	SPI0_DI ETH_TX_EN GPIO[10]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
V17	PAD_GPIO11	SPI0_DO ETH_TX_CLK GPIO[11]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U17	PAD_GPIO12	SPI1_CZ PWM0 ETH_RXD1 GPIO[12]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T17	PAD_GPIO13	SPI1_CK PWM1 ETH_RXD0 GPIO[13]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
U18	PAD_GPIO14	SPI1_DI PWM2 ETH_MDC GPIO[14]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
R16	PAD_GPIO15	SPI1_DO PWM3 ETH_MDIO GPIO[15]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
T18	PAD_FUART_RX	FUART_RX UART0_RX EJ_TCK SPI0_CZ PWM0 FUART_GPIO[0]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
R18	PAD_FUART_TX	FUART_TX UART0_TX EJ_TMS SPI0_CK PWM1 FUART_GPIO[1]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
R17	PAD_FUART_CTS	FUART_CTS UART1_RX EJ_TDO SPI0_DI PWM2 FUART_GPIO[2]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
P17	PAD_FUART_RTS	FUART_RTS UART1_TX EJ_TDI SPI0_DO PWM3 FUART_GPIO[3]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
N14	PAD_I2C0_SCL	I2C0_SCL SR_SCL I2C0_GPIO[0]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
P14	PAD_I2C0_SDA	I2C0_SDA SR_SDA I2C0_GPIO[1]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
P18	PAD_I2C1_SCL	I2C1_SCL SR_SCL I2C1_GPIO[0]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
N16	PAD_I2C1_SDA	I2C1_SDA SR_SDA I2C1_GPIO[1]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
N17	PAD_SR_IO00	I2C0_SCL I2C1_SCL SR_D[8] SR_PDN SR_D[0] SR_GPIO[0]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
M16	PAD_SR_IO01	I2C0_SDA I2C1_SDA SR_D[6] SR_VS SR_D[1] SR_GPIO[1]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
M17	PAD_SR_IO02	SR_D[9] SR_D[8] SR_D[4] SR_HS SR_D[2] CCIR_IN_D[0] SR_GPIO[2]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
L18	PAD_SR_IO03	SR_D[7] SR_D[6] SR_D[2] SR_D[0] SR_D[3] CCIR_IN_D[1] SR_GPIO[3]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
L17	PAD_SR_IO04	SR_PCK SR_D[4] SR_D[1] CCIR_IN_D[2] SR_GPIO[4]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
K18	PAD_SR_IO05	SR_D[1] SR_D[2] SR_D[0] SR_D[5] CCIR_IN_D[3] SR_GPIO[5]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
K17	PAD_SR_IO06	SR_D[0] SR_PCK SR_D[2] SR_D[3] SR_D[6] CCIR_IN_D[4] SR_GPIO[6]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
J18	PAD_SR_IO07	SR_D[3] SR_D[1] SR_PCK SR_D[9] SR_D[4] SR_D[7] CCIR_IN_D[5] SR_GPIO[7]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
J17	PAD_SR_IO08	SR_D[5] SR_D[0] SR_D[1] SR_D[3] SR_D[8] CCIR_IN_D[6] SR_GPIO[8]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
H18	PAD_SR_IO09	SR_D[4] SR_D[9] SR_D[7] SR_D[6] CCIR_IN_D[7] SR_GPIO[9]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
G16	PAD_SR_IO10	SR_D[6] SR_D[3] SR_D[5] SR_RST SR_MCK SR_D[10] CCIR_IN_D[8] SR_GPIO[10]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
G18	PAD_SR_IO11	SR_MCK SR_D[7] SR_D[3] SR_D[5] SR_D[11] CCIR_IN_D[9] SR_GPIO[11]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
F15	PAD_SR_IO12	SR_HS SR_RST SR_D[9] SR_VS SR_D[8] SR_PDN CCIR_IN_CLK SR_GPIO[12]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
E18	PAD_SR_IO13	SR_VS SR_D[5] SR_HS SR_D[9] SR_RST SR_GPIO[13]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
F17	PAD_SR_IO14	SR_D[8] SR_VS SR_PDN SR_D[10] SR_HS SR_GPIO[14]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
E17	PAD_SR_IO15	SR_D[2] SR_HS SR_MCK SR_D[11] SR_PCK SR_GPIO[15]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
F16	PAD_SR_IO16	SR_PDN SR_PCK SR_VS SR_GPIO[16]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
G17	PAD_SR_IO17	SR_RST SR_MCK SR_GPIO[17]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
C18	PAD_NAND_ALE	NAND_ALE TTL_R[2] NAND_GPIO[1]	VDDP_3	>4mA/8mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
C17	PAD_NAND_CLE	NAND_CLE TTL_R[3] EMMC_CLK SD_CLK NAND_GPIO[2]	VDDP_3	>4mA/8mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
B18	PAD_NAND_CEZ	NAND_CEZ TTL_R[4] EMMC_CMD SD_CMD NAND_GPIO[0]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
D16	PAD_NAND_WEZ	NAND_WEZ TTL_R[1] EMMC_DA[0] SD_D[0] NAND_GPIO[3]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
D17	PAD_NAND_WPZ	NAND_WPZ TTL_R[0] EMMC_DA[1] SD_D[1] NAND_GPIO[4]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
B17	PAD_NAND_REZ	NAND_REZ TTL_R[5] EMMC_DA[2] SD_D[2] NAND_GPIO[5]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
C16	PAD_NAND_RBZ	NAND_RBZ TTL_R[6] EMMC_DA[3] SD_D[3] NAND_GPIO[6]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
A17	PAD_NAND_DA0	NAND_DA[0] TTL_R[7] EMMC_RSTn NAND_GPIO[7]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
B16	PAD_NAND_DA1	NAND_DA[1] TTL_G[0] NAND_GPIO[8]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
A16	PAD_NAND_DA2	NAND_DA[2] TTL_G[1] PWM2 NAND_GPIO[9]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
C15	PAD_NAND_DA3	NAND_DA[3] TTL_G[2] PWM3 NAND_GPIO[10]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
B15	PAD_NAND_DA4	NAND_DA[4] TTL_G[3] EMMC_DA[4] PWM4 NAND_GPIO[11]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
C14	PAD_NAND_DA5	NAND_DA[5] TTL_G[4] EMMC_DA[5] PWM5 NAND_GPIO[12]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
B14	PAD_NAND_DA6	NAND_DA[6] TTL_G[5] EMMC_DA[6] PWM6 NAND_GPIO[13]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
A14	PAD_NAND_DA7	NAND_DA[7] TTL_G[6] EMMC_DA[7] PWM7 NAND_GPIO[14]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
C13	PAD_UART0_RX	UART0_RX TTL_G[7] UART0_GPIO[0]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
A13	PAD_UART0_TX	UART0_TX TTL_B[0] UART0_GPIO[1]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
B13	PAD_UART1_RX	UART1_RX TTL_B[1] UART1_GPIO[0]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
C12	PAD_UART1_TX	UART1_TX TTL_B[2] UART1_GPIO[1]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
D15	PAD_SPI0_CZ	SPI0_CZ TTL_B[7] PWM4 SPI0_GPIO[0]	VDDP_3	>4mA/8mA/12mA/16mA	PU=86kohm (±15%)/39uA(±15%)	PU	No
D14	PAD_SPI0_CK	SPI0_CK TTL_LCK PWM5 SPI0_GPIO[1]	VDDP_3	>4mA/8mA/12mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
E13	PAD_SPI0_DI	SPI0_DI TTL_LVSYNC PWM6 SPI0_GPIO[2]	VDDP_3	>4mA/8mA/12mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
E14	PAD_SPI0_DO	SPI0_DO TTL_LHSYNC PWM7 SPI0_GPIO[3]	VDDP_3	>4mA/8mA/12mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
D11	PAD_SPI1_CZ	SPI1_CZ TTL_B[4] SPI1_GPIO[0]	VDDP_3	>4mA/8mA/12mA/16mA	PU=86kohm (±15%)/39uA(±15%)	PU	No
E12	PAD_SPI1_CK	SPI1_CK TTL_B[3] SPI1_GPIO[1]	VDDP_3	>4mA/8mA/12mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
E11	PAD_SPI1_DI	SPI1_DI TTL_B[6] SPI1_GPIO[2]	VDDP_3	>4mA/8mA/12mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
E10	PAD_SPI1_DO	SPI1_DO TTL_B[5] SPI1_GPIO[3]	VDDP_3	>4mA/8mA/12mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
D12	PAD_PWM0	I2C0_SCL I2C1_SCL TTL_LDE PWM0 PWM_GPIO[0]	VDDP_3	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
D13	PAD_PWM1	I2C0_SDA I2C1_SDA PWM1 PWM_GPIO[1]	VDDP_3	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
B11	PAD_SD_CLK	SDIO_CLK SD_GPIO[0]	VDDP_3	>4mA/8mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
C10	PAD_SD_CMD	SDIO_CMD SD_GPIO[1]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
C11	PAD_SD_D0	SPI1_CZ SDIO_D[0] SD_GPIO[2]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
B12	PAD_SD_D1	SPI1_CK SDIO_D[1] SD_GPIO[3]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
A10	PAD_SD_D2	SPI1_DI SDIO_D[2] SD_GPIO[4]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
B10	PAD_SD_D3	SPI1_DO SDIO_D[3] SD_GPIO[5]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
D10	PAD_USB_CID	USB_CID	VDDP_3	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
D7	PAD_USB_VBUS	USB_VBUS	VDDP_3	>4mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
A9	PAD_USB_DM	USB_DM USB_GPIO[0]	AVDD_USB	>4mA	Hi-Z		
B9	PAD_USB_DP	USB_DP USB_GPIO[1]	AVDD_USB	>4mA	Hi-Z		
A8	PAD_DM_P1	DM_P1 USB_GPIO[2]	AVDD_USB	>4mA	Hi-Z		
B8	PAD_DP_P1	DP_P1 USB_GPIO[3]	AVDD_USB	>4mA	Hi-Z		
A6	PAD_AUD_VAG	AUD_VAG	AVDD_AUD				
C6	PAD_AUD_VRM_ADC	AUD_VRM_ADC	AVDD_AUD				
B6	PAD_AUD_VRM_DAC	AUD_VRM_DAC	AVDD_AUD				
B5	PAD_AUD_MICIN0	AUD_MICIN0	AVDD_AUD				
B4	PAD_AUD_MICIN1	AUD_MICIN1	AVDD_AUD				
A5	PAD_AUD_MICCM0	AUD_MICCM0	AVDD_AUD				
A4	PAD_AUD_MICCM1	AUD_MICCM1	AVDD_AUD				
A2	PAD_AUD_LINEOUT_R0	AUD_LINEOUT_R0	AVDD_AUD				
B3	PAD_AUD_LINEOUT_L0	AUD_LINEOUT_L0	AVDD_AUD				
G11, G12, H11, H12, H13, H14, J12, J13, J14, K12, K13, K14, L12, L13, L14	VDD						
K10	DVDD_DDR						
J10	DVDD_DDR_RX						
M8	DVDD_NODIE						

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
D6	AVDD_AUD						
P13	AVDD_ETH						
M9	AVDD_NODIE						
K8	AVDD_PLL						
D8	AVDD_USB						
R11	AVDD_XTAL						
F7, G7, G8	VDDIO_CMD						
H7, H8, J7, J8, K7	VDDIO_DATA						
J15	VDDP_1						
H15	VDDP_2						
G15	VDDP_3						
B2, B7, C3, C4, C5, C7, C8, C9, D5, D9, E1, E5, E8, E9, E15, F5, F6, F8, F9, F10, F11, F12, F13, G5, G6, G9, G10, G14, H1, H6, H10, H17, J1, J6, J11, J16, K6, K11, K15, L2, L5, L6, L7, L8, L10, L11, L15, L16, M5, M6, M11, M12, M13, M14, M18, N1, N5, N11, P3, P5, P6, R5, R10, R13, T10, T11, T12, T14, U1, U5, V4	VSS						
	DVSS_DDR						
	AVSS_AUD						
	AVSS_ETH						
	AVSS_NODIE						
	AVSS_PLL						
	AVSS_RTC						
	AVSS_USB						
	AVSS_XTAL						
	AVSSIO_CMD						
	AVSSIO_CMD2						
	VSSIO_DATA						
	VSSIO_MCLK						
B1	A_DDR3_A[0]	A_DDR3_A[0]	VDDIO_CMD				
G3	A_DDR3_A[1]	A_DDR3_A[1]	VDDIO_CMD				
C2	A_DDR3_A[2]	A_DDR3_A[2]	VDDIO_CMD				
F1	A_DDR3_A[3]	A_DDR3_A[3]	VDDIO_CMD				
F4	A_DDR3_A[4]	A_DDR3_A[4]	VDDIO_CMD				
F2	A_DDR3_A[5]	A_DDR3_A[5]	VDDIO_CMD				
F3	A_DDR3_A[6]	A_DDR3_A[6]	VDDIO_CMD				
D1	A_DDR3_A[7]	A_DDR3_A[7]	VDDIO_CMD				
E4	A_DDR3_A[8]	A_DDR3_A[8]	VDDIO_CMD				

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
C1	A_DDR3_A[9]	A_DDR3_A[9]	VDDIO_CMD				
K3	A_DDR3_A[10]	A_DDR3_A[10]	VDDIO_CMD				
E3	A_DDR3_A[11]	A_DDR3_A[11]	VDDIO_CMD				
G4	A_DDR3_A[12]	A_DDR3_A[12]	VDDIO_CMD				
D2	A_DDR3_A[13]	A_DDR3_A[13]	VDDIO_CMD				
D4	A_DDR3_A[14]	A_DDR3_A[14]	VDDIO_CMD				
H3	A_DDR3_A[15]	A_DDR3_A[15]	VDDIO_CMD				
G1	A_DDR3_BA[0]	A_DDR3_BA[0]	VDDIO_CMD				
J4	A_DDR3_BA[1]	A_DDR3_BA[1]	VDDIO_CMD				
G2	A_DDR3_BA[2]	A_DDR3_BA[2]	VDDIO_CMD				
D3	A_DDR3_CKE	A_DDR3_CKE	VDDIO_CMD				
H4	A_DDR3_ODT	A_DDR3_ODT	VDDIO_CMD				
H2	A_DDR3_WEZ	A_DDR3_WEZ	VDDIO_CMD				
J3	A_DDR3_RASZ	A_DDR3_RASZ	VDDIO_CMD				
K4	A_DDR3_CASZ	A_DDR3_CASZ	VDDIO_CMD				
E2	A_DDR3_RST	A_DDR3_RST	VDDIO_CMD				
J2	A_DDR3_CSB[0]	A_DDR3_CSB[0]	VDDIO_CMD				
K1	A_DDR3_MCLK	A_DDR3_MCLK	VDDIO_DATA				
K2	A_DDR3_MCLKZ	A_DDR3_MCLKZ	VDDIO_DATA				
U2	A_DDR3_DQM[0]	A_DDR3_DQM[0]	VDDIO_DATA				
M4	A_DDR3_DQM[1]	A_DDR3_DQM[1]	VDDIO_DATA				
P2	A_DDR3_DQS[0]	A_DDR3_DQS[0]	VDDIO_DATA				
N4	A_DDR3_DQS[1]	A_DDR3_DQS[1]	VDDIO_DATA				
P1	A_DDR3_DQSB[0]	A_DDR3_DQSB[0]	VDDIO_DATA				
P4	A_DDR3_DQSB[1]	A_DDR3_DQSB[1]	VDDIO_DATA				
N2	A_DDR3_DQ[0]	A_DDR3_DQ[0]	VDDIO_DATA				
T2	A_DDR3_DQ[1]	A_DDR3_DQ[1]	VDDIO_DATA				
M1	A_DDR3_DQ[2]	A_DDR3_DQ[2]	VDDIO_DATA				
T1	A_DDR3_DQ[3]	A_DDR3_DQ[3]	VDDIO_DATA				
L1	A_DDR3_DQ[4]	A_DDR3_DQ[4]	VDDIO_DATA				
R1	A_DDR3_DQ[5]	A_DDR3_DQ[5]	VDDIO_DATA				
M2	A_DDR3_DQ[6]	A_DDR3_DQ[6]	VDDIO_DATA				
R2	A_DDR3_DQ[7]	A_DDR3_DQ[7]	VDDIO_DATA				
C4	A_DDR3_DQ[8]	A_DDR3_DQ[8]	VDDIO_DATA				
M3	A_DDR3_DQ[9]	A_DDR3_DQ[9]	VDDIO_DATA				

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Ball Location	Ball Name	Multi Function	PAD Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
N3	A_DDR3_DQ[10]	A_DDR3_DQ[10]	VDDIO_DATA				
L3	A_DDR3_DQ[11]	A_DDR3_DQ[11]	VDDIO_DATA				
R3	A_DDR3_DQ[12]	A_DDR3_DQ[12]	VDDIO_DATA				
R4	A_DDR3_DQ[13]	A_DDR3_DQ[13]	VDDIO_DATA				
T3	A_DDR3_DQ[14]	A_DDR3_DQ[14]	VDDIO_DATA				
T4	A_DDR3_DQ[15]	A_DDR3_DQ[15]	VDDIO_DATA				

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SIGNAL DESCRIPTION

Image Sensor

Signal Name	Signal Type	Function	Ball Location
SR_D[0]	Input	Image Sensor Data Bus	K17, J17, K18, K17, L18, N17
SR_D[1]	Input	Image Sensor Data Bus	K18, J18, J17, K18, L17, M16
SR_D[2]	Input	Image Sensor Data Bus	E17, K18, K17, L18, K18, M17
SR_D[3]	Input	Image Sensor Data Bus	J18, G16, G18, J17, K17, L18
SR_D[4]	Input	Image Sensor Data Bus	H18, L17, L17, M17, J18, L17
SR_D[5]	Input	Image Sensor Data Bus	J17, E18, G16, G18, J17, K18
SR_D[6]	Input	Image Sensor Data Bus	G16, L18, L18, M16, H18, K17
SR_D[7]	Input	Image Sensor Data Bus	L18, G18, H18, H18, G18, J18
SR_D[8]	Input	Image Sensor Data Bus	F17, M17, M17, N17, F15, J17
SR_D[9]	Input	Image Sensor Data Bus	M17, H18, F15, J18, E18, H18
SR_D[10]	Input	Image Sensor Data Bus	F17
SR_D[11]	Input	Image Sensor Data Bus	E17
SR_HS	Input	Image Sensor Horizontal Sync Signal	F15, E17, E18, E18, M17, F17
SR_VS	Input	Image Sensor Vertical Sync Signal	E18, F17, F17, F15, M16, F16
SR_PCK	Input	Image Sensor Pixel Clock	L17, K17, J18, L17, F16, E17
SR_PDN	Output	Image Sensor Power Down Control	F16, F16, F16, F17, N17, F15
SR_RST	Output	Image Sensor Reset Control	G17, F15, G17, G16, G17, E18
SR_MCK	Output	Image Sensor Reference Clock	G18, G17, E17, E17, G16, G17
SR_SCL	Output	Image Sensor I2C Serial Clock	N14, P18
SR_SDA	Input/Output	Image Sensor I2C Serial Data	P14, N16

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CCIR

Signal Name	Signal Type	Function	Ball Location
CCIR_IN_D[0]	Input	CCIR Data Bus	M17
CCIR_IN_D[1]	Input	CCIR Data Bus	L18
CCIR_IN_D[2]	Input	CCIR Data Bus	L17
CCIR_IN_D[3]	Input	CCIR Data Bus	K18
CCIR_IN_D[4]	Input	CCIR Data Bus	K17
CCIR_IN_D[5]	Input	CCIR Data Bus	J18
CCIR_IN_D[6]	Input	CCIR Data Bus	J17
CCIR_IN_D[7]	Input	CCIR Data Bus	H18
CCIR_IN_D[8]	Input	CCIR Data Bus	G16
CCIR_IN_D[9]	Input	CCIR Data Bus	G18
CCIR_IN_CLK	Input	CCIR Sample Clock	F15

Audio Interface

Signal Name	Signal Type	Function	Ball Location
AUD_LINEOUT_L0	Output	Audio Left Channel Line Output	B3
AUD_LINEOUT_R0	Output	Audio Right Channel Line Output	A2
AUD_VAG	Output	Audio Reference Voltage from 1/2 AVDD_AUD	A6
AUD_VRM_ADC	Input	Audio Reference Voltage for ADC	C6
AUD_VRM_DAC	Input	Audio Reference Voltage for DAC	B6
AUD_MICIN0	Input	Audio Left Channel Microphone Postive Input	B5
AUD_MICIN1	Input	Audio Right Channel Microphone Postive Input	B4
AUD_MICCM0	Input	Audio Left Channel Microphone Negative Input	A5
AUD_MICCM1	Input	Audio Right Channel Microphone Negative Input	A4

10/100 Ethernet Interface

Signal Name	Signal Type	Function	Ball Location
ETH_RN	Input	10/100 Ethernet Negative Receiving Input	U13
ETH_RP	Input	10/100 Ethernet Positive Receiving Input	T13
ETH_TN	Output	10/100 Ethernet Negative Transmitting Output	U14
ETH_TP	Output	10/100 Ethernet Positive Transmitting Output	V14

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Signal Name	Signal Type	Function	Ball Location
ETH_LED0	Output	10/100 Ethernet LED 0 Control	N13
ETH_LED1	Output	10/100 Ethernet LED 1 Control	N12

NAND Flash Interface

Signal Name	Signal Type	Function	Ball Location
NAND_ALE	Output	NAND Flash Address Latch Enable	C18
NAND_CLE	Output	NAND Flash Command Latch Enable	C17
NAND_CEZ	Output	NAND Flash Chip 0 Enable (active low)	B18
NAND_WEZ	Output	NAND Flash Write Enable (active low)	D16
NAND_WPZ	Output	NAND Flash Write Protect (active low)	D17
NAND_REZ	Output	NAND Flash Read Enable (active low)	B17
NAND_RBZ	Input	NAND Flash Status (high: ready, low: busy)	C16
NAND_DA[0]	Input/Output	NAND Flash Data Bus	A17
NAND_DA[1]	Input/Output	NAND Flash Data Bus	B16
NAND_DA[2]	Input/Output	NAND Flash Data Bus	A16
NAND_DA[3]	Input/Output	NAND Flash Data Bus	C15
NAND_DA[4]	Input/Output	NAND Flash Data Bus	B15
NAND_DA[5]	Input/Output	NAND Flash Data Bus	C14
NAND_DA[6]	Input/Output	NAND Flash Data Bus	B14
NAND_DA[7]	Input/Output	NAND Flash Data Bus	A14

SD Card Interface

Signal Name	Signal Type	Function	Ball Location
SD_CLK	Output	SD Card Clock	C17
SD_CMD	Output	SD Card Command	B18
SD_D[0]	Input/Output	SD Card Data Bus	D16
SD_D[1]	Input/Output	SD Card Data Bus	D17
SD_D[2]	Input/Output	SD Card Data Bus	B17
SD_D[3]	Input/Output	SD Card Data Bus	C16

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SDIO 2.0 Interface

Signal Name	Signal Type	Function	Ball Location
SDIO_CLK	Output	SDIO 2.0 Clock	B11
SDIO_CMD	Output	SDIO 2.0 Command	C10
SDIO_D[0]	Input/Output	SDIO 2.0 Data Bus	C11
SDIO_D[1]	Input/Output	SDIO 2.0 Data Bus	B12
SDIO_D[2]	Input/Output	SDIO 2.0 Data Bus	A10
SDIO_D[3]	Input/Output	SDIO 2.0 Data Bus	B10
SD_CDZ	Input	SD Card Detect (active low)	V3

SPI Flash Interface

Signal Name	Signal Type	Function	Ball Location
SPI_CK	Output	SPI Flash Clock	N10
SPI_CZ1	Output	SPI Flash Chip Select 1 (active low)	T9
SPI_CZ2	Output	SPI Flash Chip Select 2 (active low)	V8
SPI_DI	Output	SPI Flash Serial DataTo Device	V10
SPI_DO	Input	SPI Flash Serial Data From Device	U10
SPI_WPZ	Output	SPI Flash Write Protect Control (active low)	N9
SPI_HLDZ	Output	SPI Flash Hold Control (active low)	P10

USB 2.0 Interface

Signal Name	Signal Type	Function	Ball Location
USB_CID	Input	USB 2.0 OTG ID (high slave mode, low host mode)	D10
USB_VBUS	Input	USB 2.0 VBUS Power	D7
USB_DM	Input/Output	USB 2.0 Inverting Data	A9
USB_DP	Input/Output	USB 2.0 Non-inverting Data	B9
DM_P1	Input/Output	USB 2.0 Inverting Data1	A8
DP_P1	Input/Output	USB 2.0 Non-inverting Data0	B8

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Master SPI Interface

Signal Name	Signal Type	Function	Ball Location
SPI0_CZ	Output	Master SPI 0 Chip Select (active low)	D15, U16, T18
SPI0_CK	Output	Master SPI 0 Serial Clock	D14, V16, R18
SPI0_DI	Output	Master SPI 0 Serial Data In	E13, T16, R17
SPI0_DO	Input	Master SPI 0 Serial Data Out	E14, V17, P17
SPI1_CZ	Output	Master SPI 1 Chip Select (active low)	D11, U17, C11, R14
SPI1_CK	Output	Master SPI 1 Serial Clock	E12, T17, B12, R15
SPI1_DI	Output	Master SPI 1 Serial Data In	E11, U18, A10, P16
SPI1_DO	Input	Master SPI 1 Serial Data Out	E10, R16, B10, P15

Master I2C Interface

Signal Name	Signal Type	Function	Ball Location
I2C0_SCL	Output	Master I2C 0 Serial Clock	N14, D12, N17
I2C0_SDA	Input/Output	Master I2C 0 Serial Data	P14, D13, M16
I2C1_SCL	Output	Master I2C 1 Serial Clock	P18, D12, N17
I2C1_SDA	Input/Output	Master I2C 1 Serial Data	N16, D13, M16

UART Interface

Signal Name	Signal Type	Function	Ball Location
UART_RX0	Input	UART 0 Receiver	C13, T18, N15
UART_TX0	Output	UART 0 Transmitter	A13, R18, M15
UART_RX1	Input	UART 1 Receiver	B13, R17, U15
UART_TX1	Output	UART 1 Transmitter	C12, P17, T15

Fast UART Interface

Signal Name	Signal Type	Function	Ball Location
FUART_RX	Input	Fast UART Receiver	T18, R14
FUART_TX	Output	Fast UART Transmitter	R18, R15
FUART_CTS	Input	Fast UART Clear to Set	R17, P16
FUART_RTS	Output	Fast UART Request to Set	P17, P15

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DDR3 Interface

Signal Name	Signal Type	Function	Ball Location
A_DDR3_A[0]	Output	DRAM Memory Address [0]	B1
A_DDR3_A[1]	Output	DRAM Memory Address [1]	G3
A_DDR3_A[2]	Output	DRAM Memory Address [2]	C2
A_DDR3_A[3]	Output	DRAM Memory Address [3]	F1
A_DDR3_A[4]	Output	DRAM Memory Address [4]	F4
A_DDR3_A[5]	Output	DRAM Memory Address [5]	F2
A_DDR3_A[6]	Output	DRAM Memory Address [6]	F3
A_DDR3_A[7]	Output	DRAM Memory Address [7]	D1
A_DDR3_A[8]	Output	DRAM Memory Address [8]	E4
A_DDR3_A[9]	Output	DRAM Memory Address [9]	C1
A_DDR3_A[10]	Output	DRAM Memory Address [10]	K3
A_DDR3_A[11]	Output	DRAM Memory Address [11]	E3
A_DDR3_A[12]	Output	DRAM Memory Address [12]	G4
A_DDR3_A[13]	Output	DRAM Memory Address [13]	D2
A_DDR3_A[14]	Output	DRAM Memory Address [14]	D4
A_DDR3_A[15]	Output	DRAM Memory Address [15]	H3
A_DDR3_BA[0]	Output	DRAM Memory Bank Address [0]	G1
A_DDR3_BA[1]	Output	DRAM Memory Bank Address [1]	J4
A_DDR3_BA[2]	Output	DRAM Memory Bank Address [2]	G2
A_DDR3_CKE	Output	DRAM Clock Enable Output	D3
A_DDR3_ODT	Input/Output	Reserved for future On-Die Termination	H4
A_DDR3_WEZ	Output	Write Enable; active low	H2
A_DDR3_RASZ	Output	Row Address Strobe; active low	J3
A_DDR3_CASZ	Output	Column Address Strobe; active low	K4
A_DDR3_RST	Output	DRAM Memory Reset; active low	E2
A_DDR3_CSB[0]	Output	DRAM Chip Select	J2
A_DDR3_MCLK	Output	DRAM Memory Positive Differential Clock	K1
A_DDR3_MCLKZ	Output	DRAM Memory Negative Differential Clock	K2
A_DDR3_DQM[0]	Output	Data Mask for Low Byte; active high [0]	U2
A_DDR3_DQM[1]	Output	Data Mask for Low Byte; active high [1]	M4
A_DDR3_DQS[0]	Input/Output	Data Strobe [0]	P2
A_DDR3_DQS[1]	Input/Output	Data Strobe [1]	N4
A_DDR3_DQSB[0]	Input/Output	Data Strobe Inverse [0]	P1

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Signal Name	Signal Type	Function	Ball Location
A_DDR3_DQSB[1]	Input/Output	Data Strobe Inverse [1]	P4
A_DDR3_DQ[0]	Input/Output	DRAM Memory Data Bus [0]	N2
A_DDR3_DQ[1]	Input/Output	DRAM Memory Data Bus [1]	T2
A_DDR3_DQ[2]	Input/Output	DRAM Memory Data Bus [2]	M1
A_DDR3_DQ[3]	Input/Output	DRAM Memory Data Bus [3]	T1
A_DDR3_DQ[4]	Input/Output	DRAM Memory Data Bus [4]	L1
A_DDR3_DQ[5]	Input/Output	DRAM Memory Data Bus [5]	R1
A_DDR3_DQ[6]	Input/Output	DRAM Memory Data Bus [6]	M2
A_DDR3_DQ[7]	Input/Output	DRAM Memory Data Bus [7]	R2
A_DDR3_DQ[8]	Input/Output	DRAM Memory Data Bus [8]	C4
A_DDR3_DQ[9]	Input/Output	DRAM Memory Data Bus [9]	M3
A_DDR3_DQ[10]	Input/Output	DRAM Memory Data Bus [10]	N3
A_DDR3_DQ[11]	Input/Output	DRAM Memory Data Bus [11]	L3
A_DDR3_DQ[12]	Input/Output	DRAM Memory Data Bus [12]	R3
A_DDR3_DQ[13]	Input/Output	DRAM Memory Data Bus [13]	R4
A_DDR3_DQ[14]	Input/Output	DRAM Memory Data Bus [14]	T3
A_DDR3_DQ[15]	Input/Output	DRAM Memory Data Bus [15]	T4

PWM Interface

Signal Name	Signal Type	Function	Ball Location
PWM0	Output	PWM 0 Output	D12, U17, N8, T7
PWM1	Output	PWM 1 Output	D13, T17, P8, U7
PWM2	Output	PWM 2 Output	U18, R9, U9
PWM3	Output	PWM 3 Output	R16, P9, U8
PWM4	Output	PWM 4 Output	B15, D15
PWM5	Output	PWM 5 Output	C14, D14
PWM6	Output	PWM 6 Output	B14, E13
PWM7	Output	PWM 7 Output	A14, E14

IR Interface

Signal Name	Signal Type	Function	Ball Location
IRIN	Input	IR Receiver	V2

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SAR Interface

Signal Name	Signal Type	Function	Ball Location
SAR_ASI0	Input	SAR Analog Signal Channel 0	R7
SAR_ASI1	Input	SAR Analog Signal Channel 1	R6
SAR_ASI2	Input	SAR Analog Signal Channel 2	P7
SAR_ASI3	Input	SAR Analog Signal Channel 3	N7

System Interface

Signal Name	Signal Type	Function	Ball Location
XTAL_IN	Input	24MHz Crystal Output	V11
XTAL_OUT	Output	24MHz Crystal Input	U11
SE_XTAL_OUT	Output	24MHz Clock Output	R12
HW_RESET	Input	Chip Reset (active high)	U3
RTC_OUT	Output	32KHz Crystal Output	U4
RTC_IN	Input	32KHz Crystal Input	V5
UART_RX	Input	Debug Port for UART Receiver or Slave I2C Serial Clock	U6
UART_TX	Output	Debug Port for UART Transmitter or Slave I2C Serial Data	T5
GND_EFUSE	Input	Power Source if eFuse Burning (connect to ground)	L5

GPIO Interface

Signal Name	Signal Type	Function	Ball Location
GPIO[0]	Input/Output	General Purpose Input/Output	R14
GPIO[1]	Input/Output	General Purpose Input/Output	R15
GPIO[2]	Input/Output	General Purpose Input/Output	P16
GPIO[3]	Input/Output	General Purpose Input/Output	P15
GPIO[4]	Input/Output	General Purpose Input/Output	N15
GPIO[5]	Input/Output	General Purpose Input/Output	M15
GPIO[6]	Input/Output	General Purpose Input/Output	U15
GPIO[7]	Input/Output	General Purpose Input/Output	T15
GPIO[8]	Input/Output	General Purpose Input/Output	U16
GPIO[9]	Input/Output	General Purpose Input/Output	V16
GPIO[10]	Input/Output	General Purpose Input/Output	T16

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Signal Name	Signal Type	Function	Ball Location
GPIO[11]	Input/Output	General Purpose Input/Output	V17
GPIO[12]	Input/Output	General Purpose Input/Output	U17
GPIO[13]	Input/Output	General Purpose Input/Output	T17
GPIO[14]	Input/Output	General Purpose Input/Output	U18
GPIO[15]	Input/Output	General Purpose Input/Output	R16
FUART_GPIO[0]	Input/Output	General Purpose Input/Output	T18
FUART_GPIO[1]	Input/Output	General Purpose Input/Output	R18
FUART_GPIO[2]	Input/Output	General Purpose Input/Output	R17
FUART_GPIO[3]	Input/Output	General Purpose Input/Output	P17
UART0_GPIO[0]	Input/Output	General Purpose Input/Output	C13
UART0_GPIO[1]	Input/Output	General Purpose Input/Output	A13
UART1_GPIO[0]	Input/Output	General Purpose Input/Output	B13
UART1_GPIO[1]	Input/Output	General Purpose Input/Output	C12
I2C0_GPIO[0]	Input/Output	General Purpose Input/Output	N14
I2C0_GPIO[1]	Input/Output	General Purpose Input/Output	P14
I2C1_GPIO[0]	Input/Output	General Purpose Input/Output	P18
I2C1_GPIO[1]	Input/Output	General Purpose Input/Output	N16
SPI0_GPIO[0]	Input/Output	General Purpose Input/Output	D15
SPI0_GPIO[1]	Input/Output	General Purpose Input/Output	D14
SPI0_GPIO[2]	Input/Output	General Purpose Input/Output	E13
SPI0_GPIO[3]	Input/Output	General Purpose Input/Output	E14
SPI1_GPIO[0]	Input/Output	General Purpose Input/Output	D11
SPI1_GPIO[1]	Input/Output	General Purpose Input/Output	E12
SPI1_GPIO[2]	Input/Output	General Purpose Input/Output	E11
SPI1_GPIO[3]	Input/Output	General Purpose Input/Output	E10
PWM_GPIO[0]	Input/Output	General Purpose Input/Output	D12
PWM_GPIO[1]	Input/Output	General Purpose Input/Output	D13
NAND_GPIO[0]	Input/Output	General Purpose Input/Output	B18
NAND_GPIO[1]	Input/Output	General Purpose Input/Output	C18
NAND_GPIO[10]	Input/Output	General Purpose Input/Output	C15
NAND_GPIO[11]	Input/Output	General Purpose Input/Output	B15
NAND_GPIO[12]	Input/Output	General Purpose Input/Output	C14
NAND_GPIO[13]	Input/Output	General Purpose Input/Output	B14

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Signal Name	Signal Type	Function	Ball Location
NAND_GPIO[14]	Input/Output	General Purpose Input/Output	A14
NAND_GPIO[2]	Input/Output	General Purpose Input/Output	C17
NAND_GPIO[3]	Input/Output	General Purpose Input/Output	D16
NAND_GPIO[4]	Input/Output	General Purpose Input/Output	D17
NAND_GPIO[5]	Input/Output	General Purpose Input/Output	B17
NAND_GPIO[6]	Input/Output	General Purpose Input/Output	C16
NAND_GPIO[7]	Input/Output	General Purpose Input/Output	A17
NAND_GPIO[8]	Input/Output	General Purpose Input/Output	B16
NAND_GPIO[9]	Input/Output	General Purpose Input/Output	A16
SD_GPIO[0]	Input/Output	General Purpose Input/Output	B11
SD_GPIO[1]	Input/Output	General Purpose Input/Output	C10
SD_GPIO[2]	Input/Output	General Purpose Input/Output	C11
SD_GPIO[3]	Input/Output	General Purpose Input/Output	B12
SD_GPIO[4]	Input/Output	General Purpose Input/Output	A10
SD_GPIO[5]	Input/Output	General Purpose Input/Output	B10
SR_GPIO[0]	Input/Output	General Purpose Input/Output	N17
SR_GPIO[1]	Input/Output	General Purpose Input/Output	M16
SR_GPIO[2]	Input/Output	General Purpose Input/Output	M17
SR_GPIO[3]	Input/Output	General Purpose Input/Output	L18
SR_GPIO[4]	Input/Output	General Purpose Input/Output	L17
SR_GPIO[5]	Input/Output	General Purpose Input/Output	K18
SR_GPIO[6]	Input/Output	General Purpose Input/Output	K17
SR_GPIO[7]	Input/Output	General Purpose Input/Output	J18
SR_GPIO[8]	Input/Output	General Purpose Input/Output	J17
SR_GPIO[9]	Input/Output	General Purpose Input/Output	H18
SR_GPIO[10]	Input/Output	General Purpose Input/Output	G16
SR_GPIO[11]	Input/Output	General Purpose Input/Output	G18
SR_GPIO[12]	Input/Output	General Purpose Input/Output	F15
SR_GPIO[13]	Input/Output	General Purpose Input/Output	E18
SR_GPIO[14]	Input/Output	General Purpose Input/Output	F17
SR_GPIO[15]	Input/Output	General Purpose Input/Output	E17
SR_GPIO[16]	Input/Output	General Purpose Input/Output	F16
SR_GPIO[17]	Input/Output	General Purpose Input/Output	G17

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Signal Name	Signal Type	Function	Ball Location
USB_GPIO[0]	Input/Output	General Purpose Input/Output	A9
USB_GPIO[1]	Input/Output	General Purpose Input/Output	B9
PM_GPIO[0]	Input/Output	General Purpose Input/Output	N8
PM_GPIO[1]	Input/Output	General Purpose Input/Output	P8
PM_GPIO[2]	Input/Output	General Purpose Input/Output	R9
PM_GPIO[3]	Input/Output	General Purpose Input/Output	P9
PM_GPIO[4]	Input/Output	General Purpose Input/Output	T6
PM_GPIO[5]	Input/Output	General Purpose Input/Output	U7
PM_GPIO[6]	Input/Output	General Purpose Input/Output	T7
PM_GPIO[7]	Input/Output	General Purpose Input/Output	T8
PM_GPIO[8]	Input/Output	General Purpose Input/Output	V8
PM_GPIO[9]	Input/Output	General Purpose Input/Output	U9
PM_GPIO[10]	Input/Output	General Purpose Input/Output	U8
SD_CDZ_GPIO	Input/Output	General Purpose Input/Output	V3
IRIN_GPIO	Input/Output	General Purpose Input/Output	V2
SPI_GPIO[0]	Input/Output	General Purpose Input/Output	T9
SPI_GPIO[1]	Input/Output	General Purpose Input/Output	N10
SPI_GPIO[2]	Input/Output	General Purpose Input/Output	V10
SPI_GPIO[3]	Input/Output	General Purpose Input/Output	U10
SPI_GPIO[4]	Input/Output	General Purpose Input/Output	N9
SPI_GPIO[5]	Input/Output	General Purpose Input/Output	P10
SAR_GPIO[0]	Input/Output	General Purpose Input/Output	R7
SAR_GPIO[1]	Input/Output	General Purpose Input/Output	R6
SAR_GPIO[2]	Input/Output	General Purpose Input/Output	P7
SAR_GPIO[3]	Input/Output	General Purpose Input/Output	N7
ETH_GPIO[0]	Input/Output	General Purpose Input/Output	U13
ETH_GPIO[1]	Input/Output	General Purpose Input/Output	T13
ETH_GPIO[2]	Input/Output	General Purpose Input/Output	U14
ETH_GPIO[3]	Input/Output	General Purpose Input/Output	V14
LED_GPIO[0]	Input/Output	General Purpose Input/Output	N13
LED_GPIO[1]	Input/Output	General Purpose Input/Output	N12

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Cortex-A7 JTAG

Signal Name	Signal Type	Function	Ball Location
EJ_TCK	Input	CA7 JTAG Clock	T18, D15
EJ_TMS	Intpu	CA7 JTAG Mode Select	R18, D14
EJ_TDO	Output	CA7 JTAG Data Out	R17, E13
EJ_TDI	Input	CA7 JTAG Data In	P17, E14

Power Interface

Signal Name	Signal Type	Function	Ball Location
VDD	Input	Digital Power	G11, G12, H11, H12, H13, H14, J12, J13, J14, K12, K13, K14, L12, L13, L14
DVDD_DDR	Input	Digital Power for DDR	K10
DVDD_DDR_RX	Input	Digital Power for DDR	J10
DVDD_NODIE	Output	PM LDO Output	M8
AVDD_AUD	Input	Analog Power for Audio	D6
AVDD_ETH	Input	Analog Power for Ethernet	P13
AVDD_NODIE	Input	Analog Power for PM	M9
AVDD_PLL	Input	Analog Power for PLL	K8
AVDD_USB	Input	Analog Power for USB	D8
AVDD_XTAL	Input	Analog Power for XTAL	R11
VDDIO_CMD	Input	Analog Power for DDR	F7, G7, G8
VDDIO_DATA	Input	Analog Power for DDR	H7, H8, J7, J8, K7
VDDP_1	Input	Pad Power	J15
VDDP_2	Input	Pad Power	H15
VDDP_3	Input	Pad Power	G15

Gound

Signal Name	Signal Type	Function	Ball Location
VSS	Input	Digital Ground	B2, B7, C3, C4, C5, C7, C8, C9, D5, D9, E1, E5, E8, E9, E15, F5, F6, F8, F9, F10, F11, F12, F13, G5, G6, G9, G10, G14, H1, H6, H10, H17, J1, J6, J11, J16, K6, K11, K15, L2, L5, L6,
DVSS_DDR	Input	Digital Ground for DDR	
AVSS_AUD	Input	Analog Ground for Audio	
AVSS_ETH	Input	Analog Ground for Ethernet	
AVSS_NODIE	Input	Analog Ground for PM	

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Signal Name	Signal Type	Function	Ball Location
AVSS_PLL	Input	Analog Ground for PLL	L7, L8, L10, L11, L15, L16, M5, M6, M11, M12, M13, M14, M18, N1, N5, N11, P3, P5, P6, R5, R10, R13, T10, T11, T12, T14, U1, U5, V4
AVSS_RTC	Input	Analog Ground for 32KHz XTAL	
AVSS_USB	Input	Analog Ground for USB	
AVSS_XTAL	Input	Analog Ground for 24MHz XTAL	
VSSIO_CMD	Input	Analog Ground for DDR	
VSSIO_CMD2	Input	Analog Ground for DDR	
VSSIO_DATA	Input	Analog Ground for DDR	
VSSIO_MCLK	Input	Analog Ground for DDR	

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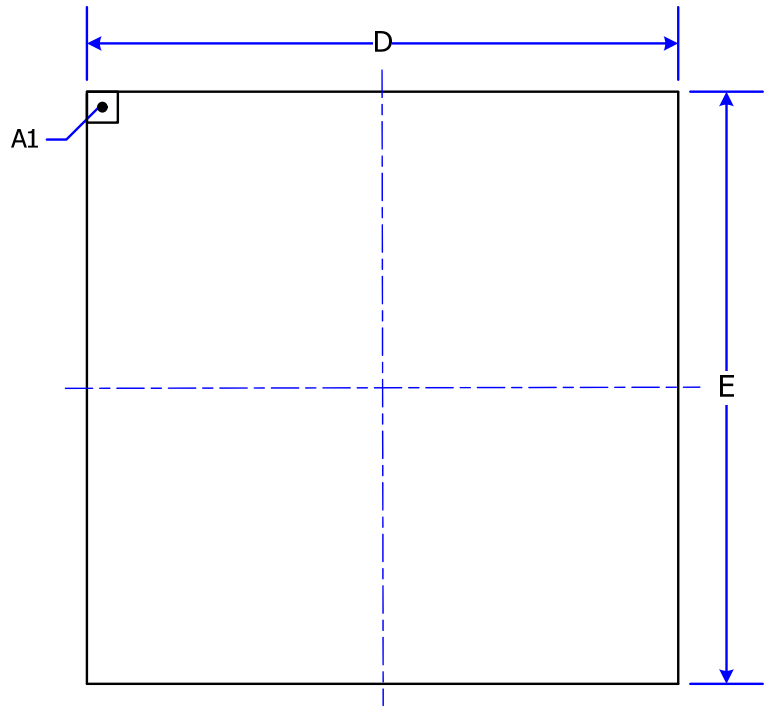
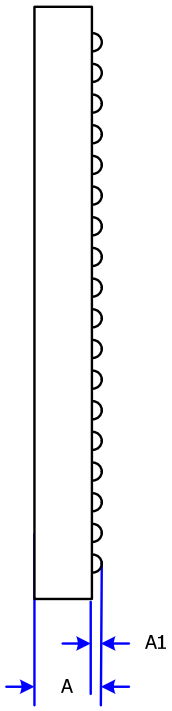
MECHANICAL DIMENSIONS

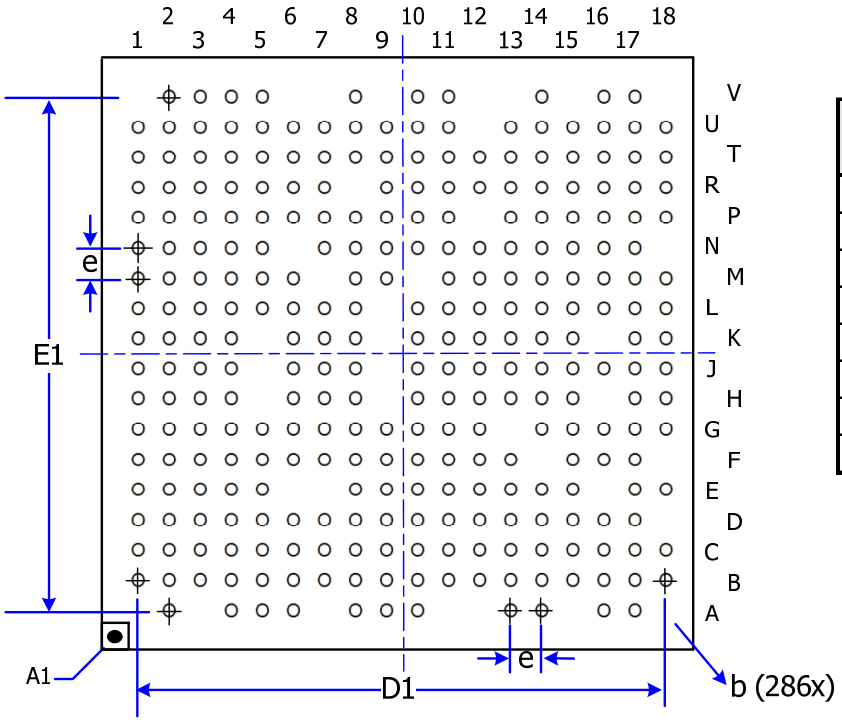
Top View



Side View



Bottom View



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.6	-	-	0.063
A1	0.2	-	0.3	0.08	-	0.012
D	11.9	12	12.1	0.469	0.472	0.476
E	11.9	12	12.1	0.469	0.472	0.476
D1	11	11.05	11.1	0.433	0.435	0.437
E1	11	11.05	11.1	0.433	0.435	0.437
e	0.6	0.65	0.7	0.024	0.026	0.028
b	0.3	0.35	0.4	0.012	0.014	0.016

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ELECTRICAL SPECIFICATIONS

Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	V_{IH}	2.5			V
Input Voltage, Low	V_{IL}			0.8	V
Input Current, High	I_{IH}			-1.0	uA
Input Current, Low	I_{IL}			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	V_{OH}	VDDP-0.1[Note]			V
Output Voltage, Low	V_{OL}			0.1	V
SAR ADC Input		0		V_{VDD_33}	V
AUDIO OUTPUTS					
Line-Out			2.54		Vp-p

Note: 1. VDDP can be V_{VDD_33}, V_{VDD_15}

2. 0.9Vrms @10Kohm load

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}		3.3		V
1.5V Supply Voltage (DDR III)	V_{VDD_15}		1.5		V
Core Power Supply Voltage (Core)	V_{VDD_core}	0.87	0.9		V
Ambient Operation Temperature	T_A	-40		85	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	**Symbol**	**Min**	**Typ.**	**Max.**	**Unit**
3.3V Supply Voltage	V_{VDD_33}			3.63	V
1.5V Supply Voltage (DDR III)	V_{VDD_15}			1.65	V
Core Power Supply Voltage (Core)	V_{VDD_core}			1.26	V
Storage Temperature	T_{STG}	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

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HARDWARE POWER SEQUENCE PROCEDURE

The timing requirements of the hardware reset signal are shown as below:

Hardware Reset

HWRESET: Chip Reset; High Reset (Level)

The HWRESET pin is suggested to connect with 3.3V standby as shown in Figure 1. The VIH is 2V (Typ) +/- 10% (2.2V~1.8V); the VIL is 1.2V (Typ) +/- 10% (1.08V~1.32V). The power sequence is as shown in Figure 2.

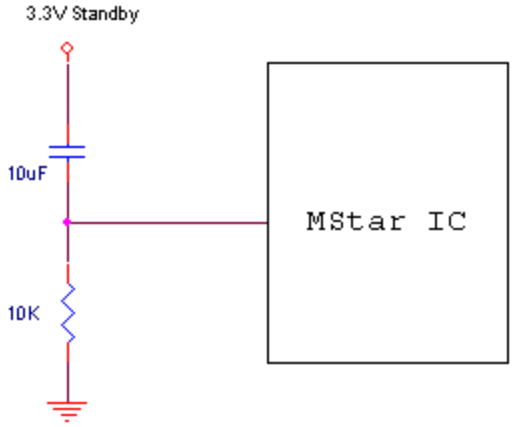

Figure 1: Reset Application Circuit

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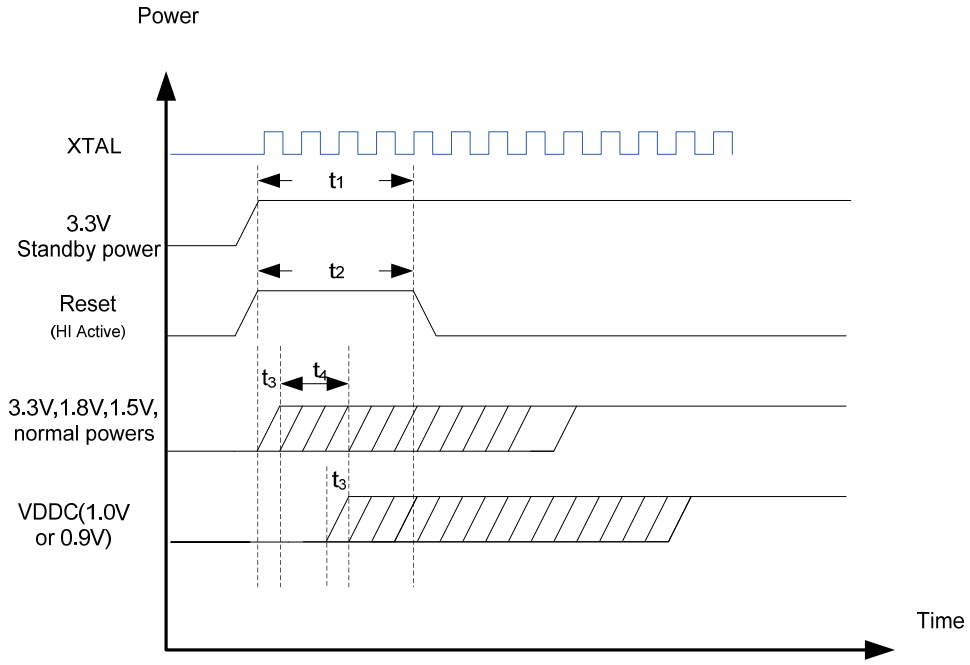
External Reset IC with External LDO

The timing is shown as Figure 2. The RST and power waveform must satisfy Figure 2 with parameters listed in Table 1.



Note:

***3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)**

***1.0V/0.9V (VDD, DVDD_DDR, DVDD_DDR_RX)**

***1.5V (VDDIO_DATA, VDDIO_CMD)**

***1.8V (VDDP_2)**

***3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)**

Figure 2: Power on Sequence

Table 1: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	XTAL stable to Reset falling	5	—	—	ms
t_2	Reset pulse width	5	—	—	ms
t_3	Normal 3.3V, 1.8V, 1.5V, VDDC power rising time (0% to 100%)	—	—	20	ms
t_4	Normal 3.3V, 1.8V, 1.5V to VDDC lead time	1	—	—	ms

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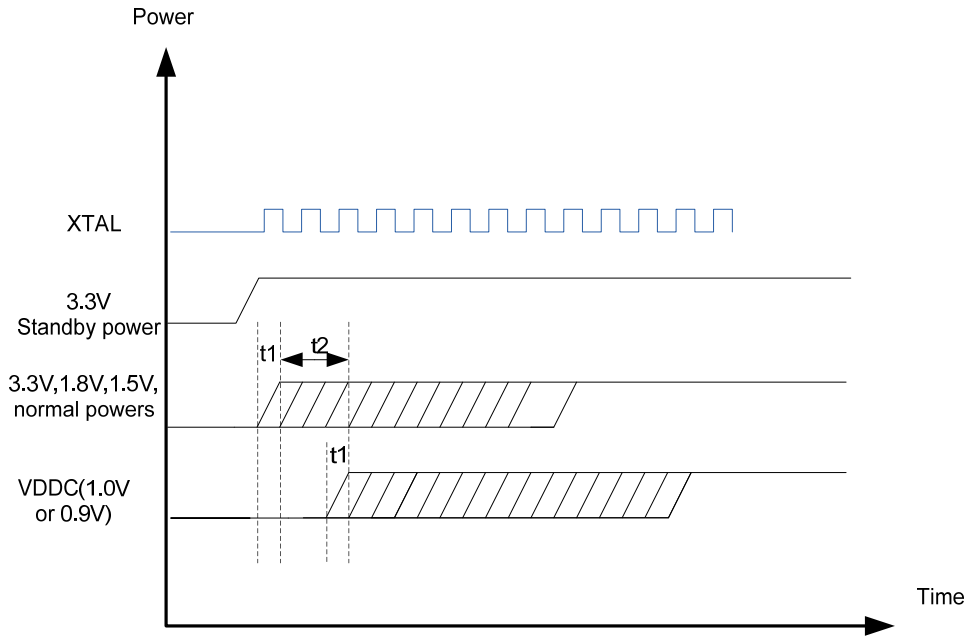
Without external Reset IC with External LDO

The timing is shown as Figure 3. The power waveform must satisfy Figure 3 with parameters listed in Table 1.



Note:

***3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)**

***1.0V/0.9V (VDD, DVDD_DDR, DVDD_DDR_RX)**

***1.5V (VDDIO_DATA, VDDIO_CMD)**

***1.8V (VDDP_2)**

***3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)**

Figure 3: Power on Sequence

Table 2: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	Normal 3.3V, 1.8V, 1.5V, VDDC power rising time (0% to 100%)	—	—	20	ms
t_2	Normal 3.3V, 1.8V, 1.5V to VDDC lead time	1	—	—	ms

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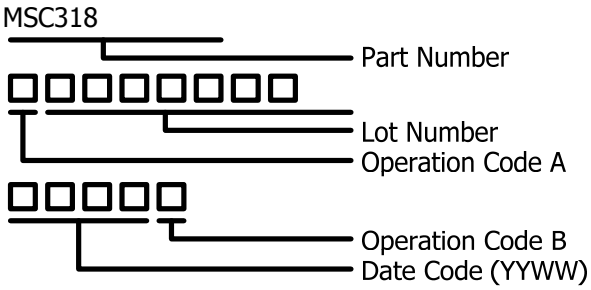
ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MSC318	-40°C to +85°C	BGA	286-ball

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MSC318 comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

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