

MSC313E
High-Integrated IP Camera SoC
Processor

Preliminary Product Brief Version 0.3

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REVISION HISTORY

Revision No.	Description	Date
0.1	Y Initial release	01/06/2017
0.2	Y Updated Functional Description for clarity	04/11/2017
	Y Updated Pin Description: Pin #3 and #77	
	Y Updated Electrical Specifications	
0.3	Y Updated Block Diagram	05/03/2017
	Y Updated Electrical Specifications	

FEATURES

- n High Performance Processor Core
 - Ÿ ARM Cortex-A7 Single Core
 - Ÿ Neon and FPU
 - Ÿ Memory Management Unit for Linux support
 - Ÿ DMA Engine
- n Image/Video Processor
 - Ÿ Supports 10-bit parallel interface for raw data input
 - Ÿ Supports MIPI interface with 2 data lanes and 1 clock lane
 - Ÿ Supports 8/10-bit CCIR656 interface
 - Ÿ Supports 1920x1080p20fps+CIF20fps video recording
 - Ÿ Supports image snapshot (resolution will be the same with the 2nd video stream if the main video stream is 1920x1080)
 - Ÿ Bad pixel compensation
 - Ÿ Noise Reduction (NR)
 - Ÿ Optical black correction
 - Ÿ Lens shading compensation
 - Ÿ Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
 - Ÿ CFA color interpolation
 - Ÿ Color correction
 - Ÿ Gamma correction
 - Ÿ Video stabilization
 - Ÿ Wide Dynamic Range
 - Ÿ Rotation with 90 or 270 degree
 - Ÿ Lens distortion correction
 - Ÿ Fully programmable multi-function scaling engines
- n MStar Advanced Color Engine (MStarACE)
 - Ÿ Luma gain/offset adjustment
 - Ÿ Supports 2D peaking
 - Ÿ Horizontal noise masking
 - Ÿ Direct Luma Correction (DLC)
 - Ÿ Black/White Level Extension (BLE/WLE)
 - Ÿ IHC/ICC/IBC for chroma adjustment
 - Ÿ Histogram statistics
- n H.265/HEVC Encoder
 - Ÿ Supports H.265/HEVC baseline and main profile encoding
 - Ÿ Supports MVs: 32x32, 16x16, 8x8
 - Ÿ Supports up to quarter-pixel
 - Ÿ Supports one reference frame
 - Ÿ Supports Max. 1920x1080p20fps encoding
- n H.264 Encoder
 - Ÿ Supports H.264 baseline and main profile encoding
 - Ÿ Supports MVs: 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, 4x4
 - Ÿ Supports up to quarter-pixel
 - Ÿ Supports two reference frames
 - Ÿ Supports rate control and ROI
 - Ÿ Supports Max. 1920x1080p20fps encoding
- n JPEG Encoder
 - Ÿ Supports JPEG baseline encoding
 - Ÿ Supports YUV422 or YUV420 formats
 - Ÿ Supports Max. 1280x960p30fps encoding
- n Video Encoding Performance
 - Ÿ Supports 1920x1080p20fps (or 1280x960p30) + CIFp30 H.265 (or H.264) encoding
 - Ÿ Supports MJPEG 1M (1280x720) 30fps encoding (the resolution will be the same with the 2nd video stream if the 1st stream is 1920x1080)
- n Audio Processor
 - Ÿ One ADC for microphone input
 - Ÿ One DAC for lineout
 - Ÿ Supports 8K/16K/32KHz sampling rate audio recording
 - Ÿ Digital and analog gain adjustment
- n NOR Flash Interface
 - Ÿ Compliant with standard and dual SPI Flash memory components

n SDIO 2.0 Interface

- Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
- Compatible with SD spec. 2.0, data bus 1/4 bit mode

n USB 2.0 Interface

- One USB 2.0 host
- Supports EHCI specification

n DRAM Memory

- Embedded DDR2 DRAM memory
- Memory size up to 512Mb

n Connectivity

- Built-in 10/100M Ethernet MAC and Ethernet PHY
- One USB 2.0 Host Controller could be used for USB Wi-Fi Dongle or Module
- One SDIO 2.0 Host Controller could be used for SDIO Wi-Fi module
- Supports Wakeup on LAN (WOL)

n Security Engines

- Supports AES/DES/TDES
- Supports secure booting

n Peripherals

- Two generic UARTs and one fast UART with flow control
- Three generic timers and one watchdog timer
- One SPI masters
- One I2C Masters
- Built-in SAR ADC with 3 channels analog inputs for different kinds of applications
- One IR input

n Operating Voltage Range

- Core: 0.9V
- I/O: 1.8 ~ 3.3V
- DRAM: 1.8V
- Power Consumption: TBD

n Package

- S2QFN, 8mm x 8mm

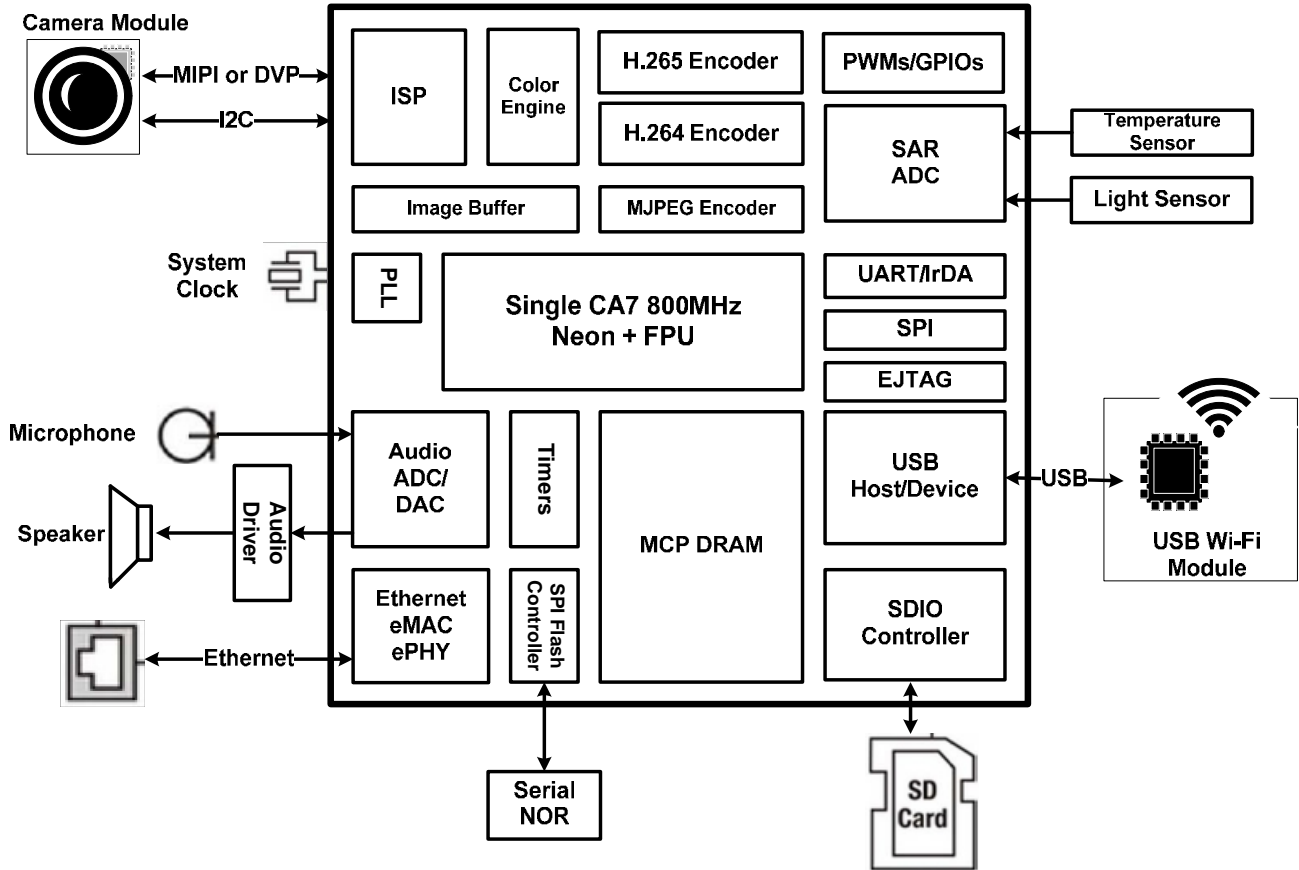
GENERAL DESCRIPTIONS

The MSC313E is a highly integrated SOC. Based on ARM Cortex-A7, the MSC313E integrates Image Signal Processor (ISP), Color Engine, Video (H.265/H.264/MJPEG) Encoders and other useful peripherals for IP camera applications.

A typical utilization of the MSC313E application processor is demonstrated in the following block diagram. The complete system includes a camera module (CMOS sensor), a connectivity module (WiFi or Ethernet), and a non-volatile storage (NOR flash or SD card). The ISP and Color Engine handle images captured from the camera sensor, and the video stream is composed of lots of frames. There are pre- and post-video processing stages. The pre-video processing rotates images, reduces noises, enhances signals and translates color domains. The post-video processing corrects lens distortion, adjusts color quality, and generates multiple video streams with different resolutions. Multimedia Encoders can compress those video streams with different compressing standards at the same time. The well compressed video/audio streams could be streamed or stored in the cloud server through Wi-Fi or Ethernet or stored in a local SD Card. The NOR flash is usually reserved for operating system and application software. Moreover, other peripherals like SAR/Audio ADC, UARTs and SPI are supported to realize applications with maximal flexibility.

Besides, the MSC313E supports secure booting and personalization authentication mechanism for securing system. The AES/DES/3DES cipher engines could also help encrypt the compressed video/audio streams to protect privacy.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Video Encoder

I. JPE Feature Description

n JPE features

- ÿ Supports JPEG encoding 3Mp
 - Frame mode
 - IMI row mode
- ÿ Supports YUYV input format
- ÿ Supports NV12 input format
- ÿ Supports DCT mode to accelerate SW encoding

II. H.264 Feature Description

n H.264 features

- ÿ Supports H264 baseline encoding
- ÿ Supports MVs: 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, 4x4
- ÿ Supports up to quarter-pel
- ÿ Supports up to two reference frames
- ÿ Max resolutions
 - H264 supported are 2Mp
- ÿ Frame-level & mb-level rate control
- ÿ Supports YUYV input format
- ÿ Supports NV12 input format
- ÿ Supports 16/235 and 0/255 Range Converter
- ÿ Supports cost-penalty adjustment
- ÿ Supports force zero-motion
- ÿ Supports intra16x16 planar mode

n Stream combination

- ÿ 2M@20fps
- ÿ 960p@30fps+VGA@30fps+CIF@30fps
- ÿ 960p@30fps+D1@30fps

III. H.265 Brief Feature Description

n Stream combination

- ÿ 2M@20fps
- ÿ 960p@30fps+VGA@30fps+CIF@30fps
- ÿ 960p@30fps+D1@30fps

ISP

I. Brief Feature Description

The ISP design is used to transfer raw sensor data output to YUV data and also supports YUV sensor at ISP bypass mode default.

- ÿ Supports to FHD@30, sensor input
- ÿ Fix pattern noise correction
- ÿ Bad pixel compensation
- ÿ Green equal
- ÿ Supports rgbir2x2 or rgbir4x4 mode input
- ÿ Optical black correction
- ÿ Len shading compensation
- ÿ Asymmetric Lens shading compensation
- ÿ Statistic for AWB/AE/AF
- ÿ Bayer domain de-noise
- ÿ Supports Bayer domain rotation
- ÿ White Balance PreGain and PostGain can be enable at the same time.
- ÿ CFA color interpolation
- ÿ Gamma correction
- ÿ Video stabilization statistic
- ÿ Supports menuload for ALSC_gain/DefectPxl/Gamma table

Peripheral

I. USB Brief Feature Description

One port of host/OTG controller and one port of host only controller are fully compliant with the USB 2.0 specification and the Enhanced Host Controller Interface (EHCI) specification. This Host/OTG Controller can support FS/LS transactions, Interrupt/Control/Bulk transfers and split/preamble transactions for hub.

II. MIPI CSI Interface

The features are listed below:

- ÿ CSI-2 1.1/D-PHY 1.1 compliant receiver with maximum Input Frequency 1GHz
- ÿ Supports 1 clock lane, 2 data lanes
- ÿ Supports YUV422 8-bit, Raw8, Raw10, Raw12, Generic 8-bit long packet and User defined byte-based data type
- ÿ Supports 1-bit error correction/2-bit error detection for packet header
- ÿ Supports checksum error detection for payload data
- ÿ Supports timing generation for Vsync and Hsync

III. Ethernet MAC Brief Feature Description

- ÿ IEEE Std 802.3 compatible
- ÿ Supports 10/100 Mbit/s operation.
- ÿ Full/Half duplex support.
- ÿ Automatic pad and CRC generation on transmitted packet.

- ÿ Supports transmit packet(IP/TCP/UDP) checksum generate
- ÿ Receiver & Transmitter Packet management by internal storage with descriptor header control
- ÿ Internal async-FIFO for receiver & transmitter frame wire speed operation
- ÿ Supports Tagged frame
- ÿ Supports IPV6 check-sum
- ÿ Supports IEEE802.3az EEE function

IV. EPHY Brief Feature Description

The Ethernet PHY (EPHY) is an IEEE 802.3 compliant single-port Ethernet Transceiver for both 100Mbps and 10Mbps operations. The EPHY acts as an interface between the physical signaling and the Media Access Controller (MAC). It supports the Auto-Negotiation function to simplify the network installation and maintenance.

The major functions of EPHY included:

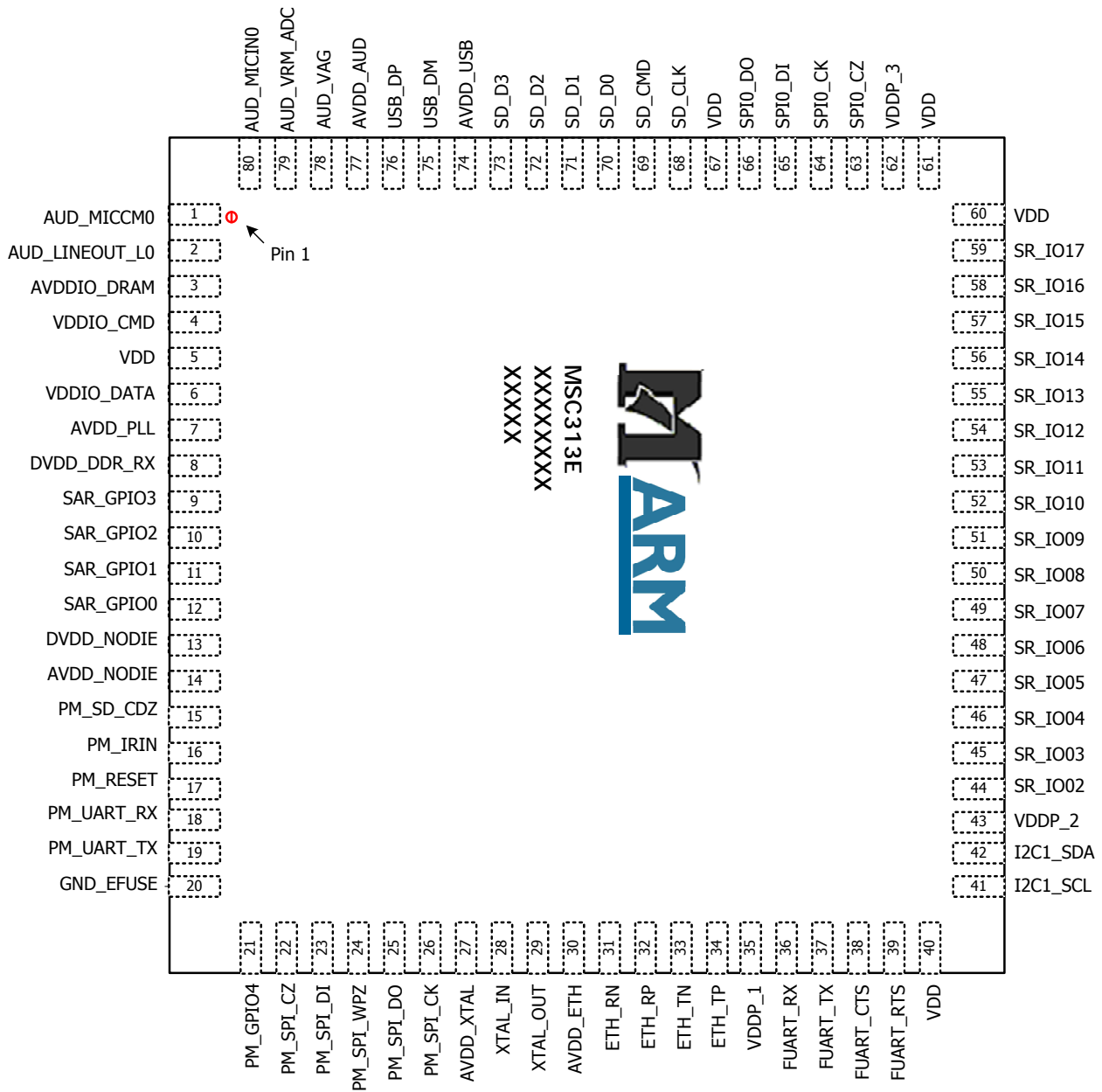
- ÿ 10/100Mbps TX/RX
- ÿ Full-duplex or half duplex
- ÿ Supports IEEE 802.3u auto-negotiation
- ÿ DSP-based PHY Transceiver technology
- ÿ Supports WOL (Wake on Lan) feature (Magic Packet only)
- ÿ Supports IEEE 802.3az EEE function

V. Encryption Brief Feature Description

AESDMA is a secure IP for Secure Boot and HDMI Key Authentication. There are three engines inside this IP:

- ÿ AES: ECB, CBC (dvs042), ECB_CTS, CBC_CTS, CTR
- ÿ SHA: SHA_1, SHA_256
- ÿ RSA: RSA_2048 in HW key mode, programmable size in SW key mode

PIN DIAGRAM (MSC313E)



PIN CHARACTERISTICS

QFN Pin Location	Pin Name	Multi Function	IO Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
9	PAD_SAR_GPIO3	SAR_ASI3 SAR_GPIO[3]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
10	PAD_SAR_GPIO2	SAR_ASI2 SAR_GPIO[2]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
11	PAD_SAR_GPIO1	SAR_ASI1 SAR_GPIO[1]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
12	PAD_SAR_GPIO0	SAR_ASI0 SAR_GPIO[0]	AVDD_NODIE	>4mA	Hi-Z	Hi-Z	Yes
15	PAD_PM_SD_CDZ	SD_CDZ SD_CDZ_GPIO	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
16	PAD_PM_IRIN	IRIN IRIN_GPIO	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
17	PAD_PM_RESET	HW_RESET	AVDD_NODIE		PD=64kohm (±15%)/52uA(±15%)	PD	Yes
18	PAD_PM_UART_RX	UART_RX	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
19	PAD_PM_UART_TX	UART_TX	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
21	PAD_PM_GPIO4	GPIO_PM[4]	AVDD_NODIE	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
22	PAD_PM_SPI_CZ	SPI_CZ1 SPI_CZ2 SPI_GPIO[0]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
23	PAD_PM_SPI_DI	SPI_DI SPI_GPIO[2]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
24	PAD_PM_SPI_WPZ	SPI_WPZ SPI_GPIO[4]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
25	PAD_PM_SPI_DO	SPI_DO SPI_GPIO[3]	AVDD_NODIE	>4mA/8mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
26	PAD_PM_SPI_CK	SPI_CK SPI_GPIO[1]	AVDD_NODIE	>4mA/8mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
28	PAD_XTAL_IN	XTAL_IN	AVDD_XTAL				
29	PAD_XTAL_OUT	XTAL_OUT	AVDD_XTAL				
31	PAD_ETH_RN	ETH_RN ETH_GPIO[0]	AVDD_ETH				
32	PAD_ETH_RP	ETH_RP ETH_GPIO[1]	AVDD_ETH				
33	PAD_ETH_TN	ETH_TN ETH_GPIO[2]	AVDD_ETH				
34	PAD_ETH_TP	ETH_TP ETH_GPIO[3]	AVDD_ETH				
36	PAD_FUART_RX	FUART_RX UART0_RX EJ_TCK SPI0_CZ PWM0 FUART_GPIO[0]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes

QFN Pin Location	Pin Name	Multi Function	IO Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
37	PAD_FUART_TX	FUART_TX UART0_TX EJ_TMS SPI0_CK PWM1 FUART_GPIO[1]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
38	PAD_FUART_CTS	FUART_CTS UART1_RX EJ_TDO SPI0_DI PWM2 FUART_GPIO[2]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
39	PAD_FUART_RTS	FUART_RTS UART1_TX EJ_TDI SPI0_DO PWM3 FUART_GPIO[3]	VDDP_1	>4mA	PU=86kohm (±15%)/39uA(±15%)	PU	Yes
41	PAD_I2C1_SCL	I2C1_SCL SR_SCL I2C1_GPIO[0]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
42	PAD_I2C1_SDA	I2C1_SDA SR_SDA I2C1_GPIO[1]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
44	PAD_SR_IO02	SR_D[9] SR_D[8] SR_D[4] SR_HS SR_D[2] CCIR_IN_D[0] SR_GPIO[2]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
45	PAD_SR_IO03	SR_D[7] SR_D[6] SR_D[2] SR_D[0] SR_D[3] CCIR_IN_D[1] SR_GPIO[3]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
46	PAD_SR_IO04	SR_PCK SR_D[4] SR_D[1] CCIR_IN_D[2] SR_GPIO[4]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
47	PAD_SR_IO05	SR_D[1] SR_D[2] SR_D[0] SR_D[5] CCIR_IN_D[3] SR_GPIO[5]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No

QFN Pin Location	Pin Name	Multi Function	IO Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
48	PAD_SR_IO06	SR_D[0] SR_PCK SR_D[2] SR_D[3] SR_D[6] CCIR_IN_D[4] SR_GPIO[6]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
49	PAD_SR_IO07	SR_D[3] SR_D[1] SR_PCK SR_D[9] SR_D[4] SR_D[7] CCIR_IN_D[5] SR_GPIO[7]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
50	PAD_SR_IO08	SR_D[5] SR_D[0] SR_D[1] SR_D[3] SR_D[8] CCIR_IN_D[6] SR_GPIO[8]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
51	PAD_SR_IO09	SR_D[4] SR_D[9] SR_D[7] SR_D[6] CCIR_IN_D[7] SR_GPIO[9]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
52	PAD_SR_IO10	SR_D[6] SR_D[3] SR_D[5] SR_RST SR_MCK SR_D[10] CCIR_IN_D[8] SR_GPIO[10]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
53	PAD_SR_IO11	SR_MCK SR_D[7] SR_D[3] SR_D[5] SR_D[11] CCIR_IN_D[9] SR_GPIO[11]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
54	PAD_SR_IO12	SR_HS SR_RST SR_D[9] SR_VS SR_D[8] SR_PDN CCIR_IN_CLK SR_GPIO[12]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
55	PAD_SR_IO13	SR_VS SR_D[5] SR_HS SR_D[9] SR_RST SR_GPIO[13]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No

QFN Pin Location	Pin Name	Multi Function	IO Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
56	PAD_SR_IO14	SR_D[8] SR_VS SR_PDN SR_D[10] SR_HS SR_GPIO[14]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
57	PAD_SR_IO15	SR_D[2] SR_HS SR_MCK SR_D[11] SR_PCK SR_GPIO[15]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
58	PAD_SR_IO16	SR_PDN SR_PCK SR_VS SR_GPIO[16]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
59	PAD_SR_IO17	SR_RST SR_MCK SR_GPIO[17]	VDDP_2	>4mA/8mA	Option PU = 90kohm (+/-15%) Option PD = 64kohm (+/-15%)	PU	No
63	PAD_SPI0_CZ	SPI0_CZ TTL_B[7] PWM4 SPI0_GPIO[0]	VDDP_3	>4mA/8mA/1 2mA/16mA	PU=86kohm (±15%)/39uA(±15%)	PU	No
64	PAD_SPI0_CK	SPI0_CK TTL_LCK PWM5 SPI0_GPIO[1]	VDDP_3	>4mA/8mA/1 2mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
65	PAD_SPI0_DI	SPI0_DI TTL_LVSYNC PWM6 SPI0_GPIO[2]	VDDP_3	>4mA/8mA/1 2mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
66	PAD_SPI0_DO	SPI0_DO TTL_LHSYNC PWM7 SPI0_GPIO[3]	VDDP_3	>4mA/8mA/1 2mA/16mA	PD=64kohm (±15%)/52uA(±15%)	PD	No
68	PAD_SD_CLK	SDIO_CLK SD_GPIO[0]	VDDP_3	>4mA/8mA	PD=64kohm (±15%)/52uA(±15%)	PD	Yes
69	PAD_SD_CMD	SDIO_CMD SD_GPIO[1]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
70	PAD_SD_D0	SPI1_CZ SDIO_D[0] SD_GPIO[2]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
71	PAD_SD_D1	SPI1_CK SDIO_D[1] SD_GPIO[3]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
72	PAD_SD_D2	SPI1_DI SDIO_D[2] SD_GPIO[4]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
73	PAD_SD_D3	SPI1_DO SDIO_D[3] SD_GPIO[5]	VDDP_3	>4mA/8mA	Option PU=86kohm (±15%)/39uA(±15%)	Hi-Z	Yes
75	PAD_USB_DM	USB_DM USB_GPIO[0]	AVDD_USB	>4mA	Hi-Z		

QFN Pin Location	Pin Name	Multi Function	IO Power	Driving Capability	Pull Resistor	Core-Off Status	5V-Tolerant
76	PAD_USB_DP	USB_DP USB_GPIO[1]	AVDD_USB	>4mA	Hi-Z		
78	PAD_AUD_VAG	AUD_VAG	AVDD_AUD				
79	PAD_AUD_VRM_A DC	AUD_VRM_ADC	AVDD_AUD				
79	PAD_AUD_VRM_D AC	AUD_VRM_DAC	AVDD_AUD				
80	PAD_AUD_MICIN 0	AUD_MICIN0	AVDD_AUD				
1	PAD_AUD_MICCM 0	AUD_MICCM0	AVDD_AUD				
2	PAD_AUD_LINEO UT_L0	AUD_LINEOUT_L0	AVDD_AUD				
5, 40, 60, 61, 67	VDD						
3	AVDDIO_DRAM						
8	DVDD_DDR						
8	DVDD_DDR_RX						
14	DVDD_NODIE						
77	AVDD_AUD						
31	AVDD_ETH						
13	AVDD_NODIE						
7	AVDD_PLL						
74	AVDD_USB						
27	AVDD_XTAL						
4	VDDIO_CMD						
6	VDDIO_DATA						
35	VDDP_1						
43	VDDP_2						
62	VDDP_3						
EPAD	VSS						

SIGNAL DESCRIPTION

Image Sensor

Signal Name	Signal Type	Function	Pin Location
SR_D[0]	Input	Image Sensor Data Bus	48, 50, 47
SR_D[1]	Input	Image Sensor Data Bus	47, 49, 50
SR_D[2]	Input	Image Sensor Data Bus	57, 47, 48
SR_D[3]	Input	Image Sensor Data Bus	49, 52, 53
SR_D[4]	Input	Image Sensor Data Bus	51, 46, 46
SR_D[5]	Input	Image Sensor Data Bus	50, 55, 52
SR_D[6]	Input	Image Sensor Data Bus	52, 45, 45
SR_D[7]	Input	Image Sensor Data Bus	45, 53, 51
SR_D[8]	Input	Image Sensor Data Bus	56, 44, 44
SR_D[9]	Input	Image Sensor Data Bus	44, 51, 54
SR_HS	Input	Image Sensor Horizontal Sync Signal	54, 57, 55
SR_VS	Input	Image Sensor Vertical Sync Signal	55, 56, 56
SR_PCK	Input	Image Sensor Pixel Clock	46, 48, 49
SR_PDN	Output	Image Sensor Power Down Control	58, 58, 58
SR_RST	Output	Image Sensor Reset Control	59, 54, 59
SR_MCK	Output	Image Sensor Reference Clock	53, 59, 57
SR_SCL	Output	Image Sensor I2C Serial Clock	41
SR_SDA	Input/Output	Image Sensor I2C Serial Data	42

CCIR Sensor

Signal Name	Signal Type	Function	Pin Location
CCIR_IN_D[0]	Input	CCIR Data Bus	44
CCIR_IN_D[1]	Input	CCIR Data Bus	45
CCIR_IN_D[2]	Input	CCIR Data Bus	46
CCIR_IN_D[3]	Input	CCIR Data Bus	47
CCIR_IN_D[4]	Input	CCIR Data Bus	48
CCIR_IN_D[5]	Input	CCIR Data Bus	49
CCIR_IN_D[6]	Input	CCIR Data Bus	50
CCIR_IN_D[7]	Input	CCIR Data Bus	51
CCIR_IN_D[8]	Input	CCIR Data Bus	52
CCIR_IN_D[9]	Input	CCIR Data Bus	53
CCIR_IN_CLK	Input	CCIR Sample Clock	54

Audio Interface

Signal Name	Signal Type	Function	Pin Location
AUD_LINEOUT_L0	Output	Audio Left Channel Line Output	2
AUD_VAG	Output	Audio Reference Voltage from 1/2 AVDD_AUD	78
AUD_VRM_ADC	Input	Audio Reference Voltage for ADC	79
AUD_VRM_DAC	Input	Audio Reference Voltage for DAC	79
AUD_MICIN0	Input	Audio Left Channel Microphone Positive Input	80
AUD_MICCM0	Input	Audio Left Channel Microphone Negative Input	1

10/100 Ethernet Interface

Signal Name	Signal Type	Function	Pin Location
ETH_RN	Input	10/100 Ethernet Negative Receiving Input	31
ETH_RP	Input	10/100 Ethernet Positive Receiving Input	32
ETH_TN	Output	10/100 Ethernet Negative Transmitting Output	33
ETH_TP	Output	10/100 Ethernet Positive Transmitting Output	34

SDIO Interface

Signal Name	Signal Type	Function	Pin Location
SDIO_CLK	Output	SDIO 2.0 Clock	68
SDIO_CMD	Output	SDIO 2.0 Command	69
SDIO_D[0]	Input/Output	SDIO 2.0 Data Bus	70
SDIO_D[1]	Input/Output	SDIO 2.0 Data Bus	71
SDIO_D[2]	Input/Output	SDIO 2.0 Data Bus	72
SDIO_D[3]	Input/Output	SDIO 2.0 Data Bus	73
SD_CDZ	Input	SD Card Detect (active low)	15

SPI Flash Interface

Signal Name	Signal Type	Function	Pin Location
SPI_CK	Output	SPI Flash Clock	26
SPI_CZ1	Output	SPI Flash Chip Select 1 (active low)	22
SPI_DI	Output	SPI Flash Serial Data To Device	23
SPI_DO	Input	SPI Flash Serial Data From Device	25
SPI_WPZ	Output	SPI Flash Write Protect Control (active low)	24

USB 2.0 Interface

Signal Name	Signal Type	Function	Pin Location
USB_DM	Input/Output	USB 2.0 Inverting Data	75
USB_DP	Input/Output	USB 2.0 Non-inverting Data	76

Master SPI Interface

Signal Name	Signal Type	Function	Pin Location
SPI0_CZ	Output	Master SPI 0 Chip Select (active low)	63
SPI0_CK	Output	Master SPI 0 Serial Clock	64
SPI0_DI	Output	Master SPI 0 Serial Data In	65
SPI0_DO	Input	Master SPI 0 Serial Data Out	66

Master I2C Interface

Signal Name	Signal Type	Function	Pin Location
I2C1_SCL	Output	Master I2C 1 Serial Clock	41
I2C1_SDA	Input/Output	Master I2C 1 Serial Data	42

UART Interface

Signal Name	Signal Type	Function	Pin Location
UART_RX0	Input	UART 0 Receiver	36
UART_TX0	Output	UART 0 Transmitter	37
UART_RX1	Input	UART 1 Receiver	38
UART_TX1	Output	UART 1 Transmitter	39

Fast UART Interface

Signal Name	Signal Type	Function	Pin Location
FUART_RX	Input	Fast UART Receiver	36
FUART_TX	Output	Fast UART Transmitter	37
FUART_CTS	Input	Fast UART Clear to Set	38
FUART_RTS	Output	Fast UART Request to Set	39

IR Interface

Signal Name	Signal Type	Function	Pin Location
IRIN	Input	IR Receiver	16

SAR Interface

Signal Name	Signal Type	Function	Pin Location
SAR_ASI0	Input	SAR Analog Signal Channel 0	12
SAR_ASI1	Input	SAR Analog Signal Channel 1	11
SAR_ASI2	Input	SAR Analog Signal Channel 2	10
SAR_ASI3	Input	SAR Analog Signal Channel 3	9

System

Signal Name	Signal Type	Function	Pin Location
PAD_XTAL_IN	Input	24MHz Crystal Output	28
PAD_XTAL_OUT	Output	24MHz Crystal Input	29
HW_RESET	Input	Chip Reset (active high)	17
UART_RX	Input	Debug Port for UART Receiver or Slave I2C Serial Clock	18
UART_TX	Output	Debug Port for UART Transmitter or Slave I2C Serial Data	19
GND_EFUSE	Input	Power Source if eFuse Burning (connect to ground)	20

GPIO Interface

Signal Name	Signal Type	Function	Pin Location
FUART_GPIO[0]	Input/Output	General Purpose Input/Output	36
FUART_GPIO[1]	Input/Output	General Purpose Input/Output	37
FUART_GPIO[2]	Input/Output	General Purpose Input/Output	38
FUART_GPIO[3]	Input/Output	General Purpose Input/Output	39
I2C0_GPIO[0]	Input/Output	General Purpose Input/Output	41
I2C0_GPIO[1]	Input/Output	General Purpose Input/Output	42
SPI0_GPIO[0]	Input/Output	General Purpose Input/Output	63
SPI0_GPIO[1]	Input/Output	General Purpose Input/Output	64
SPI0_GPIO[2]	Input/Output	General Purpose Input/Output	65
SPI0_GPIO[3]	Input/Output	General Purpose Input/Output	66
SD_GPIO[0]	Input/Output	General Purpose Input/Output	68
SD_GPIO[1]	Input/Output	General Purpose Input/Output	69
SD_GPIO[2]	Input/Output	General Purpose Input/Output	70
SD_GPIO[3]	Input/Output	General Purpose Input/Output	71

Signal Name	Signal Type	Function	Pin Location
SD_GPIO[4]	Input/Output	General Purpose Input/Output	72
SD_GPIO[5]	Input/Output	General Purpose Input/Output	73
SR_GPIO[2]	Input/Output	General Purpose Input/Output	44
SR_GPIO[3]	Input/Output	General Purpose Input/Output	45
SR_GPIO[4]	Input/Output	General Purpose Input/Output	46
SR_GPIO[5]	Input/Output	General Purpose Input/Output	47
SR_GPIO[6]	Input/Output	General Purpose Input/Output	48
SR_GPIO[7]	Input/Output	General Purpose Input/Output	49
SR_GPIO[8]	Input/Output	General Purpose Input/Output	50
SR_GPIO[9]	Input/Output	General Purpose Input/Output	51
SR_GPIO[10]	Input/Output	General Purpose Input/Output	52
SR_GPIO[11]	Input/Output	General Purpose Input/Output	53
SR_GPIO[12]	Input/Output	General Purpose Input/Output	54
SR_GPIO[13]	Input/Output	General Purpose Input/Output	55
SR_GPIO[14]	Input/Output	General Purpose Input/Output	56
SR_GPIO[15]	Input/Output	General Purpose Input/Output	57
SR_GPIO[16]	Input/Output	General Purpose Input/Output	58
SR_GPIO[17]	Input/Output	General Purpose Input/Output	59
USB_GPIO[0]	Input/Output	General Purpose Input/Output	75
USB_GPIO[1]	Input/Output	General Purpose Input/Output	76
PM_GPIO[4]	Input/Output	General Purpose Input/Output	21
SD_CDZ_GPIO	Input/Output	General Purpose Input/Output	15
IRIN_GPIO	Input/Output	General Purpose Input/Output	16
SPI_GPIO[0]	Input/Output	General Purpose Input/Output	22
SPI_GPIO[1]	Input/Output	General Purpose Input/Output	26
SPI_GPIO[2]	Input/Output	General Purpose Input/Output	23
SPI_GPIO[3]	Input/Output	General Purpose Input/Output	25
SPI_GPIO[4]	Input/Output	General Purpose Input/Output	24
SAR_GPIO[0]	Input/Output	General Purpose Input/Output	12
SAR_GPIO[1]	Input/Output	General Purpose Input/Output	11
SAR_GPIO[2]	Input/Output	General Purpose Input/Output	10
SAR_GPIO[3]	Input/Output	General Purpose Input/Output	9
ETH_GPIO[0]	Input/Output	General Purpose Input/Output	31
ETH_GPIO[1]	Input/Output	General Purpose Input/Output	32
ETH_GPIO[2]	Input/Output	General Purpose Input/Output	33

Signal Name	Signal Type	Function	Pin Location
ETH_GPIO[3]	Input/Output	General Purpose Input/Output	34

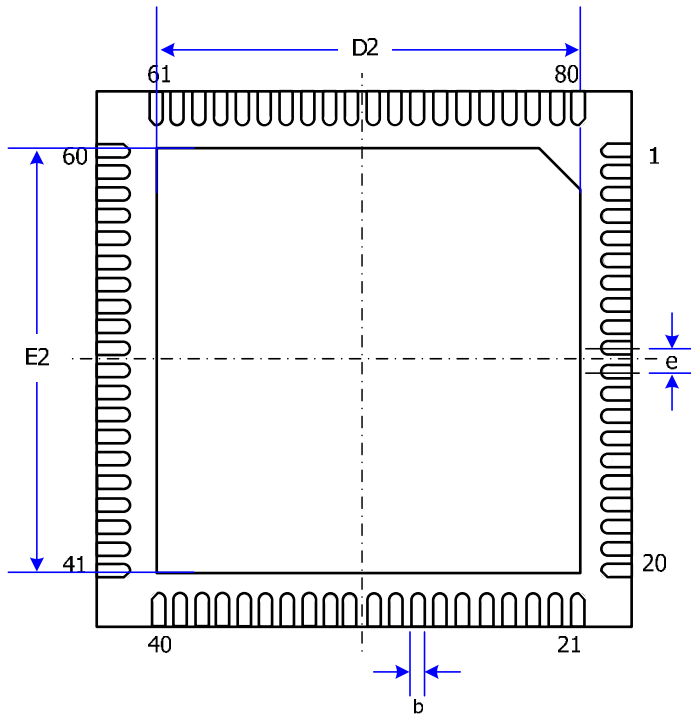
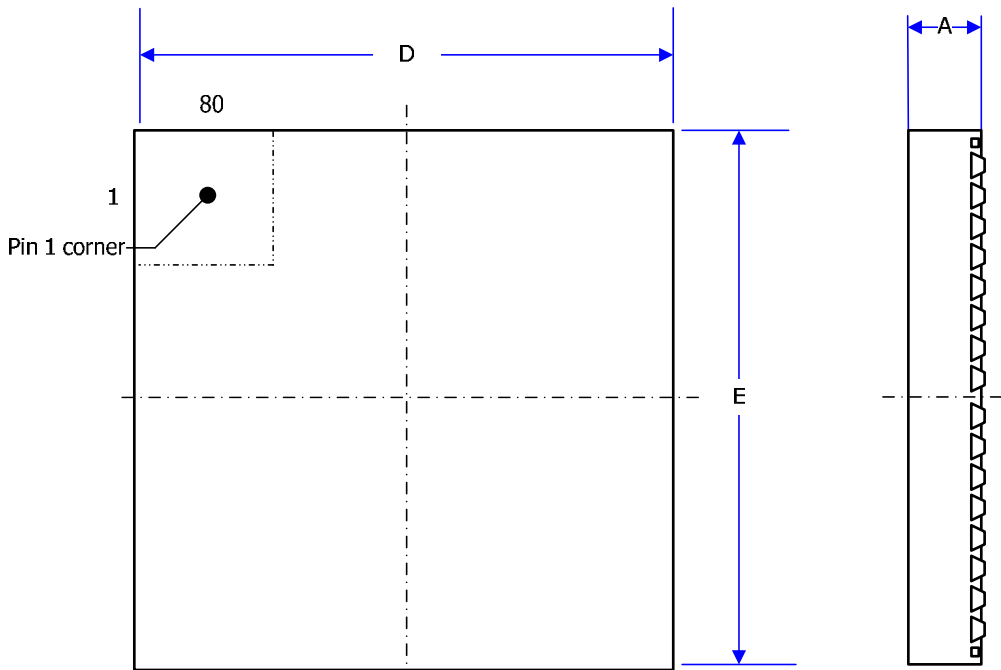
Cortex-A7 JTAG

Signal Name	Signal Type	Function	Pin Location
EJ_TCK	Input	CA7 JTAG Clock	36, 63
EJ_TMS	Intpu	CA7 JTAG Mode Select	37, 64
EJ_TDO	Output	CA7 JTAG Data Out	38, 65
EJ_TDI	Input	CA7 JTAG Data In	39, 66

Power Pins

Signal Name	Signal Type	Function	Pin Location
VDD	Input	Digital Power	5, 40, 60, 61, 67
DVDD_DDR	Input	Digital Power for DDR	8
DVDD_DDR_RX	Input	Digital Power for DDR	8
DVDD_NODIE	Output	PM LDO Output	14
AVDD_AUD	Input	Analog Power for Audio	77
AVDD_ETH	Input	Analog Power for Ethernet	31
AVDD_NODIE	Input	Analog Power for PM	13
AVDD_PLL	Input	Analog Power for PLL	7
AVDD_USB	Input	Analog Power for USB	74
AVDD_XTAL	Input	Analog Power for XTAL	27
VDDIO_CMD	Input	Analog Power for DDR	4
VDDIO_DATA	Input	Analog Power for DDR	6
VDDP_1	Input	Pad Power	35
VDDP_2	Input	Pad Power	43
VDDP_3	Input	Pad Power	62
AVDDIO_DRAM	Input	Stack DRAM Power	3

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	0.90	0.0315	0.0335	0.0354
D	-	8	-	-	0.3150	-
E	-	8	-	-	0.3150	-
D2	6.60	6.70	6.80	0.2598	0.2638	0.2677
E2	6.60	6.70	6.80	0.2598	0.2638	0.2677
b	0.13	0.18	0.23	0.0051	0.0071	0.0091
e	-	0.35	-	-	0.0138	-

Note: E-pad have to connect to system GND net.

ELECTRICAL SPECIFICATIONS

Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	V_{IH}	2.5			V
Input Voltage, Low	V_{IL}			0.8	V
Input Current, High	I_{IH}			-1.0	uA
Input Current, Low	I_{IL}			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	V_{OH}	$V_{DDP}-0.1$ ^{Note}			V
Output Voltage, Low	V_{OL}			0.1	V
SAR ADC Input		0		V_{VDD_33}	V
AUDIO OUTPUTS					
Line-Out			2.54		Vp-p

Note: 1. V_{DDP} can be V_{VDD_33} , V_{VDD_15}

2. 0.9Vrms @10Kohm load

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}		3.3		V
1.8V Supply Voltage (DDR II)	V_{VDD_18}		1.8		V
Core Power Supply Voltage (Core)	V_{VDD_core}	0.87	0.9		V
Ambient Operation Temperature	T_A	-40		85	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}			3.63	V
1.8V Supply Voltage (DDR II)	V_{VDD_18}			1.98	V
Core Power Supply Voltage (Core)	V_{VDD_core}			1.26	V
Storage Temperature	T_{STG}	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

HARDWARE POWER SEQUENCE PROCEDURE

The timing requirements of the hardware reset signal are shown as below:

Hardware Reset

HWRESET: Chip Reset; High Reset (Level)

The HWRESET pin is suggested to connect with 3.3V standby as shown in Figure 1. The V_{IH} is 2V (Typ) +/- 10% (2.2V~1.8V); the V_{IL} is 1.2V (Typ) +/- 10% (1.08V~1.32V). The power sequence is as shown in Figure 2.

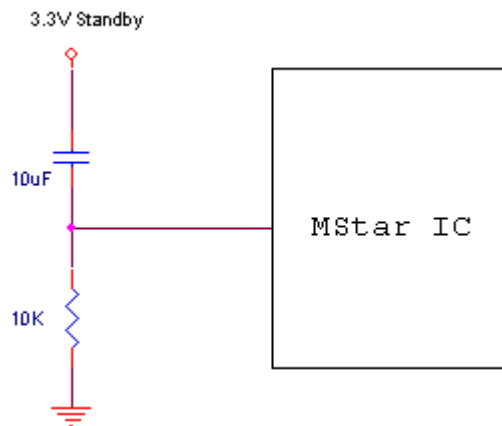
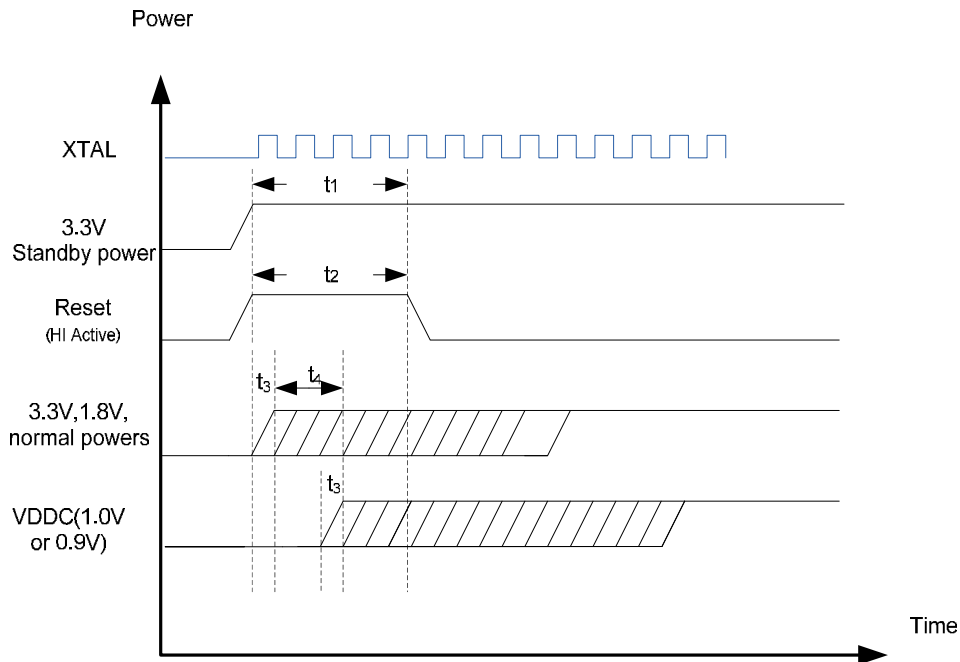


Figure 1: Reset Application Circuit

External Reset IC with External LDO

The timing is shown as Figure 2. The RST and power waveform must satisfy Figure 2 with parameters listed in Table 1.



Note:

- *3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)
- *1.0V/0.9V (VDD, DVDD_DDR_RX)
- *1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD, VDDP_2)
- *3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)

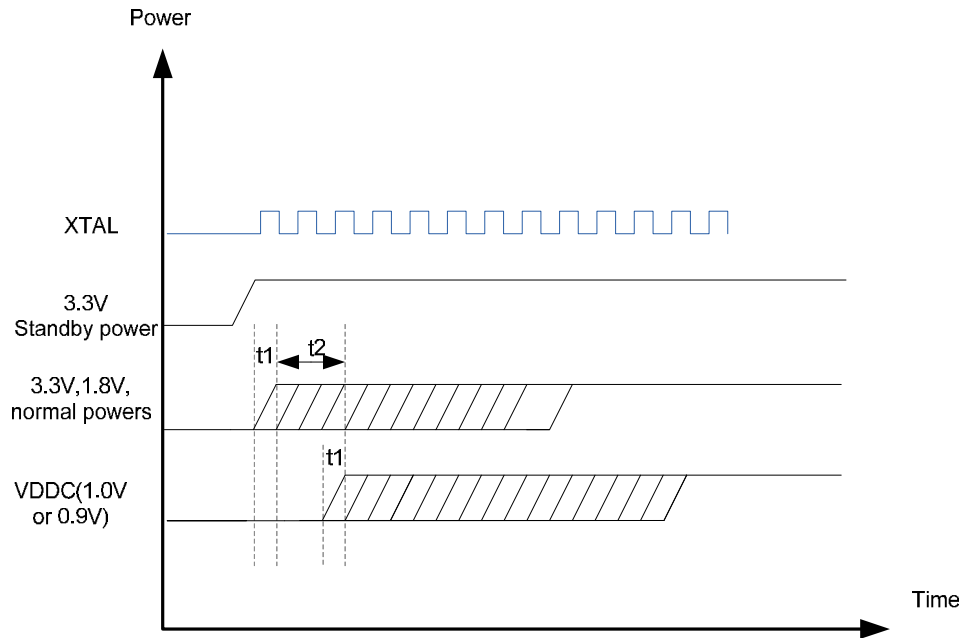
Figure 2: Power on Sequence

Table 1: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	XTAL stable to Reset falling	5	—	—	ms
t_2	Reset pulse width	5	—	—	ms
t_3	Normal 3.3V, 1.8V VDDC power rising time (0% to 100%)	—	—	20	ms
t_4	Normal 3.3V, 1.8V to VDDC lead time	1	—	—	ms

Without external Reset IC with External LDO

The timing is shown as Figure 3. The power waveform must satisfy Figure 3 with parameters listed in Table 1.



Note:

- *3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)
- *1.0V/0.9V (VDD, DVDD_DDR, DVDD_DDR_RX)
- *1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_MCLK, VDDIO_CMD, VDDP_2)
- *3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)

Figure 3: Power on Sequence

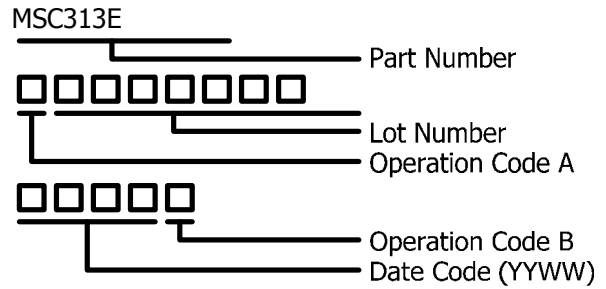
Table 2: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t ₁	Normal 3.3V, 1.8V, VDDC power rising time (0% to 100%)	—	—	20	ms
t ₂	Normal 3.3V, 1.8V to VDDC lead time	1	—	—	ms

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MSC313E	-40°C to +85°C	S2QFN	80-pin

MARKING INFORMATION



DISCLAIMER

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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MSC313E comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.