Attention Please: Under the technology license agreement between MStar and Dolby/SRS/BBE/DivX/Microsoft/QSound, MStar is obliged not to provide samples that incorporate Dolby/SRS/BBE/DivX/Microsoft/QSound technology to any third party who is not a qualified licensee of Dolby/SRS/BBE/DivX/Microsoft/QSound respectively.

FEATURES

- High Performance Micro-processor
  - ARM Cortex-A9 dual core CPU with 512KB L2 Cache
  - Memory Management Unit for Linux support
  - Six full duplex UARTs
  - DMA Engine
  - Energy-efficient management unit
- MPEG-2 Video Decoder
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Automatic frame rate conversion
  - Supports resolution up to HDTV (1080P, 1080i, 720P) and SDTV
  - Supports dual stream decoding for 3D content
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 SP and ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@30fps)
  - Supports DivX[1] Home Theater & HD profiles[Optional]
  - Supports FLV version 1.0 video format decoding
  - Supports dual stream decoding for 3D content
- VC1 Video Decoder
  - Support VC1 [Optional] video decoding up to AP@L3 and HD level
  - Supports resolutions up to HDTV (1080p@30fps)
  - Supports dual stream decoding for 3D content
- H.264 MVC Decoder
  - ITU-T H.264, ISO/IEC 14496-10 video decoding (Main and high profile up to level 4.2)
  - Support resolutions up to 1080p@30fps *2(dual view)
- H.264 Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.2) video decoding
  - Supports SVAF 2ES (for Dual Decode)
  - Profile Level 4.2
  - Supports resolutions up to 1080p@60fps
  - Supports CABAC and CAVLC stream types
  - Processing of ES and PES streams, extraction and provision of time stamps
  - Up to 50 Mbits bitrate (Blu-ray spec.)
- VP Decoder[Optional]
  - Supports VP8 (WebM)
  - Supports VP6
- AVS Decoder[Optional]
  - Supports Jizhun profile, level 6.0
  - Supports resolutions up to 1920x1088 @30fps
  - Supports bit-rate up to 40Mbps
  - Supports dual stream decoding
- RealMedia Decoder[Optional]
  - Supports maximum resolution up to 1080p@30fps
  - Supports RV8, RV9, RV10, RA8-LBR and HE-AAC decoders
  - Supports file formats with RM and RMVB
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame
  - Supports dual stream decoding for 720p@30*2
- H.264 Encoder
  - Supports H.264 baseline encoding, BP level 3.0
  - Supports MVs: 16x16, 16x8, 8x16, 8x8
  - Supports up to quarter-pel
  - Supports one reference frames
- JPEG Encoder
  - Supports Jpeg baseline encoding
  - 422 encode up to 5M(2592x1944)@7fps
  - Supports Thumbnail
  - Programmable Q-Table

[1] **Trademark of DivX, Inc.**

Optional **Please see Ordering Guide for details.**

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- Hardware JPEG Decode
  - Supports sequential mode, single scan
  - Supports both color and grayscale pictures
  - Following the file header scan the hardware decoder fully handles the decode process
  - Supports programmable Region of Interest (ROI)
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2, 1/4, 1/8
  - Supports picture rotation
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Three configurable CVBS & Y/C S-video inputs
- Sound Processor
  - Audio processing for loudspeaker channel, including volume, balance, mute, EQ controls
  - Supports digital audio format decoding:
    - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3)[Optional], AAC-LC, HE-AAC, WMA, and WMA9 Pro
  - Supports MPEG audio encoding
- Audio Interface
  - Two stereo ADC for line-in and Mic.
  - Two stereo DAC for line-out and earphone output
  - I2S digital audio input & output
  - S/PDIF digital audio output
  - Two stereo digital Mic. input
- Analog RGB Compliant Input Ports
  - Three analog ports support up to 1080P
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
- Analogue RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync Detection for H/V Sync
- MStar Advanced Color Engine (MStarACE)
  - Fully programmable multi-function scaling engine
    - Nonlinear video scaling supports various modes including Panorama
    - Supports dynamic scaling for RM, VC-1
  - Advanced video processing engine
    - 3D video deinterlacer with edge and artifact smoother
    - Edge-oriented deinterlacer with edge and artifact smoother
    - Automatic 3:2/2:2/M:N pull-down detection and recovery
    - 3D noise reduction for lousy air/cable input
    - Motion adaptive SNR
    - Arbitrary frame rate conversion
  - MStar Professional Picture Enhancement:
    - Intensified contrast and details
    - Dynamic *Vivid Skin*
    - Dynamic sharpened Luma/Chroma edges
    - Global and local dynamic depth of field perception
    - Accurate and independent color control
    - Supports sRGB and xvYCC color processing
    - Supports HDMI 1.3 deep color format
  - Programmable 12-bit RGB gamma CLUT
- LVDS Output Interface
  - Single link 8/10-bit LVDS output
  - Supports panel resolution up to 1366x768 (or 1280x800) @ 60Hz
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression
  - Supports 60Hz 3D polarizd panel (line interleave and Pixel interleave)
- TTL/DTCON Output Interface
  - Supports 8-bit TTL panel output
  - Supports 6-bit TTL panel with DTCON output

Optional **Please see Ordering Guide for details.**

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- HDMI Output Interface
  - Supports HDMI v1.4 3D format
  - Supports deep color 8/10-bit color depth per channel and resolution up to 1080p@ 60Hz or 720p/1080i @120Hz
  - Supports HDCP 1.3
  - Supports DVI 1.0
  - Supports RGB or YCbCr 444 format
  - Supports CEC
- CVBS Video Output
  - Supports all NTSC/PAL TV Standard
  - Stand-alone scaling engine
  - Programmable Hue, Contract and Brightness
- 3D-like Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill, and text draw
  - BitBlt, stretch BitBlt, trapezoid BitBlt, mirror BitBlt and rotate BitBlt
  - Supports alpha and destination alpha compare
  - Raster Operation (ROP)
  - Supports Porter-Duff
- 3D Graphic GPU
  - Supports OpenGL ES 1.1/2.0
  - Supports OpenGL VG 1.1
  - Supports rendering size up to 2Kx2K
  - Supports fill-rate up to 250M pixel/sec and polygons up to 25M tri/sec
- High-Efficiency GPS/Glonass[Optional] Baseband
  - GPS L1, C/A Code, with all-in-view processing
  - High sensitivity enabling deep indoor applications
  - Autonomous operation involving optimum use of all available assistance data
  - Fast TTFF in all modes
  - DGPS and WAAS capable

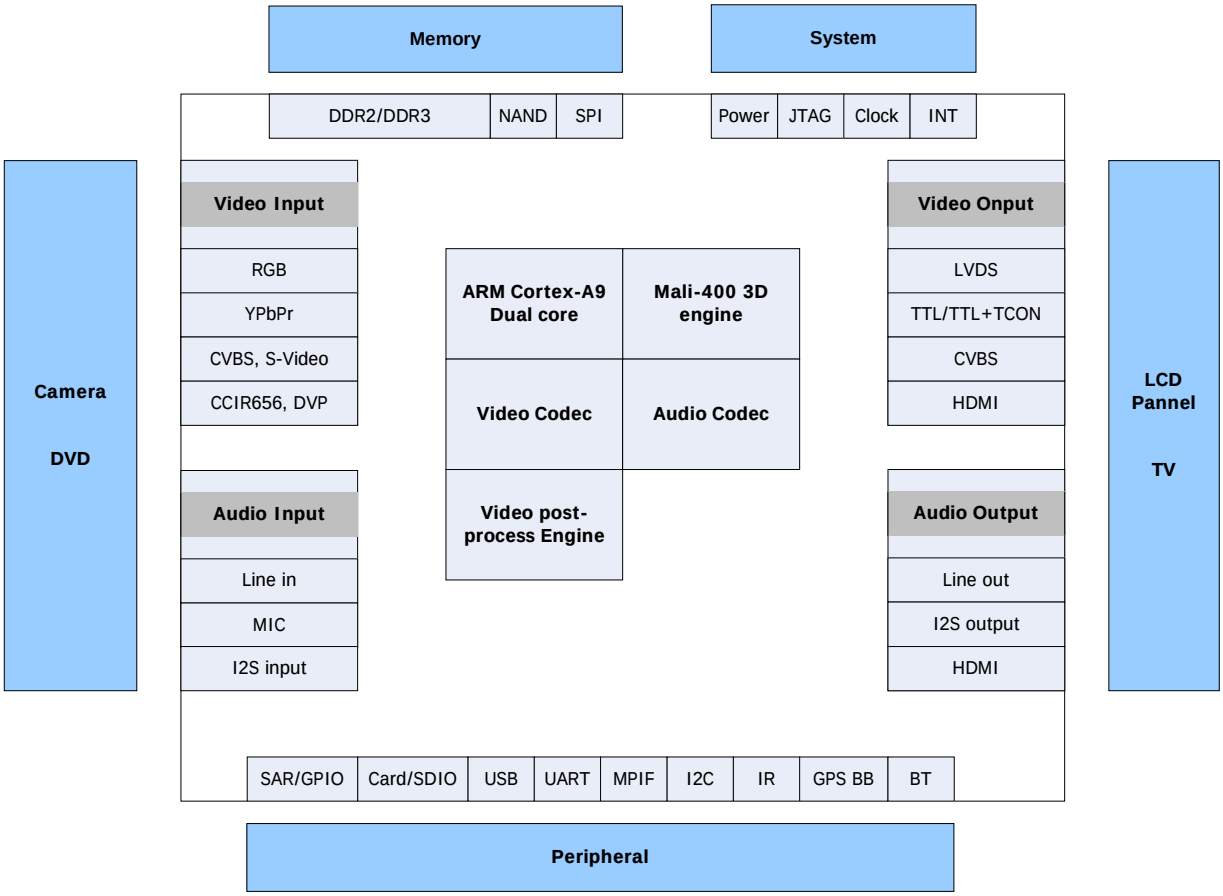
Optional **Glonass is available as option.**

- Bluetooth Mac
  - Full compliant with Bluetooth Specifications Version 2.0 EDR
  - Supports for all Bluetooth operation modes
  - Provides a programmable, interrupt-generating timer to assist Sniff, Hold or Park mode operation
  - Provides a PCM interface and sample rate conversion to transmit voice data
- Camera Sensor Interface
  - Supports 8/10-bit parallel interface
  - Supports to 5M pixel sensor output [2560x2048]
  - Bad pixel compensation
  - Bayer domain de-noise
  - Optical black correction
  - Len shading compensation
  - Auto white Balance / Auto exposure
  - CFA color interpolation
  - Gamma correction
- Flash Card and NAND Interface
  - Supports 3 SDIO ports and 1 NAND/eMMC port
  - Compatible with SDIO spec. 1.10, data bus 1/4 bit mode
  - Compatible with SD spec. 2.0, data bus 1/4 bit mode
  - Compatible with MMC spec. 4.41, data bus 1/4/8 bit mode with boot operation
  - Compatible with MS spec. 1.3, data bus 1 bit mode
  - Compatible with MSPro spec. 1.0, data bus 1/4 bit mode
  - Supports i-NAND (support eSD mode, 8bits eMMC mode)
  - Support Movi-NAND
  - Supports SLC/MLC NAND Flash (8-bit interface, and 60-bit ECC)
- USB Interface
  - Two USB 2.0 host ports – support EHCI host mode
  - One USB 2.0 host/device – support EHCI host mode or usb20 device mode

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- **Proprietary MPIF High Speed Interface**
  - Compatible with SPI (3-wire or 4-wire)
  - DMA for large amount of data transfer
  - Supports flow control with hardware CRC/checksum mechanism
- **DRAM Memory**
  - Supports DDR2-16x2 800/1066 MHz
  - Supports DDR3-16(8x2) 1600/1866 MHz
  - Supports memory size up to 1GB
- **Peripherals**
  - Up to 30 dedicated GPIOs for system control
  - Up to 6 PWMs shared with GPIO
  - Up to 6 UARTs, 2 UARTs have flow control
  - Watchdog Timer
  - SPI (CSx2) master, to support NOR flash ISP
  - Two I2C Master
  - Built-in keypad SAR and touch panel ADC
- **Real Time Clock**
  - Works with 32.768 KHz crystal
  - Alarm interrupt or wakeup
  - Tick time interrupt (millisecond)
  - Built-in regulator
- **Operating Voltage Range**
  - Core: 1.1V
  - I/O: 2.5 ~ 3.3V
  - DRAM: 1.8/1.5V
  - Power Consumption: TBD
- **Package**
  - 19 x 19 (mm) 493-ball LFBGA

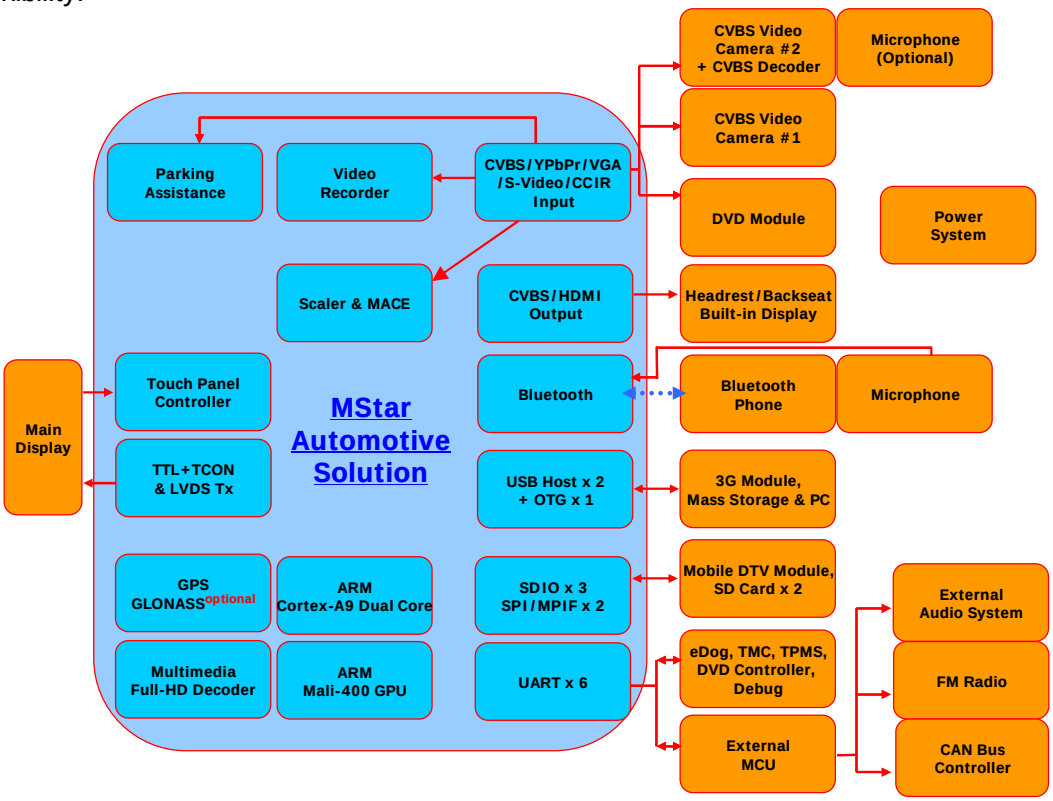
BLOCK DIAGRAM



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SYSTEM APPLICATION

The complete system includes a RF receiver, an LCD module with touch panel, a NAND flash, an SD/MMC card, a Bluetooth RF and an audio codec. External crystal of 32 kHz frequency is used to drive the Real Time Clock (RTC), which can keep time scale when the main power is off. The MST786 storage media interface supports the most popular storage cards on market, including SD/T-Flash and MMC. It also supports NAND-type flash and SPI serial flash interface. Moreover, other peripherals like UARTs and GPIOs are supported to realize applications with maximal flexibility.



GENERAL DESCRIPTION

The MST786 is a highly integrated SOC for automotive application, which incorporates a high-performance Cortex-A9 MP core, a high-efficiency GPS and Glonass[Optional] baseband, a high performance Bluetooth MAC, a DDR2/DD3 DRAM controller, a Mali-400 2D and 3D graphic accelerator for map navigation, a full HD multimedia decoder, a H.264 hardware encode for car recording, a high quality scaling engine with PIP/POP and other peripheral interfaces.

The MST786 can receive analog NTSC/PAL/SECAM CVBS and S-Video inputs from TV tuners, DVD, or CVBS video camera sources, including weak and distorted signals. Automatic gain control (AGC) and 10-bit 3-channel A/D converters provide high resolution video quantization. Built-in line-buffer supports adaptive 3D-comb-filter, sharpening, and synchronization stabler in a condensed manner. PIP/POP is provided for multimedia application when GPS map and movie play or car record. The MST786 has 2 independent output displays for front seat and back seat which can support LVDS or TTL for 1 display and the max resolution up to 1366x768(1280x800) and support HDMI or CVBS for another display and the max resolution is up to 1080P

Optional **Glonass is available as option.**

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PIN DIAGRAM (MST786)

Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	DDR3_DQ3 DDR2_DQ16 DDR3_DQ9	DDR3_DQ1 DDR2_DQ23 DDR3_DQ13	GND	DDR3_DQS0 DDR2_DQS[2] DDR3_DQS[1]	DDR3_DQ0 DDR2_DQM[2] DDR3_DQ8	DDR3_DQ6 DDR2_DQ17 DDR3_DQ10	GND	SR_RST	SR_VSYNC		SR_D4	SR_D2
B	DDR3_DQ5 DDR2_DQ21 DDR3_DQ11	DDR3_DQM0 DDR2_DQ18 DDR3_DQM[1]	DDR3_DQ1 DDR2_DQ19 DDR3_DQ15	DDR3_DQSB0 DDR2_DQSZ[2] DDR3_DQSZ[1]	GND	DDR3_DQ4 DDR2_DQ20 DDR3_DQ14	GND	SR_PWRDN	SR_HSYNC	SR_D7	SR_D5	SR_D1
C	DDR3_MCLK DDR2_MCLK DDR3_MCLK	DDR3_MCLKZ DDR2_MCLKZ DDR3_MCLKZ	GND	DDR3_DQ11 DDR2_DQ28 NC	DDR3_DQ13 DDR2_DQ30 NC	DDR3_DQ2 DDR2_DQ22 DDR3_DQ12	GND	SR_STROBE	SR_PCLK	SR_D6	SR_D3	SR_D0
D		DDR3_RESETZ DDR2_A10 DDR3_RESETZ	GND	DDR3_DQ9 DDR2_DQM[3] NC	DDR3_DQ15 DDR2_DQ25 NC	DDR3_DQM1 DDR2_DQ27 NC	GND	GPIO27		GPIO29	GPIO31	
E	DDR3_ODT DDR2_A14 DDR3_ODT	DDR3_A3 DDR2_BA2 DDR3_A3	DDR3_A13 DDR2_A12 DDR3_A13	DDR3_A5 DDR2_CKE DDR3_A5	DDR3_DQSB1 DDR2_DQSZ[3] NC	DDR3_DQS1 DDR2_DQS[3] NC	GND	GPIO26	GPIO28	GPIO30	GPIO32	RFSPI_CZ0
F	DDR3_A7 DDR2_A3 DDR3_A7	DDR3_WEZ DDR2_CASZ DDR3_WEZ	DDR3_A15 DDR2_A7 DDR3_A15	GND	DDR3_DQ12 DDR2_DQ26 NC	DDR3_DQ10 DDR2_DQ31 NC	GND	GPIO25	GPIO24	GPIO33	AFE0_CLK	RFSPI_DATA
G		DDR3_BA0 DDR2_BA0 DDR3_BA0	GND	DDR3_DQ14 DDR2_DQ29 NC	DDR3_DQ8 DDR2_DQ24 NC	GND	GND	VDDIO_DATA_A1	GND	GND	GND	GND
H	DDR3_A0 DDR2_A5 DDR3_A0	DDR3_RASZ DDR2_A1 DDR3_RASZ	DDR3_A9 DDR2_A9 DDR3_A9	DDR3_A2 DDR2_BA1 DDR3_A2	DDR3_BA1 DDR2_RASZ DDR3_BA1	GND	GND	VDDIO_DATA_A1	GND	VDD_DDR	VDD	VDD
J	DDR3_BA2 DDR2_A6 DDR3_BA2	DDR3_A1 DDR2_WEZ DDR3_A1	DDR3_CASZ DDR2_A11 DDR3_CASZ	DDR3_A10 DDR2_A13 DDR3_A10	DDR3_A8 DDR2_A15 DDR3_A8	DDR3_A6 DDR2_ODT DDR3_A6	GND	VDDIO_CMD	GND	GND	GND	VDD
K		DDR3_A11 DDR2_A2 DDR3_A11	GND	DDR3_A4 DDR2_A8 DDR3_A4	DDR3_A14 DDR2_A4 DDR3_A14	GND	GND	VDDIO_DATA_A0	GND	GND	GND	GND
L	NC DDR2_DQ1 DDR3_DQ6	NC DDR2_DQ4 DDR3_DQ4	DDR3_A12 DDR2_A0 DDR3_A12	NC DDR2_DQ6 DDR3_DQ2	NC DDR2_DQ12 NC	DDR3_CKE DDR2_CKE DDR3_CKE	GND	VDDIO_DATA_A0	GND	GND	GND	GND
M	NC DDR2_DQM[0] DDR3_DQ0	GND	NC DDR2_DQS[0] DDR3_DQS[0]	NC DDR2_DQ14 NC	NC DDR2_DQ11 NC	GND	GND	GND	GND	GND	GND	GND
N		NC DDR2_DQSZ[0] DDR3_DQSZ[0]	GND	NC DDR2_DQ9 NC	NC DDR2_DQM[1] NC	GND	GND	GND	GND	GND	GND	GND
P	NC DDR2_DQ7 DDR3_DQ1	NC DDR2_DQ3 DDR3_DQ7	GND	NC DDR2_DQSZ[1] NC	NC DDR2_DQS[1] NC	NC DDR2_DQ10 NC	GND	VDD_DIAMOND	VDD_DIAMOND	GND	GND	GND
R	NC DDR2_DQ2 DDR3_DQ3	NC DDR2_DQ5 DDR3_DQ5	NC DDR2_DQ0 DDR3_DQM[0]	NC DDR2_DQ8 NC	NC DDR2_DQ13 NC	NC DDR2_DQ15 NC	GND	VDD_DIAMOND	VDD_DIAMOND	GND	GND	GND
T		GND	GND	GND	GND	GND	GND	VDD_DIAMOND	GND	VDD	AVDDL_DRV	GND
U	NAND_WEZ	NAND_WPZ	NAND_ALE	VSENSE_VSS	VSENSE_VDD	GND	GND	GND	GND	GND	VDD	VDDP_NAND
V	NAND_CLE	NAND_CE3Z	NAND_CE2Z	UART_RX1	UART_TX1	UART_RX4	UART_RTS2	GPIO34	GPIO8	GPIO7	GPIO6	GPIO0
W		NAND_CE1Z	NAND_CE0Z	UART_RX2	UART_TX2	UART_CTS2	GPIO35	GPIO37	GPIO9	GPIO5	GPIO3	GPIO1
Y	NAND_RBZ	NAND_REZ	NAND_DA0	UART_RX3	UART_TX3	UART_TX4	GPIO36	GPIO38		GPIO4	GPIO2	
AA	NAND_DA1	NAND_DA2	NAND_DA7	MPIF_D0	MPIF_D2	MPIF_BUSY	GPIO23	GPIO21	GPIO18	GPIO15	GPIO13	GPIO10
AB	NAND_DA3	NAND_DQS	NAND_DA5	MPIF_CS0Z	MPIF_D1	MPIF_D3	MIIC0_SCL	GPIO22	GPIO20	GPIO16	GPIO14	GPIO12
AC		NAND_DA4	NAND_DA6	MPIF_CS1Z		MPIF_CK	MIIC0_SDA		GPIO19	GPIO17		GPIO11
	1	2	3	4	5	6	7	8	9	10	11	12

Note: Red Characters Represent DDR3 16-bit Interface

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13	14	15	16	17	18	19	20	21	22	23	
	BT_SPI_SCLK	BTI_DATA0		SD0_CLK	SD0_D1		PM_SPI_DO	PM_IIC_SCL	PM_MIIC_SCL	XIN_RTC	**A**
BT_CHIP_EN	BT_SPI_SDATA	BTI_DATA1	SD0_D2	SD0_CMD	32K_OUT	PM_SPI_CZ0	PM_SPI_DI	PM_MIIC_SDA	XOUT_RTC	DP_P2	**B**
BT_SPI_SENB	BT_CLK_24M	BTI_RX_TX	SD0_D3	SD0_D0	PM_SPI_CK	PM_SPI_GPIO	PM_IIC_SDA	XCLK_OUT	GND	DM_P2	**C**
RFSPI_CLK	AFE0_SGN		SD1_D3	SD1_CLK	PM_SD1_CDZ	PM_SD_GPIO	CEC	GND	XIN	XOUT	**D**
AFE0_MAG	RFSPI_CZ1	SD1_D2	SD1_CMD	SD1_D0	PM_SD2_CDZ	IRIN	PM_GPIO0	CVBS0	VCOM		**E**
AFE1_MAG	AFE1_SGN	A_GPS_EVENT	SD1_D1	VDDP_GPS_AFE	PM_SD0_CDZ	PM_GPIO1	RESETN	VSYNC0	CVBS1	CVBS2	**F**
GND	VDDP_SR	GND	GND	GND	VDDP_GPS	ONOFF	CHRGDET	RIN0P	RIN0M	HSYNC0	**G**
GND	VDDP_BT	GND	GND	VDDP_SD1	GND	PMIC_CHIPEN		GIN0P	GIN0M		**H**
GND	GND	GND	GND	VDDP_SD0	IDAC_OUT_X	PMIC_INT	PMIC_STDBYN	BIN0P	SOGIN0	BIN0M	**J**
GND	GND	GND	GND		EARR	BATOK	HOTPLUG	MICINP	AUXMICINN	AUXMICINP	**K**
GND	GND	VDD_PM	VDDP_PM		EARL	VOMR_LINE1		LINEIN1_L	MICINN		**L**
GND	GND	AVDDL_USB_P0 AVDDL_USB_P1 AVDDL_USB_P2	AVDDL_HDMITX	AVDD_DAC	VOPR_LINE0	VOML_LINE1	VOPR_LINE1	LINEIN0_R	LINEIN1_R	LINEIN0_L	**M**
GND	GND	GND	AVDD_USB_P2 AVDD_XTAL_MPLL AVDD_ADC		VOML_LINE0	VOMR_LINE0	VOPL_LINE1	GND	MICBIAS	AUDREF	**N**
GND	GND	GND	GND	AVDD_DRV	VOPL_LINE0	Y2		TX2N	TX2P		**P**
GND	GND	GND	GND	GND	SAR2	Y1	X2	TX0P	TX1P	TX1N	**R**
GND	GND	GND	GND	GND	AVDD_AUDIO	SAR1	X1	TXCN	TXCP	TX0N	**T**
GND	VDDP_LCM VDDP_UART VDDP_MPIF	AVDD_LPLL	GND	GND	AVDD_USB_P0 AVDD_USB_P1 AVDD_HDMITX	SAR3	SAR4	HDMI_SDA	HDMI_SCL		**U**
GND	UART_RX5	TCON_GPIO6	VDDP_SD2	TCON_GPIO5	AVDD_AUX	SD2_CLK	SD2_D2	GND	CID	VBUS	**V**
UART_TX5	UART_RTS1	TCON_GPIO7	TCON_GPIO4	TCON_GPIO2	TCON_GPIO0	SD2_D1	SD2_D3	GND	DM_P0	DP_P0	**W**
UART_CTS1	TCON_GPIO8		TCON_GPIO3	TCON_GPIO1		SD2_D0	SD2_CMD	DM_P1	DP_P1		**Y**
IIS_TRX_WS	IIS_TRX_IN	TTL_GPIO9	TTL_GPIO6	TTL_GPIO4	TTL_GPIO1	OUTP_CH5	OUTP_CH4	OUTN_CH2	OUTP_CH0	GND	**AA**
IIS_TRX_BCK	IIS_TRX_OUT	TTL_GPIO11	TTL_GPIO7	TTL_GPIO5	TTL_GPIO3	OUTN_CH5	OUTN_CH4	OUTN_CH3	OUTN_CH1	OUTN_CH0	**AB**
SPDIF_OUT		TTL_GPIO10	TTL_GPIO8		TTL_GPIO2	TTL_GPIO0		OUTP_CH3	OUTP_CH2	OUTP_CH1	**AC**
13	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	

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PIN DESCRIPTIONS

Audio Interface

Pin Name	Pin Type	Function	Pin
MICBIAS	Output	Microphone BIAS	N22
AUDREF	Input	Audio Reference	N23
LINEIN1_L	Input	Audio Line-in1 Left Channel	L21
LINEIN1_R	Input	Audio Line-in1 Right Channel	M22
LINEIN0_L	Input	Audio Line-in0 Left Channel	M23
LINEIN0_R	Input	Audio Line-in0 Right Channel	M21
MICINP	Input	Microphone Input+	K21
MICINN	Input	Microphone Input-	L22
AUXMICINP	Input	Auxiliary Microphone in+	K23
AUXMICINN	Input	Auxiliary Microphone in-	K22
VOPL_LINE0	Output	Audio Line-out0+ Left Channel	P18
VOML_LINE0	Output	Audio Line-out0- Left Channel	N18
VOPR_LINE0	Output	Audio Line-out0+ Right Channel	M18
VOMR_LINE0	Output	Audio Line-out0- Right Channel	N19
VOPL_LINE1	Output	Audio Line-out1+ Left Channel	N20
VOML_LINE1	Output	Audio Line-out1- Left Channel	M19
VOPR_LINE1	Output	Audio Line-out1+ Right Channel	M20
VOMR_LINE1	Output	Audio Line-out1- Right Channel	L19
EARL	Output	Audio Earphone Output Left Channel	L18
EARR	Output	Audio Earphone output Right Channel	K18
SPDIF_OUT	Output	S/PDIF Audio Output; 8mA driving strength	AC13
IIS_TRX_BCK	I/O	Bit Clock, Output(Master Mode)/Input(Slave Mode); 4mA driving strength	AB13
IIS_TRX_WS	I/O	Word selection, Output(Master Mode)/Input(Slave Mode); 4mA driving strength	AA13
IIS_TRX_OUT	Output	Serial Data Output	AB14
IIS_TRX_IN	Input	Serial Data Input	AA14

NAND Flash Interface

Pin Name	Pin Type	Function	Pin
NAND_REZ	Output	NAND Flash Read Enable; active low	Y2
NAND_RBZ	Input	NAND Flash Ready/Busy; active low	Y1
NAND_WPZ	Output	NAND Flash Write Protect; active low	U2

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Pin Name	Pin Type	Function	Pin
NAND_WEZ	Output	NAND Flash Write Enable; active low	U1
NAND_ALE	Output	NAND Flash Address Latch Enable; active high	U3
NAND_CLE	Output	NAND Flash CLE	V1
NAND_DQS	Input	NAND Flash Data Strobe	AB2
NAND_CE0Z	Output	NAND Flash Chip Enable 0; active low	W3
NAND_CE1Z	Output	NAND Flash Chip Enable 1; active low	W2
NAND_CE2Z	Output	NAND Flash Chip Enable 2; active low	V3
NAND_CE3Z	Output	NAND Flash Chip Enable 3; active low	V2
NAND_DA[7:0]	I/O	NAND Flash Data [7:0]	AA3, AC3, AB3, AC2, AB1, AA2, AA1, Y3

UART Interface

Pin Name	Pin Type	Function	Pin
UART_CTS1	Output	UART 1 Clear to Set	Y13
UART_RTS1	Output	UART 1 Request to Set	W14
UART_CTS2	Output	UART 2 Clear to Set	W6
UART_RTS2	Output	UART 2 Request to Set	V7
UART_RX1	Input	UART 1 Receiver	V4
UART_TX1	Output	UART 1 Transmitter	V5
UART_RX2	Input	UART 2 Receiver	W4
UART_TX2	Output	UART 2 Transmitter	W5
UART_RX3	Input	UART 3 Receiver	Y4
UART_TX3	Output	UART 3 Transmitter	Y5
UART_RX4	Input	UART 4 Receiver	V6
UART_TX4	Output	UART 4 Transmitter	Y6
UART_RX5	Input	UART 5 Receiver	V14
UART_TX5	Output	UART 5 Transmitter	W13

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MPIF Interface

Pin Name	Pin Type	Function	Pin
MPIF_CS1Z	Output	MPIF Slave 1 Chip Select	AC4
MPIF_CS0Z	Output	MPIF Slave 0 Chip Select	AB4
MPIF_D[3:0]	I/O	MPIF Data Bus [3:0]	AB6, AA5, AB5, AA4
MPIF_CK	Output	MPIF Feedback Clock	AC6
MPIF_BUSY	Input	MPIF Flow Control	AA6

IIC Interface

Pin Name	Pin Type	Function	Pin
MIIC0_SDA	I/O	Master I2C Serial Data	AC7
MIIC0_SCL	Output	Master I2C Serial Clock	AB7

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIO[7:0]	I/O	General purpose input/output; 4mA driving strength	V10, V11, W10, Y10, W11, Y11, W12, V12
GPIO[15:8]	I/O	General purpose input/output; 4mA driving strength	AA10, AB11, AA11, AB12, AC12, AA12, W9, V9
GPIO[23:16]	I/O	General purpose input/output; 4mA driving strength	AA7, AB8, AA8, AB9, AC9, AA9, AC10, AB10
GPIO[31:24]	I/O	General purpose input/output; 4mA driving strength	D11, E10, D10, E9, D8, E8, F8, F9

PM Interface

Pin Name	Pin Type	Function	Pin
PM_SPI_DO	Input	SPI Serial Data from Device	A20
PM_SPI_DI	Output	SPI Serial Data to Device	B20
PM_SPI_CZ0	Output	SPI Chip 0 Select (active low)	B19
PM_SPI_CK	Output	SPI Serial Clock	C18

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Pin Name	Pin Type	Function	Pin
PM_SPI_GPIO	Input/Output	General Purpose Input/Output	C19
CEC	Input/Output	Consumer Electronics Control	D20
IRIN	Input	IrDa Serial Data	E19
32K_OUT	Output	32KHz Clock Output	B18
PM_SD_GPIO	Input/Output	General Purpose Input/Output	D19
PM_SD2_CDZ	Input	SD Card 2 Detect (active low)	E18
PM_SD1_CDZ	Input	SD Card 1 Detect (active low)	D18
PM_SD0_CDZ	Input	SD Card 0 Detect (active low)	F18
XIN_RTC	Input	32KHz Crystal Input	A23
XOUT_RTC	Output	32KHz Crystal Output	B22
HOTPLUG	Input	HDMI Connector Hotplug Detect (active high)	K20
PM_MIIC_SCL	Output	Master I2C Serial Clock	A22
PM_MIIC_SDA	Input/Output	Master I2C Serial Data	B21
PMIC_INT	Input	PMIC Interrupt (active high when battery voltage < 3.0v)	J19
PMIC_STDBYN	Output	PMIC Mode Selection (high @ active mode; low @ standby mode)	J20
PMIC_CHIPEN	Output	PMIC Chip Enable (active high)	H19
BATOK	Input	Battery Status (active high when battery voltage > 3.2v)	K19
CHRGDET	Input	Adaptor Detect (active high)	G20
ONOFF	Input	Chip ON/OFF (active low)	G19
RESETN	Input	Chip Reset (active low)	F20
PM_IIC_SCL	Input	Slave I2C Serial Clock	A21
PM_IIC_SDA	Input/Output	Slave I2C Serial Data	C20
PM_GPIO1	Input/Output	General Purpose Input/Output	F19
PM_GPIO0	Input/Output	General Purpose Input/Output	E20

HDMI TX Interface

Pin Name	Pin Type	Function	Pin
HDMI_SCL	Output	HDMI Tx IIC Serial Clock	U22
HDMI_SDA	I/O	HDMI Tx IIC Serial Data	U21
TXCP	Output	HDMI Tx Output Clock +	T22
TXCN	Output	HDMI Tx Output Clock -	T21
TX0P	Output	HDMI Tx Channel 0 Data +	R21

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Pin Name	Pin Type	Function	Pin
TX0N	Output	HDMI Tx Channel 0 Data -	T23
TX1P	Output	HDMI Tx Channel 1 Data +	R22
TX1N	Output	HDMI Tx Channel 1 Data -	R23
TX2P	Output	HDMI Tx Channel 2 Data +	P22
TX2N	Output	HDMI Tx Channel 2 Data -	P21

TCON TX Interface

Pin Name	Pin Type	Function	Pin
TCON_GPIO[8:0]	I/O	General purpose input/output; 4mA driving strength [8:0]	Y14, W15, V15, V17, W16, Y16, W17, Y17, W18
TTL_GPIO[11:0]	I/O	General purpose input/output; 8mA driving strength [11:0]	AB15, AC15, AA15, AC16, AB16, AA16, AB17, AA17, AB18, AC18, AA18, AC19

Video ADC TX Interface

Pin Name	Pin Type	Function	Pin
HSYNC0	Input	HSYNC / Composite Sync for VGA Input from Channel 0	G23
VSYNC0	Input	VSYNC for VGA Input from Channel 0	F21
BIN0P	Input	Analog Blue Input from Channel 0	J21
BIN0M	Input	Reference Ground for Analog Blue Input from Channel 0	J23
GIN0P	Input	Analog Green Input from Channel 0	H21
GIN0M	Input	Reference Ground for Analog Green Input from Channel 0	H22
RIN0P	Input	Analog Red Input from Channel 0	G21
RIN0M	Input	Reference Ground for Analog Red Input from Channel 0	G22
SOGIN0	Input	Sync for Component Input	J22
CVBS2	Input	CVBS (Composite) Video Input Channel 2	F23
CVBS1	Input	CVBS (Composite) Video Input Channel 1	F22
CVBS0	Input	CVBS (Composite) Video Input Channel 0	E21
VCOM	Input	CVBS Input Reference Ground	E22

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DRAM Interface (DDR2 16-bit x 2)

Pin Name	Pin Type	Function	Pin
DDR2_DQ[31:16]	I/O	DRAM Memory Data Bus [15:0]	F6, C5, G4, C4, D6, F5, D5, G5, A2, C6, B1, B6, B3, B2, A6, A1
DDR2_DQM[3:2]	Output	DRAM Memory Data Mask for Low Byte [3:2]	D4, A5
DDR2_DQS[3:2]	I/O	DRAM Memory Data Strobe [3:2]	E6, A4
DDR2_DQSZ[3:2]	I/O	DRAM Memory Data Strobe Inverse [3:2]	E5, B4
DDR2_DQ[15:0]	I/O	DRAM Memory Data Bus [15:0]	R6, M4, R5, L5, M5, P6, N4, R4, P1, L4, R2, L2, P2, R1, L1, R3
DDR2_DQM[1:0]	Output	DRAM Memory Data Mask for Low Byte	N5, M1
DDR2_DQS [1:0]	I/O	DRAM Memory Data Strobe	P5, M3
DDR2_DQSZ[1:0]	I/O	DRAM Memory Data Strobe Inverse	P4, N2
DDR2_MCLK	Output	DRAM Memory Positive Differential Clock	C1
DDR2_MCLKZ	Output	DRAM Memory Negative Differential Clock	C2
DDR2_A[15:0]	Output	DRAM Memory Address [15:0]	J5, E1, J4, E3, J3, D2, H3, K4, F3, J1, H1, K5, F1, K2, H2, L3
DDR2_ODT	I/O	Reserved for Future On-Die Termination	J6
DDR2_WEZ	Output	Write Enable; active low	J2
DDR2_BA[2:0]	Output	DRAM Memory Bank Address [2:0]	E2, H4, G2
DDR2_CASZ	Output	DRAM Memory Column Address Strobe; active low	F2
DDR2_CKE	Output	DRAM Clock Enable Output	E4
DDR2_RASZ	Output	DRAM Memory Row Address Strobe; active low	H5

DRAM Interface (DDR3 8-bit x 2)

Pin Name	Pin Type	Function	Pin
DDR3_DQ [15:8]	I/O	DRAM Memory Data Bus [15:8]	B3, B6, A2, C6, B1, A6, A1, A5
DDR3_DQM[1]	Output	DRAM Memory Data Mask for Low Byte[1]	B2
DDR3_DQS[1]	I/O	DRAM Memory Data Strobe[1]	A4
DDR3_DQSZ[1]	I/O	DRAM Memory Data Strobe Inverse[1]	B4

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Pin Name	Pin Type	Function	Pin
DDR3_DQ [7:0]	I/O	DRAM Memory Data Bus [7:0]	P2, L1, R2, L2, R1, L4, P1, M1
DDR3_DQM[0]	Output	DRAM Memory Data Mask for Low Byte[0]	R3
DDR3_DQS[0]	I/O	DRAM Memory Data Strobe[0]	M3
DDR3_DQSZ[0]	I/O	DRAM Memory Data Strobe Inverse[0]	N2
DDR3_MCLK	Output	DRAM Memory Positive Differential Clock	C1
DDR3_MCLKZ	Output	DRAM Memory Negative Differential Clock	C2
DDR3_RESETZ	Output	DRAM Memory Reset; active low	D2
DDR3_A[15:0]	Output	DRAM Memory Address [15:0]	F3, K5, E3, L3, K2, J4, H3, J5, F1, J6, E4, K4, E2, H4, J2, H1
DDR3_ODT	I/O	Reserved for Future On-Die Termination	E1
DDR3_WEZ	Output	Write Enable; active low	F2
DDR3_BA[2:0]	Output	DRAM Memory Bank Address [2:0]	J1, H5, G2
DDR3_CASZ	Output	DRAM Memory Column Address Strobe; active low	J3
DDR3_CKE	Output	DRAM Clock Enable Output	L6
DDR3_RASZ	Output	DRAM Memory Row Address Strobe; active low	H2
NC		No Connect	C4, C5, D4-D6, E5, E6, F5, F6, G4, G5, L5, M4, M5, N4, N5, P4-P6, R4-R6

DRAM Interface (DDR3 16-bits)

Pin Name	Pin Type	Function	Pin
DDR3_A[15:0]	Output	DRAM Memory Address [15:0]	F3, K5, E3, L3, K2, J4, H3, J5, F1, J6, E4, K4, E2, H4, J2, H1
DDR3_DQ[15:0]	I/O	DRAM Memory Data Bus [15:0]	D5, G4, C5, F5, C4, F6, D4, G5, B3, A6, B1, B6, A1, C6, A2, A5
DDR3_BA[2:0]	Output	DRAM Memory Bank Address [2:0]	J1, H5, G2
DDR3_CASZ	Output	DRAM Memory Column Address Strobe; active low	J3
DDR3_DQM[1:0]	Output	DRAM Memory Data Mask for Low Byte [1:0]; active high	D6, B2

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Pin Name	Pin Type	Function	Pin
DDR3_DQS[1:0]	I/O	DRAM Memory Data Strobe [1:0]	E6, A4
DDR3_DQSB[1:0]	I/O	DRAM Memory Data Strobe Inverse [1:0]	E5, B4
DDR3_CKE	Output	DRAM Clock Enable Output	L6
DDR3_ODT	I/O	Reserved for Future On-Die Termination	E1
DDR3_WEZ	Output	Write Enable; active low	F2
DDR3_RASZ	Output	DRAM Memory Row Address Strobe; active low	H2
DDR3_MCLK	Output	DRAM Memory Positive Differential Clock	C1
DDR3_MCLKZ	Output	DRAM Memory Negative Differential Clock	C2
DDR3_RESETZ	Output	DRAM Memory Reset; active low	D2
NC		No Connect	L1, L2, L4, L5, M1, M3, M4, M5, N2, N4, N5, P1, P2, P4, P5, P6, R1-R6

SD Interface

Pin Name	Pin Type	Function	Pin
SD2_D[3:0]	I/O	SD Card 2 Data Bus [3:0]	W20, V20, W19, Y19
SD2_CLK	Output	SD Card 2 Clock	V19
SD2_CMD	I/O	SD Card 2 Command/Response	Y20
SD0_D[3:0]	I/O	SD Card 0 Data Bus [3:0]	C16, B16, A18, C17
SD0_CLK	Output	SD Card 0 Clock	A17
SD0_CMD	I/O	SD Card 0 Command/Response	B17
SD1_D[3:0]	I/O	SD Card 1 Data Bus [3:0]	D16, E15, F16, E17
SD1_CLK	Output	SD Card 1 Clock	D17
SD1_CMD	I/O	SD Card 1 Command/Response	E16

AUX Interface

Pin Name	Pin Type	Function	Pin
X1	Input	Touch Panel X1	T20
Y1	Input	Touch Panel Y1	R19
X2	Input	Touch Panel X2	R20
Y2	Input	Touch Panel Y2	P19

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Pin Name	Pin Type	Function	Pin
SAR1	Input	SAR Low Speed ADC Input 1	T19
SAR2	Input	SAR Low Speed ADC Input 2	R18
SAR3	Input	SAR Low Speed ADC Input 3	U19
SAR4	Input	SAR Low Speed ADC Input 4	U20

CVBS Output Interface

Pin Name	Pin Type	Function	Pin
IDAC_OUT_X	Output	CVBS Output	J18

SR Interface

Pin Name	Pin Type	Function	Pin
SR_D[7:0]	Input	Sensor Input Pixel Data [7:0]	B10, C10, B11, A11, C11, A12, B12, C12
SR_PCLK	Input	Sensor Input Pixel Clock	C9
SR_HSYNC	Input	Sensor Input Horizontal Sync	B9
SR_STROBE	Output	Flash Strobe Signal	C8
SR_VSYNC	Input	Sensor Input Vertical Sync	A9
SR_RST	Output	Sensor Reset Control Signal	A8
SR_PWRDN	Output	Sensor Power Down Control Signal	B8

MOD Interface

Pin Name	Pin Type	Function	Pin
OUTN_CH5	Output	LVDS Channel 4 Negative Data Output	AB19
OUTP_CH5	Output	LVDS Channel 4 Positive Data Output	AA19
OUTN_CH4	Output	LVDS Channel 3 Negative Data Output	AB20
OUTP_CH4	Output	LVDS Channel 3 Positive Data Output	AA20
OUTN_CH3	Output	LVDS Channel Negative Clock Output	AB21
OUTP_CH3	Output	LVDS Channel Positive Clock Output	AC21
OUTN_CH2	Output	LVDS Channel 2 Negative Data Output	AA21
OUTP_CH2	Output	LVDS Channel 2 Positive Data Output	AC22
OUTN_CH1	Output	LVDS Channel 1 Negative Data Output	AB22
OUTP_CH1	Output	LVDS Channel 1 Positive Data Output	AC23
OUTN_CH0	Output	LVDS Channel 0 Negative Data Output	AB23
OUTP_CH0	Output	LVDS Channel 0 Positive Data Output	AA22

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BT Interface

Pin Name	Pin Type	Function	Pin
BTI_RX_TX	Output	RX/TX Indication for BT Interface	C15
BTI_DATA1	I/O	BT Interface Data Bit-1	B15
BTI_DATA0	I/O	BT Interface Data Bit-0	A15
BT_CLK_24M	Input	External 24Mhz Clock Input from BT RF Chip	C14
BT_SPI_SCLK	Output	BT SPI Clock for Access BT RF Chip	A14
BT_SPI_SDATA	I/O	BT SPI Data for Access BT RF Chip	B14
BT_SPI_SENB	Output	BT SPI Enable for Access BT RF Chip	C13
BT_CHIP_EN	Output	Enable Signal for BT RF Chip	B13

GPS Interface

Pin Name	Pin Type	Function	Pin
A_GPS_EVENT	Input	Assistance GPS Event	F15
AFE1_SGN	Input	GPS 1 Sign	F14
AFE1_MAG	Input	GPS 1 Magnitude	F13
AFE0_SGN	Input	GPS 0 Sign	D14
AFE0_MAG	Input	GPS 0 Magnitude	E13
RFSPI_CLK	Output	RF SPI Clock	D13
RFSPI_DATA	I/O	RF SPI Data	F12
RFSPI_CZ1	Output	RF SPI Chip Select to GPS1	E14
RFSPI_CZ0	Output	RF SPI Chip Select to GPS0	E12
AFE0_CLK	Input	GPS AFE Clock 16.369MHz Input	F11

TOP Interface

Pin Name	Pin Type	Function	Pin
XIN	Input	Crystal Input	D22
XOUT	I/O	Crystal Output; TCXO Input	D23
XCLK_OUT	Output	Clock Output Driver	C21

USB Interface

Pin Name	Pin Type	Function	Pin
DP_P0	I/O	USB Non Inverting Data Input/Output for Port 0	W23
DM_P0	I/O	USB Inverting Data Input/Output for Port 0	W22

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Pin Name	Pin Type	Function	Pin
DP_P1	I/O	USB Non Inverting Data Input/Output for Port 1	Y22
DM_P1	I/O	USB Inverting Data Input/Output for Port 1	Y21
DP_P2	I/O	USB Non Inverting Data Input/Output for Port 2	B23
DM_P2	I/O	USB Inverting Data Input/Output for Port 2	C23
VBUS	Input	USB VBUS Power	V23
CID	Input	USB OTP ID (high: slave mode, low: host mode)	V22

Misc. Interface

Pin Name	Pin Type	Function	Pin
VSENSE_VDD	Output	Core Power Feedback	U5
VSENSE_VSS	GND	Core GND	U4

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_AUX	3.2V Analog Power	Analog AUX power	V18
AVDD_LPLL	3.2V Analog Power	LPLL Power	U15
AVDD_DRV	3.2V Analog Power	Driver Power	P17
AVDDL_DRV	1.1V Analog Power	Driver Low Voltage Power	T11
AVDD_USB_P0	3.2V Analog Power	USB port 0 power	U18
AVDDL_USB_P0	1.1V Analog Power	USB port 0 low voltage power	M15
AVDD_USB_P1	3.2V Analog Power	USB port 1 power	U18
AVDDL_USB_P1	1.1V Analog Power	USB port 1 low voltage power	M15
AVDD_USB_P2	3.2V Analog Power	USB port 2 power	N16
AVDDL_USB_P2	1.1V Analog Power	USB port 2 low voltage power	M15
AVDD_ADC	3.2V Analog Power	Video ADC Power	N16
AVDD_XTAL_MPLL	3.2V Analog Power	XTAL MPLL power	N16
AVDD_DAC	3.2V Analog Power	Video DAC Power	M17
AVDD_AUDIO	3.2V Analog Power	Audio Power	T18
VDDP_NAND	3.2V PAD Power	NAND PAD Power	U12
VDDP_PM	3.2V PAD Power	PM PAD Power	L16
VDDP_SD2	3.2V PAD Power	SD2 PAD Power	V16
VDDP_SD0	3.2V PAD Power	SD0 PAD Power	J17
VDDP_SD1	3.2V PAD Power	SD1 PAD Power	H17
VDDP_SR	3.2V PAD Power	Sensor PAD Power	G14

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Pin Name	Pin Type	Function	Pin
VDDP_LCM	3.2V PAD Power	LCM PAD Power	U14
VDDP_UART	3.2V PAD Power	UART PAD Power	U14
VDDP_MPIF	3.2V PAD Power	MPIF PAD Power	U14
VDDP_BT	3.2V PAD Power	BT PAD Power	H14
VDDP_GPS	3.2V PAD Power	GPS PAD Power	G18
VDDP_GPS_AFE	3.2V PAD Power	GPS AFE PAD Power	F17
VDD_DIAMOND	1.1V Digital Power	Diamond Power	P8, P9, R8, R9, T8
VDD_PM	1.1V Digital Power	PM Power	L15
VDD	1.1V Digital Power	Core Power	H11, H12, J12, T10, U11
AVDD_HDMITX	3.2V Analog Power	HDMI TX power	U18
AVDDL_HDMITX	1.1V Analog Power	HDMI TX power	M16
VDDIO_DATA_A1	1.5V/1.8V DDR Power	DDR Power	G8, H8
VDDIO_DATA_A0	1.5V/1.8V DDR Power	DDR Power	K8, L8
VDD_DDR	1.1V Analog Power	DDR Power	H10
VDDIO_CMD	1.5V/1.8V DDR Power	DDR Power	J8
GND			A3, A7, B5, B7, C3, C7, C22, D3, D7, D21, E7, F4, F7, G3, G6, G7, G9-G13, G15-G17, H6, H7, H9, H13, H15, H16, H18, J7, J9-J11, J13-J16, K3, K6, K7, K9-K16, L7, L9-L14, M2, M6-M14, N3, N6-N15, N21, P3, P7, P10-P16, R7, R10-R17, T2-T7, T9, T12-T17, U6-U10, U13, U16, U17, V13, V21, W21, AA23

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ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD		LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum		0.5		V p-p
Maximum		TBD		V p-p
Input Bias Current			1	uA
SWITCHING PERFORMANCE				
Maximum Conversion Rate	170			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		170	MHz
PLL Jitter		400		ps p-p
Sampling Phase Tempco		15		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1[Note1]			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output	0.3		1.3	V
AUDIO				
ADC Input		2.8		V p-p
DAC Output		2.8		V p-p
SAR ADC Input	0		3.3	V
FB ADC Input [Note2]	0		1.2	V

Specifications subject to change without notice.
Note1: VDDP can be V_{VDD_32}, V_{VDD_18}, V_{VDD_15}
Note2: Input full scale is 1.2V, but input range is 0 ~ 3.3V

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.2V Supply Voltages	V_{VDD_32}		3.2		V
1.8V Supply Voltages	V_{VDD_18}		1.8		V
1.5V Supply Voltages	V_{VDD_15}		1.5		V
1.1V Supply Voltages	V_{VDD_11}		1.1		V
Ambient Operating Temperature	T_A	-40		85	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.2V Supply Voltages	V_{VDD_32}		3.52	V
1.8V Supply Voltages	V_{VDD_18}		1.98	V
1.5V Supply Voltages	V_{VDD_15}		1.65	V
1.1V Supply Voltages	V_{VDD_11}		1.21	V
Storage Temperature	T_{STG}	-40	150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

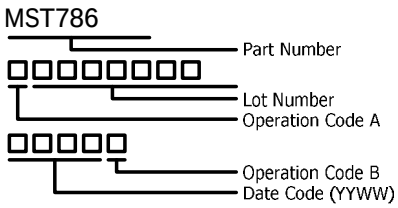
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ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MST786	-40°C to +85°C	LFBGA	493-ball
MST786-XX	-40°C to +85°C	LFBGA	493-ball

Note: XX suffix represents advanced features. Please contact MStar sales for details.

MARKING INFORMATION



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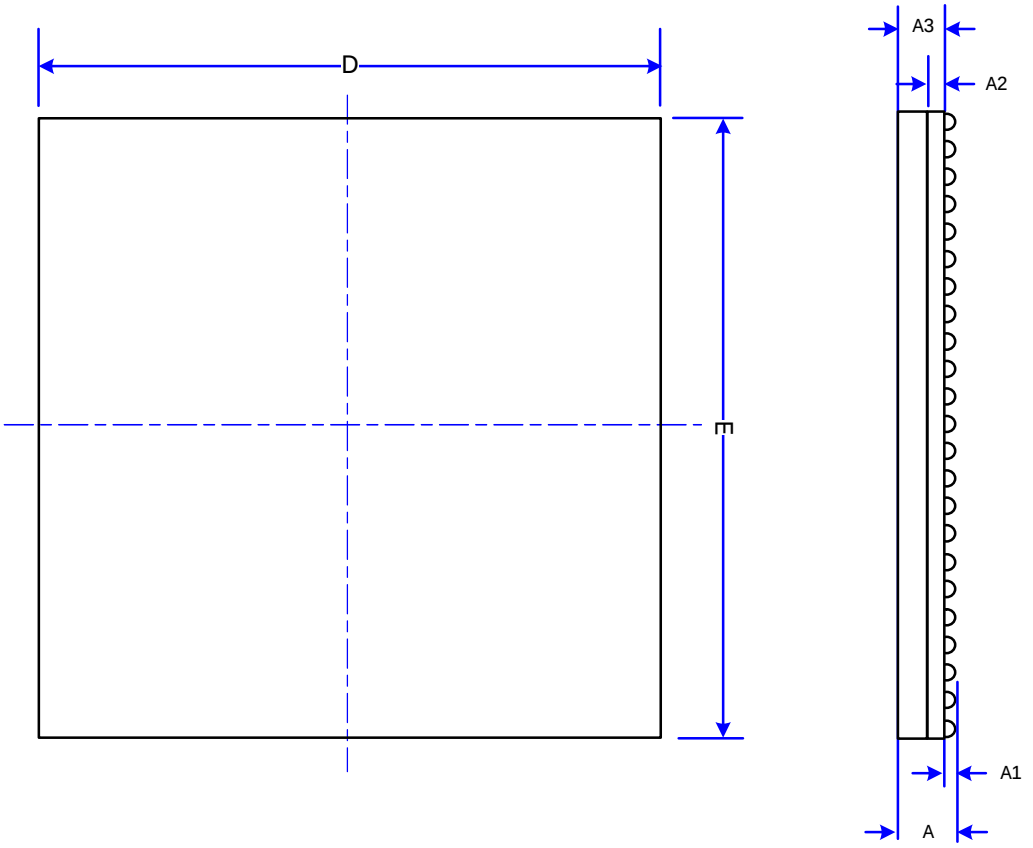
Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST786 comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

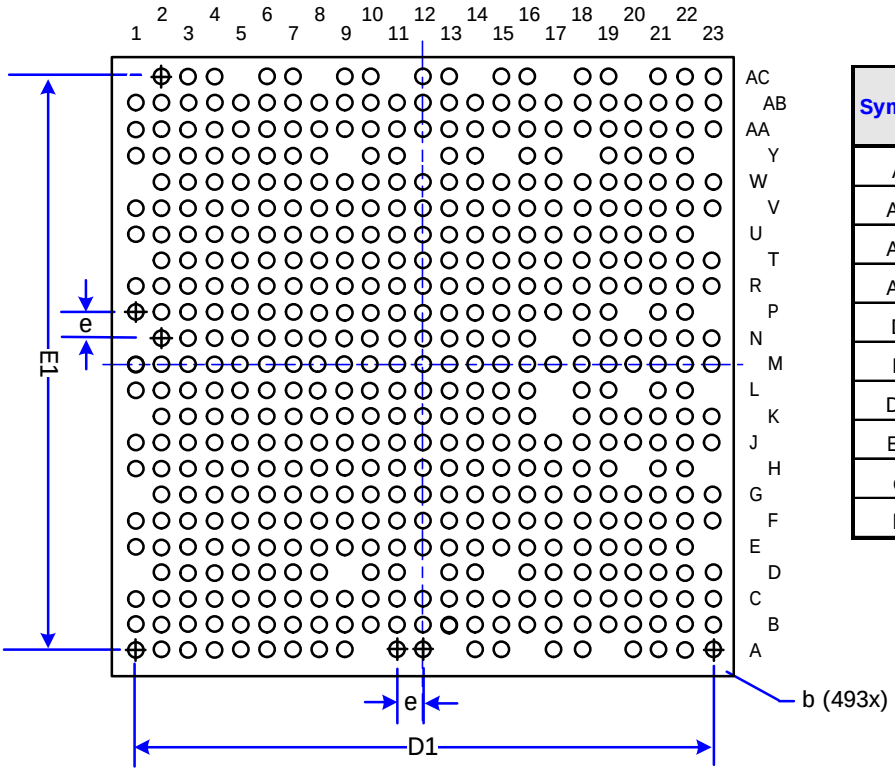
REVISION HISTORY

Document	Description	Date
MST786_ds_v01	Ÿ Initial release	Sep 2012

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MECHANICAL DIMENSIONS





Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.40	-	-	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.22	0.26	0.30	0.009	0.010	0.012
A3	0.91	0.96	1.01	0.036	0.038	0.040
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	-	17.60	-	-	0.693	-
E1	-	17.60	-	-	0.693	-
e	-	0.80	-	-	0.031	-
b	0.35	0.40	0.45	0.014	0.016	0.018

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REGISTER DESCRIPTIONS – HOUSEKEEPING PM REGISTER TABLE

MENULOAD Register (Bank = 02)

MENULOAD Register (Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0200h)	**REG0200**	**7:0**	**Default : 0x00**	**Access : R/W**
	MENULOAD_ADR[7:0]	7:0	Set initial start address for menuload 512bytes SRAM.	
00h (0201h)	**REG0201**	**7:0**	**Default : 0x00**	**Access : R/W**
	MENULOAD_ADR[15:8]	7:0	See description of '0200h'.	
01h (0202h)	**REG0202**	**7:0**	**Default : 0x00**	**Access : R/W**
	MENULOAD_WRITE_DATA[7:0]	7:0	Write/read data to menuload SRAM. Once write this port, menuload address will be auto increased by one.	

GDMA Register (Bank = 03)

GDMA Register (Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0300h)	**REG0300**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_C[7:0]	7:0	GDMA configuration register. BIT[7:6]: Source addressing mode. 00: Fixed. 01: Incremented by one. 10: Reserved. 11: Reserved. BIT[5:4]: Destination addressing mode. 00: Fixed. 01: Incremented by one. 10: Reserved. 11: Reserved. BIT[2]: Interrupt enable. 0: Disable. 1: Enable. BIT[1]: Reset. 0: Reset. 1: Not Reset. BIT[0]: Enable GDMA. 0: Disable. 1: Enable.	

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GDMA Register (Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0301h)	**REG0301**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_PIU_DS[2:0]	7:5	PIU destination module selection. 000: HK51_PM 1KB SRAM. Other: Reserved.	
	GDMA_PIU_SS[2:0]	4:2	PIU source module selection. 000: SPI. Other: Reserved.	
	GDMA_PATH_SEL[1:0]	1:0	GDMA transfer path selection. 00: Reserved. 01: Reserved. 10: Reserved. 11: PIU ----> PIU.	
01h (0302h)	**REG0302**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[7:0]	7:0	GDMA source address register.	
01h (0303h)	**REG0303**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[15:8]	7:0	See description of '0302h'.	
02h (0304h)	**REG0304**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[23:16]	7:0	See description of '0302h'.	
02h (0305h)	**REG0305**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[31:24]	7:0	See description of '0302h'.	
03h (0306h)	**REG0306**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[7:0]	7:0	GDMA destination address register.	
03h (0307h)	**REG0307**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[15:8]	7:0	See description of '0306h'.	
04h (0308h)	**REG0308**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[23:16]	7:0	See description of '0306h'.	
04h (0309h)	**REG0309**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[31:24]	7:0	See description of '0306h'.	
05h (030Ah)	**REG030A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_TC[7:0]	7:0	GDMA transfer count register.	
05h (030Bh)	**REG030B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_TC[15:8]	7:0	See description of '030Ah'.	
06h (030Ch)	**REG030C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_TC[23:16]	7:0	See description of '030Ah'.	

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GDMA Register (Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (030Eh)	**REG030E**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	GDMA_TRIGGER	0	GDMA transfer start.	
08h (0310h)	**REG0310**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	GDMA_TRANSFER_DONE_FLAG	0	Busy status. HW sets to one when transfer is completed. 1: Transfer Done or interrupt pending. 0: Transfer Busy or interrupt not pending.	
09h (0312h)	**REG0312**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	GDMA_CLEAR_TRANSFER_DONE	0	SW needs to set this bit to clear transfer_done flag or interrupt in order to receive the subsequent DMA transfer_done flag or interrupt.	

ISP Register (Bank = 08)

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (0802h)	**REG0802**	**7:0**	**Default : 0x00**	**Access : WO**
	SPI_COMMAND[7:0]	7:0	SPI command, If write data to this port, ISP will start operation.	
02h (0804h)	**REG0804**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDRESS1[7:0]	7:0	SPI address 1, A[7:0].	
02h (0805h)	**REG0805**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDERSS2[7:0]	7:0	SPI address 2, A[15:8].	
03h (0806h)	**REG0806**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDRESS3[7:0]	7:0	SPI address 3, A[23:16].	
04h (0808h)	**REG0808**	**7:0**	**Default : 0x00**	**Access : WO**
	WDATA[7:0]	7:0	SPI write data register.	
05h (080Ah)	**REG080A**	**7:0**	**Default : 0x00**	**Access : RO**
	RDATA[7:0]	7:0	SPI read data register.	
06h (080Ch)	**REG080C**	**7:0**	**Default : 0x04**	**Access : R/W**
	SPI_CLK_DIV16	7	SPI_CLOCK = MCU_CLOCK/16.	

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ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPI_CLK_DIV8	6	SPI_CLOCK = MCU_CLOCK/8.	
	SPI_CLK_DIV7	5	Reserved.	
	SPI_CLK_DIV6	4	Reserved.	
	SPI_CLK_DIV5	3	Reserved.	
	SPI_CLK_DIV4	2	SPI_CLOCK = MCU_CLOCK/4.	
	SPI_CLK_DIV3	1	Reserved.	
	SPI_CLK_DIV2	0	SPI_CLOCK = MCU_CLOCK/2.	
06h (080Dh)	**REG080D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPI_CLK_DIV128	2	SPI_CLOCK = MCU_CLOCK/128.	
	SPI_CLK_DIV64	1	SPI_CLOCK = MCU_CLOCK/64.	
	SPI_CLK_DIV32	0	SPI_CLOCK = MCU_CLOCK/32.	
07h (080Eh)	**REG080E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DEVICE_SELECT[2:0]	2:0	Select Device. 000: PMC.MXIC. 001: NextFlash. 010: ST. 011: SST. 100: ATMEL.	
08h (0810h)	**REG0810**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_CE_CLR	0	SPI chip enable clear. Software can force SPI chip disable at burst SPI read/write, this bit is write-then-clear register. 1: For clear. 0: For not clear.	
09h (0812h)	**REG0812**	**7:0**	**Default : 0x01**	**Access : R/W**
	TCES_TIME[7:0]	7:0	SPI Chip enable setup/hold time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delay 2 SPI clock.	
09h	**REG0813**	**7:0**	**Default : 0x00**	**Access : R/W**

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ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(0813h)	TCES_TIME[15:8]	7:0	See description of '0812h'.	
0Ah (0814h)	**REG0814**	**7:0**	**Default : 0xF3**	**Access : R/W**
	TBP_TIME[7:0]	7:0	Byte-Program time for device SST. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delay 500 SPI clock, Assume SPI clock 40ns, Delay 500*40 = 20 us.	
0Ah (0815h)	**REG0815**	**7:0**	**Default : 0x01**	**Access : R/W**
	TBP_TIME[15:8]	7:0	See description of '0814h'.	
0Bh (0816h)	**REG0816**	**7:0**	**Default : 0x04**	**Access : R/W**
	TCEH_TIME[7:0]	7:0	SPI Chip enable pulse high time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delay 5 SPI clock.	
0Bh (0817h)	**REG0817**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCEH_TIME[15:8]	7:0	See description of '0816h'.	
0Ch (0818h)	**REG0818**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_RD_REQ	0	SPI READ Data Request, For CPU read SPI data via RIU, If CPU read SPI data via XIU, request not needed.	
0Dh (081Ah)	**REG081A**	**7:0**	**Default : 0x14**	**Access : R/W**
	ISP_RP_ADR1[7:0]	7:0	Programmable ISP Read port address[15:0].	
0Dh (081Bh)	**REG081B**	**7:0**	**Default : 0xC2**	**Access : R/W**
	ISP_RP_ADR1[15:8]	7:0	See description of '081Ah'.	
0Eh (081Ch)	**REG081C**	**7:0**	**Default : 0x81**	**Access : R/W**
	ISP_RP_ADR2[7:0]	7:0	Programmable ISP Read port address[31:0].	
0Eh (081Dh)	**REG081D**	**7:0**	**Default : 0x1F**	**Access : R/W**
	ISP_RP_ADR2[15:8]	7:0	See description of '081Ch'.	
0Fh (081Eh)	**REG081E**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	

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ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ENDIAN_SEL_SPI	0	0: Big_endian. 1: Little_endian.	
10h (0820h)	**REG0820**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ISP_ACTIVE	0	ISP ACTIVE FLAG.	
11h (0822h)	**REG0822**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CPU_ACTIVE	1	CPU_ACTIVE FLAG.	
	-	0	Reserved.	
12h (0824h)	**REG0824**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	DMA_ACTIVE	2	DMA_ACTIVE FLAG.	
	-	1:0	Reserved.	
13h (0826h)	**REG0826**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	ISP_FSM[5:0]	5:0	ISP_FSM.	
14h (0828h)	**REG0828**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	SPI_MASTER_FSM[2:0]	2:0	SPI_MASTER_FSM.	
15h (082Ah)	**REG082A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_RD_DATA_RDY	0	SPI Read Data Ready flag. 1: Read data ready. 0: Read data not ready.	
16h (082Ch)	**REG082C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_DATA_RDY	0	SPI Write Ready flag. 1: Write data ready. 0: Write data not ready.	
17h (082Eh)	**REG082E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_CM_RDY	0	SPI Write Command Ready flag. 1: Write command ready. 0: Write command not ready.	

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ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
18h (0830h)	**REG0830**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CPU_RST_FM_ISP	0	ISP generate reset to CUP, When ISP programming done, software maybe can. Issue a reset to CPU.	
19h (0832h)	**REG0832**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ISP_OLD_EN	0	Read flag, for ISP_OLD_EN.	
20h (0840h)	**REG0840**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FORCE_ISP_IDLE	0	FORCE_ISP_IDLE.	
21h (0842h)	**REG0842**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAI_NUM[7:0]	7:0	For SST SPI FLASH USE. At AAI mode, set how many data will be written. 0x0000: For 1 byte programming. 0x0001: For 2 byte programming. 0xFFFF: For 64k byte programming.	
21h (0843h)	**REG0843**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAI_NUM[15:8]	7:0	See description of '0842h'.	
22h (0844h)	**REG0844**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAGE_PRO_REG	7	FORCE SPI COMMAND. Force PAGE PROGRAMMING.	
	FAST_READ_REG	6	FORCE SPI COMMAND. Force FAST READ.	
	READ_REG	5	FORCE SPI COMMAND. Force READ.	
	WRCR_REG	4	FORCE SPI COMMAND. Force WRCR.	
	RDCR_REG	3	FORCE SPI COMMAND. Force RDCR.	
	WRSR_REG	2	FORCE SPI COMMAND. Force WRSR.	
	RDSR_REG	1	FORCE SPI COMMAND. Force RDSR.	

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ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AAI_REG	0	FORCE SPI COMMAND. Force AAI mode.	
22h (0845h)	**REG0845**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAN_ID_REG	1	FORCE SPI COMMAND. Force READ MANUFACTURER ID.	
	B_ERASE_REG	0	FORCE SPI COMMAND. Force BLOCK ERASE.	
25h (084Ah)	**REG084A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MODE[7:0]	7:0	TEST_MODE, User define SPI waveform, 0x7777: User define. others: Not User define, Before entry TEST_MODE, Please make sure. ISP/DMA disable.	
25h (084Bh)	**REG084B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MODE[15:8]	7:0	See description of '084Ah'.	
26h (084Ch)	**REG084C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_CEB	0	User generate SPI chip enable waveform.	
27h (084Eh)	**REG084E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_SCK	0	User generate SPI clock waveform.	
28h (0850h)	**REG0850**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_SI	0	User generate SPI data waveform.	
29h (0852h)	**REG0852**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TEST_SPI_SO	0	SPI Data output. For RIU read. Please delay 1us for every setting(TEST MODE). EX1. W(0x21,0x0) --> delay 1us --> W(0x23,0x1) -->. Delay 1us --> W(0x22,0x1) --> delay 1us -->. W(0x22,0x0) --> delay 1us .....--> W(ox21,0x1). EX2. W(0x21,0x0) --> delay 1us --> W(0x22,0x1) -->. Delay 1us --> W(0x22,0x0) --> delay 1us -->. R(0x24) --> delay 1us .....> W(0x21,01).	
2Ah (0854h)	**REG0854**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRIGGER_MODE[7:0]	7:0	TRIGGER_MODE,, 0x3333: Trigger mode. others: Not Trigger mode. Before entry Trigger mode, Please make sure. ISP/DMA disable.	
2Ah (0855h)	**REG0855**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRIGGER_MODE[15:8]	7:0	See description of '0854h'.	
2Fh (085Eh)	**REG085E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SPI_ABORT_EN	1	Reserved.	
	SPI_PRE_FETCH_EN	0	Reserved.	
37h (086Eh)	**REG086E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CPHA	1	Configures the data sampling point. When 0, data is sampled when "SCLK" goes to active state(see reg_cpol). When 1, data is sampled when "SCLK" goes to idle state(see reg_cpol).	
	CPOL	0	Clock Polarity. Configures the idle state of "SCLK" serial clock when SPI is enabled (when disabled, "SCLK" is in high level). When 1, the "SCLK" output is set (SCLK = 1) otherwise it is cleared(SCLK = 0).	
3Ah (0874h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (087Eh)	**REG087E**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	SPI_BURST_RESET_Z	2	Software reset spi_burst. 0: Reset. 1: Not reset.	
	SPI_ARBITER_RESET_Z	1	Software reset spi arbiter. 0: Reset. 1 not reset.	
	ISP_TOP_RESET_Z	0	Software reset isp_top. 0: Reset. 1: Not reset.	

FSP Register (Bank = 08)

FSP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
C0h (0880h)	**REG0880**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD0[7:0]	7:0	Write data buffer0.	
C0h (0881h)	**REG0881**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD1[7:0]	7:0	Write data buffer1.	
C1h (0882h)	**REG0882**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD2[7:0]	7:0	Write data buffer2.	
C1h (0883h)	**REG0883**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD3[7:0]	7:0	Write data buffer3.	
C2h (0884h)	**REG0884**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD4[7:0]	7:0	Write data buffer4.	
C2h (0885h)	**REG0885**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD5[7:0]	7:0	Write data buffer5.	
C3h (0886h)	**REG0886**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD6[7:0]	7:0	Write data buffer6.	
C3h (0887h)	**REG0887**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD7[7:0]	7:0	Write data buffer7.	
C4h (0888h)	**REG0888**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD8[7:0]	7:0	Write data buffer8.	

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FSP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
C4h (0889h)	**REG0889**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD9[7:0]	7:0	Write data buffer9.	
C5h (088Ah)	**REG088A**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD0[7:0]	7:0	Read data buffer0.	
C5h (088Bh)	**REG088B**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD1[7:0]	7:0	Read data buffer1.	
C6h (088Ch)	**REG088C**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD2[7:0]	7:0	Read data buffer2.	
C6h (088Dh)	**REG088D**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD3[7:0]	7:0	Read data buffer3.	
C7h (088Eh)	**REG088E**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD4[7:0]	7:0	Read data buffer4.	
C7h (088Fh)	**REG088F**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD5[7:0]	7:0	Read data buffer5.	
C8h (0890h)	**REG0890**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD6[7:0]	7:0	Read data buffer6.	
C8h (0891h)	**REG0891**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD7[7:0]	7:0	Read data buffer7.	
C9h (0892h)	**REG0892**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD8[7:0]	7:0	Read data buffer8.	
C9h (0893h)	**REG0893**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD9[7:0]	7:0	Read data buffer9.	
CAh (0894h)	**REG0894**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WBF_SIZE1[3:0]	7:4	Set how many bytes will be transmitted in the second command. Max size is 9Byte. Min. Size is 1Byte.	
	FSP_WBF_SIZE0[3:0]	3:0	Set how many bytes will be transmitted in the first command. Max size is 10Byte. Min. Size is 1Byte.	
CAh	**REG0895**	**7:0**	**Default : 0x00**	**Access : R/W**

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FSP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(0895h)	-	7:4	Reserved.	
	FSP_WBF_SIZE2[3:0]	3:0	Set how many bytes will be transmitted in the third command. Max size is 8Byte. Min. Size is 1Byte.	
CBh (0896h)	**REG0896**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_RBF_SIZE1[3:0]	7:4	Set how many bytes will be received in the second command. Max size is 10Byte. Min. Size is 0Byte.	
	FSP_RBF_SIZE0[3:0]	3:0	Set how many bytes will be received in the first command. Max size is 10Byte. Min. Size is 0Byte.	
CBh (0897h)	**REG0897**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FSP_RBF_SIZE2[3:0]	3:0	Set how many bytes will be received in the third command. Max size is 10Byte. Min. Size is 0Byte.	
CCh (0898h)	**REG0898**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_CTRL0[7:0]	7:0	Control Register0. Bit[7:4]: Reserved. Bit[3]: Enable auto check error flag. Bit[2]: Enable fsp interrupt. 0: Disable. 1: Enable. Bit[1]: Reset. 0: Reset. 1: Not Reset. Bit[0]: Enable fsp. 0: Disable. 1: Enable.	
CCh	**REG0899**	**7:0**	**Default : 0x00**	**Access : R/W**

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FSP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(0899h)	FSP_CTRL1[7:0]	7:0	Control Register1. Bit[7]: Enable Second command. 0: Disable. 1: Enable. Bit[6]: Enable third command. 0: Disable. 1: Enable. Bit[5]: Enable auto check flash status. 0: Disable. 1: Enable. Bit[4:3]: Indicate which command is RDSR. 00: First command. 01: Second command. 10: Third command. 11: Reserved. Bit[2:0]: Indicate which bit is flash ready bit (For auto check flash status). Bit[2:0] = 0x0 ~ 0x7, HW will auto check reg_fsp_rd10[7:0].	
CDh (089Ah)	**REG089A**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	FSP_TRIGGER	0	Start flash self-programming.	
CEh (089Ch)	**REG089C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	FSP_AUTO_CHK_ERROR	1	Reserved.	
	FSP_DONE_FLAG	0	Busy status, HW sets to one when self-programming is completed. 1: Self-programming done or interrupt pending. 0: Self-programming busy or interrupt not pending.	
CFh (089Eh)	**REG089E**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	FSP_CLEAR_DONE_FLAG	0	SW needs to set this bit to clear done flag or interrupt.	

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QSPI Register (Bank = 08)

QSPI Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
E0h (08C0h)	**REG08C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_SPI[6:0]	6:0	CKG_SPI[5:0]: for spi clock selection. Bit[0]: for gating clock. Bit[1]: for clock invert. Bit[5]: 0, select XTAL. 1, It is decided by Bit[4:2]. Bit [4:2]. 000: XTAL. 001: 27M. 010: 36M. 011: 43M. 100: 54M. 101: 72M. Others: Reserved.	
E1h (08C2h)	**REG08C2**	**7:0**	**Default : 0x1A**	**Access : R/W**
	CSZ_SETUP[3:0]	7:4	CSZ setup time. (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
	CSZ_HIGH[3:0]	3:0	CSZ deselect time (SCZ = high). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
E1h (08C3h)	**REG08C3**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CSZ_HOLD[3:0]	3:0	CSZ hold time. (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
E2h (08C4h)	**REG08C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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QSPI Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MODE_SEL[3:0]	3:0	SPI model select. 0x0: Normal mode, (SPI command is 0x03). 0x1: Enable fast read mode, (SPI command is 0x0B). 0x2: Enable address single & data dual mode, (SPI command is 0x3B). 0x3: Enable address dual & data dual mode, (SPI command is 0xBB). 0xa: Enable address single & data quad mode, (SPI command is 0x6B) (Reserved). 0xb: Enable address quad & data quad mode, (SPI command is 0xEB). (Reserved.	
EAh (08D4h)	**REG08D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CHIP_SELECT[1:0]	1:0	00: Select external #1 SPI Flash. 01: Select external #2 SPI Flash. 10: Select external #3 SPI Flash. 11: Reserved.	
EFh (08DEh)	**REG08DE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ENDIA	0	For 32bit CPU read data.	

PM_SLEEP Register (Bank = 0E)

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0E00h)	**REG0E00**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	PG_AVDD_ANA	3	LDO power good.	
	PG_AVDD_IO	2	LDO power good.	
	PG_DVDD_CORE	1	LDO power good.	
	PG_DVDD_ARM	0	LDO power good.	
01h (0E02h)	**REG0E02**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PG_EN_AVDD_ANA	3	LDO power good enable.	

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PG_EN_AVDD_IO	2	LDO power good enable.	
	PG_EN_DVDD_CORE	1	LDO power good enable.	
	PG_EN_DVDD_ARM	0	LDO power good enable.	
03h (0E06h)	**REG0E06**	**7:0**	**Default : 0x00**	**Access : R/W**
	STANDBY_PASSWD[7:0]	7:0	Set the passwd to make the master FSM into the standby mode. 16'hBABE : active to sleep. 16'hEBAB : active to doze.	
03h (0E07h)	**REG0E07**	**7:0**	**Default : 0x00**	**Access : R/W**
	STANDBY_PASSWD[15:8]	7:0	See description of '0E06h'.	
06h (0E0Ch)	**REG0E0C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	NOBAT_INT	7	On battery detection interrupt (after debounce).	
	BATDET	6	Battery detection flag asserts as VBAT<3.0V.	
	-	5:4	Reserved.	
	EN_BATDET	3	Enable battery detection. 0: Disable 1: enable.	
	BATDET_DEBOUNCE[2:0]	2:0	Battery detecttion debounce time. 000: 0.1us 100: 5us. 001: 0.6us 101: 10us. 010: 1.2us 110: 20us. 011: 2.4us 111: 40us.	
0Bh (0E16h)	**REG0E16**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWRHLD_PASSWD[7:0]	7:0	Power hold passwd register : cpu need to set this passwd when the first power on. 8'h5A : active to off. 8'hA5 : power hold to active.	
0Bh (0E17h)	**REG0E17**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	PMU_DOZE_FLAG	2	Pmu doze flag.	
	PMU_SLEEP_FLAG	1	Pmu sleep flag.	
	PMU_ACTIVE_FLAG	0	Pmu active flag.	
0Ch (0E18h)	**REG0E18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	WKUP_TIMER_SEL[1:0]	1:0	Wakup delay time. 00: 50 ms. 01: 20 ms. 10: 6 ms. 11: 500 us.	
0Dh (0E1Ah)	**REG0E1A**	**7:0**	**Default : 0x00**	**Access : RO**
	WAKEUP_SRC_OUT_VAL[7:0]	7:0	Pmu wakeup source output value. [22]: TP_OUT. [21]: KEY0_OUT. [20:0]:GPIO_OUT.	
0Dh (0E1Bh)	**REG0E1B**	**7:0**	**Default : 0x00**	**Access : RO**
	WAKEUP_SRC_OUT_VAL[15:8]	7:0	See description of '0E1Ah'.	
0Eh (0E1Ch)	**REG0E1C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	WAKEUP_SRC_OUT_VAL[22:16]	6:0	See description of '0E1Ah'.	
0Fh (0E1Eh)	**REG0E1E**	**7:0**	**Default : 0x40**	**Access : R/W**
	SRAM_CTRL_SEL	7	SRAM timing control. 0: From default value. 1: From overwrite register.	
	DDR_CTRL_VAL	6	DDR I/O control under self-refresh mode, 0: Disable DDR I/O. 1: Enable DDR I/O.	
	DDR_CTRL_SEL	5	DDR I/O control under self-refresh mode, 0: PM atop control. 1: SW register control.	
	SLFRSH_CTRL	4	DDR I/O control. 0: Normal path. 1: Self-refresh path.	
	-	3:2	Reserved.	
	DBBUS_SEL[1:0]	1:0	Debug bus selection.	
10h (0E20h)	**REG0E20**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[7:0]	7:0	Key to off riu_cksum_prot (h51685168).	
10h (0E21h)	**REG0E21**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[15:8]	7:0	See description of '0E20h'.	
11h (0E22h)	**REG0E22**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[23:16]	7:0	See description of '0E20h'.	

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (0E23h)	**REG0E23**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[31:24]	7:0	See description of '0E20h'.	
14h (0E28h)	**REG0E28**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_GLHRM_EN[7:0]	7:0	The enable control of glitch remover for ext_int_in.	
14h (0E29h)	**REG0E29**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_GLHRM_EN[15:8]	7:0	See description of '0E28h'.	
15h (0E2Ah)	**REG0E2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GPIO_PM_GLHRM_EN[20:16]	4:0	See description of '0E28h'.	
16h (0E2Ch)	**REG0E2C**	**7:0**	**Default : 0x0F**	**Access : R/W**
	GPIO_PM_GLHRM_NUM[7:0]	7:0	The cycle number of glitch remover for ext_int_in.	
16h (0E2Dh)	**REG0E2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_GLHRM_NUM[15:8]	7:0	See description of '0E2Ch'.	
18h (0E30h)	**REG0E30**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE0[7:0]	7:0	Pmu spare register (for SW).	
18h (0E31h)	**REG0E31**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE0[15:8]	7:0	See description of '0E30h'.	
19h (0E32h)	**REG0E32**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE1[7:0]	7:0	Pmu spare register (for SW).	
19h (0E33h)	**REG0E33**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE1[15:8]	7:0	See description of '0E32h'.	
1Ah (0E34h)	**REG0E34**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE2[7:0]	7:0	Pmu spare register (for SW).	
1Ah (0E35h)	**REG0E35**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE2[15:8]	7:0	See description of '0E34h'.	
1Bh (0E36h)	**REG0E36**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE3[7:0]	7:0	Pmu spare register (for SW).	
1Bh (0E37h)	**REG0E37**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE3[15:8]	7:0	See description of '0E36h'.	
1Ch ~ 1Fh (0E38h ~ 0E3Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
44h	**REG0E88**	**7:0**	**Default : 0xC8**	**Access : R/W**

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(0E88h)	POR_EN	7		
	FRO_EN	6		
	FRO_CLK_ADJ[5:0]	5:0	Fro clock adjust. //default from efuse[5:0]. Can be over write by set reg_clkadj_ov_en=1 ,	
45h (0E8Ah)	**REG0E8A**	**7:0**	**Default : 0x17**	**Access : R/W**
	-	7	Reserved.	
	XTAL_OFF	6		
	CLOCK_OFF	5		
	STDBY_OFF	4		
	-	3	Reserved.	
	SYS_RSTN	2		
	FENC_OFF	1		
	PMIC_EN	0		
5Ch (0EB8h)	**REG0EB8**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_TESTBUS[7:0]	7:0	Pmu testbus : selection by reg_dbbus_sel.	
5Ch (0EB9h)	**REG0EB9**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_TESTBUS[15:8]	7:0	See description of '0EB8h'.	
5Dh (0EBAh)	**REG0EBA**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_TESTBUS[23:16]	7:0	See description of '0EB8h'.	
5Fh (0EBEh)	**REG0EBE**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVED_STATUS[7:0]	7:0	Read only reserved status [15:0] = 16'b0.	
5Fh (0EBFh)	**REG0EBF**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVED_STATUS[15:8]	7:0	See description of '0EBEh'.	
60h (0EC0h)	**REG0EC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PMIC_EN_PASSWD[7:0]	7:0	Password for control of PAD_PMIC_CHIPEN. All zero is enable (to pad). Not all zero ; the control will diable(PMIC_CHIPEN = 1).	
60h (0EC1h)	**REG0EC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	STDBY_EN_PASSWD[7:0]	7:0	Password for control of PAD_PMIC_STDBYN. All zero is enable (to pad). Not all zero ; the control will diable(PMIC_STDBYN = 1).	
61h	**REG0EC2**	**7:0**	**Default : 0x00**	**Access : R/W**

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(0EC2h)	FRO_EN_PASSWD[7:0]	7:0	Password for control of FRO_EN. All zero is enable. Not all zero ; the control will diable(FRO_EN = 1).	
61h (0EC3h)	**REG0EC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_EN_PASSWD[7:0]	7:0	Password for control of XTAL_EN. All zero is enable. Not all zero ; the control will diable(XTAL_EN = 1).	
62h (0EC4h)	**REG0EC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	ABBRESET_PASSWD[7:0]	7:0	Password for enable PAD_ABBRESET. All zero is enable (from pad). Not all zero ; PAD_ABBRESET will diable(ABBRESET = 0).	
62h (0EC5h)	**REG0EC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_EN_PASSWD[7:0]	7:0	Password for control of CLK_EN. All zero is enable. Not all zero ; the control will diable(CLK_EN = 1).	
64h (0EC8h)	**REG0EC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLKADJ_OV_EN	7	Clk adjust control override enable (0: disable; 1: enable).	
	-	6:5	Reserved.	
	BAT_NO_OK_TURNOFF	4	When vbat <2.8v bat is not ok. 0: Battery < 2.8v will not turn off phone. 1: Battery < 2.8v turn off phone.	
	BAT_OK_TIME_SEL	3	Select vbat ok debounce clock. 0: Use 2ms debounce. 1: Use 16ms debounce.	
	STDBY_TRIGGER	2	Trigger master standby function.	
	DOZE_EN	1	Enable master standby function; go to doze mode.	
	SLEEP_EN	0	Enable master standby function; go to sleep mode.	
64h (0EC9h)	**REG0EC9**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	PMU_DIG_RSTZ	6	Pmu soft ware reset for irq. Ldo soft start, pwm. 0: Reset. 1: Release.	
	MCU_STDBY_EN	5	Enable mcu standby function.	
	SYS_STDBY_EN	4	Enable system standby function.	
	-	3:0	Reserved.	

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
65h (0ECAh)	**REG0ECA**	**7:0**	**Default : 0x00**	**Access : RO**
	PMTEST	7	PAD PM_TEST flag to pmu_fsm.	
	PWRHLD	6	Power hold flag.	
	PMU_OFF	5	PMU_OFF flag.	
	PIN_STDBYN_M	4	Standby_n flag.	
	CHRG_PGIN	3	Chager plug in flag.	
	BAT_ON_DEBOUNCE	2	Battery on flag.	
	ONOFF_APPEAR	1	ONOFF_APPEAR from rtc_fsm to pmu_fsm.	
	PMU_FSM_EN	0	PMU_FSM_EN from rtc_fsm to pmu_fsm.	
65h (0ECBh)	**REG0ECB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	PIN_XTALEN_M	2	Xtal_en flag.	
	PIN_CLKEN_M	1	Clock_en flag.	
	PIN_CHIPEN_M	0	Chip_en flag.	
66h (0ECCh)	**REG0ECC**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[7:0]	7:0	Pmu_fsm state[47:0]. [16:0] : state. [23:17]:reserved. [40:24] : mstate. [47:41]:reserved.	
66h (0ECDh)	**REG0ECD**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[15:8]	7:0	See description of '0ECCh'.	
67h (0ECEh)	**REG0ECE**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[23:16]	7:0	See description of '0ECCh'.	
67h (0ECFh)	**REG0ECF**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[31:24]	7:0	See description of '0ECCh'.	
68h (0ED0h)	**REG0ED0**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[39:32]	7:0	See description of '0ECCh'.	
68h (0ED1h)	**REG0ED1**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[47:40]	7:0	See description of '0ECCh'.	
69h (0ED2h)	**REG0ED2**	**7:0**	**Default : 0x01**	**Access : R/W**
	KEYOFF_TIME_OUT[7:0]	7:0	Time out value for ON/OFF button shut-down.	
69h (0ED3h)	**REG0ED3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	KEYOFF_TIMER_CLEAR	4	Clear timer of ON/OFF button.	
	KEYOFF_TIMER_EN	3	Enable press ON/OFF button for force shut-down.	
	KEYOFF_TIME_OUT[10:8]	2:0	See description of '0ED2h'.	
6Ah (0ED4h)	**REG0ED4**	**7:0**	**Default : 0x60**	**Access : R/W**
	XHD_TC0	7	SRAM wrapper configuration.	
	XHD_TC1	6	SRAM wrapper configuration.	
	XRF_TC0	5	SRAM wrapper configuration.	
	XRF_TC1	4	SRAM wrapper configuration.	
	DELAY_AMT[3:0]	3:0	MIU dynamical gated delay.	
6Ah (0ED5h)	**REG0ED5**	**7:0**	**Default : 0x29**	**Access : R/W**
	SRAM_VSEL[1:0]	7:6	SRAM wrapper configuration.	
	SRAM2P_VW[1:0]	5:4	SRAM wrapper configuration.	
	SRAM2P_VR[1:0]	3:2	SRAM wrapper configuration.	
	AMG_TC0	1	SRAM wrapper configuration.	
	AMG_TC1	0	SRAM wrapper configuration.	
6Eh ~ 6Eh (0EDCh ~ 0EDDh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
70h (0EE0h)	**REG0EE0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[7:0]	7:0	Mask interrupt.	
70h (0EE1h)	**REG0EE1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[15:8]	7:0	See description of '0EE0h'.	
71h (0EE2h)	**REG0EE2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[23:16]	7:0	See description of '0EE0h'.	
71h (0EE3h)	**REG0EE3**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[31:24]	7:0	See description of '0EE0h'.	
72h (0EE4h)	**REG0EE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[7:0]	7:0	Force interrupt to be 1.	
72h (0EE5h)	**REG0EE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[15:8]	7:0	See description of '0EE4h'.	
73h (0EE6h)	**REG0EE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[23:16]	7:0	See description of '0EE4h'.	
73h	**REG0EE7**	**7:0**	**Default : 0x00**	**Access : R/W**

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(0EE7h)	IRQ_FORCE[31:24]	7:0	See description of '0EE4h'.	
74h (0EE8h)	**REG0EE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[7:0]	7:0	Clear interrupt.	
74h (0EE9h)	**REG0EE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[15:8]	7:0	See description of '0EE8h'.	
75h (0EEAh)	**REG0EEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[23:16]	7:0	See description of '0EE8h'.	
75h (0EEBh)	**REG0EEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[31:24]	7:0	See description of '0EE8h'.	
76h (0EECh)	**REG0EEC**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[7:0]	7:0	IRQ raw status. [31] reg cksum protection. [30] no battery. [29] charger unplug. [28] charger plug. [27] KEYOFF_PULSE. [26] ONOFF_PULSE. [25] cec wkup interrupt. [24] ir wkup interrupt. [23] rtc interrupt. [22] touch panel interrupt. [21] keypad interrupt. [20] ***useless***. [19:16] SD detection. [15:0] GPIO interrupt.	
76h (0EEDh)	**REG0EED**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[15:8]	7:0	See description of '0EECh'.	
77h (0EEEh)	**REG0EEE**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[23:16]	7:0	See description of '0EECh'.	
77h (0EEFh)	**REG0EEF**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[31:24]	7:0	See description of '0EECh'.	
78h (0EF0h)	**REG0EF0**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ final status.	
78h (0EF1h)	**REG0EF1**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[15:8]	7:0	See description of '0EF0h'.	

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PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
79h (0EF2h)	**REG0EF2**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[23:16]	7:0	See description of '0EF0h'.	
79h (0EF3h)	**REG0EF3**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[31:24]	7:0	See description of '0EF0h'.	
7Ah (0EF4h)	**REG0EF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_POLARITY[7:0]	7:0	Irq source polarity.	
7Ah (0EF5h)	**REG0EF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_POLARITY[15:8]	7:0	See description of '0EF4h'.	
7Bh (0EF6h)	**REG0EF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_POLARITY[23:16]	7:0	See description of '0EF4h'.	
7Bh (0EF7h)	**REG0EF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_POLARITY[31:24]	7:0	See description of '0EF4h'.	

PM_GPIO Register (Bank = 0F)

PM_GPIO Register (Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0F00h)	**REG0F00**	**7:0**	**Default : 0x65**	**Access : R/W**
	SPI_CZ1_MODE	7	PAD_PM_SPI_GPIO (0: gpio; 1: spi function).	
	SPI_CZ0_MODE	6	PAD_PM_SPI_CZ0 (0: gpio; 1: spi function).	
	SPI_MODE	5	PAD_PM_SPI_DI, PAD_PM_SPI_DO, PAD_PM_SPI_CK (0: gpio; 1: spi function).	
	MIIC_MODE	4	PAD_PM_MIIC_SDA, PAD_PM_MIIC_SCL (0: gpio; 1: master i2c function).	
	IR_MODE	3	PAD_IRIN (0: gpio; 1: ir function).	
	IIC_MODE	2	PAD_PM_IIC_SDA, PAD_PM_IIC_SCL (0: gpio, 1: slave i2c function).	
	CEC_MODE	1	PAD_CEC (0: gpio; 1: cec function).	
	ALL_PAD_IN	0	0: Disable PM all pad as input. 1: Enable PM all pad as input.	
00h (0F01h)	**REG0F01**	**7:0**	**Default : 0x0E**	**Access : R/W**
	-	7	Reserved.	
	SD2_MODE	6	PAD_PM_SD2_CDZ (0: gpio; 1: sd function).	

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PM_GPIO Register (Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD1_MODE	5	PAD_PM_SD1_CDZ (0: gpio; 1: sd function).	
	SD0_MODE	4	PAD_PM_SD0_CDZ (0: gpio; 1: sd function).	
	32KOUT_MODE	3	PAD_32K_OUT (0: gpio; 1: 32k out function).	
	CHRGDET_MODE	2	PAD_CHRGDET (0: gpio; 1: charger detect function).	
	ONOFF_MODE	1	PAD_ONOFF (0: gpio; 1: onoff function).	
	UART_MODE	0	PAD_PM_GPIO0, PAD_PM_GPIO1 (0: gpio; 1: uart function).	
01h (0F02h)	**REG0F02**	**7:0**	**Default : 0x48**	**Access : R/W**
	SD1_PS	7	Pull select of PAD_PM_SD1_CDZ (0: down; 1: up).	
	SD1_PE	6	Pull enable of PAD_PM_SD1_CDZ.	
	SD1_DRV	5	Driving strength of PAD_PM_SD1_CDZ.	
	SD0_PS	4	Pull select of PAD_PM_SD0_CDZ (0: down; 1: up).	
	SD0_PE	3	Pull enable of PAD_PM_SD0_CDZ.	
	SD0_DRV	2	Driving strength of PAD_PM_SD0_CDZ.	
	SPI_DRV1	1	Driving strength 1 of PAD_PM_SPI_CZ0 & PAD_PM_SPI_GPIO.	
	SPI_DRV0	0	Driving strength 0 of PAD_PM_SPI_CZ0 & PAD_PM_SPI_GPIO.	
01h (0F03h)	**REG0F03**	**7:0**	**Default : 0x12**	**Access : R/W**
	SETL	7	PM all pads set low.	
	SETH	6	PM all pads set high.	
	SD3_PS	5	Pull select of PAD_PM_SD_GPIO (0: down; 1: up).	
	SD3_PE	4	Pull enable of PAD_PM_SD_GPIO.	
	SD3_DRV	3	Driving strength of PAD_PM_SD_GPIO.	
	SD2_PS	2	Pull select of PAD_PM_SD2_CDZ (0: down; 1: up).	
	SD2_PE	1	Pull enable of PAD_PM_SD2_CDZ.	
	SD2_DRV	0	Driving strength of PAD_PM_SD2_CDZ.	
02h (0F04h)	**REG0F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_OUT_MODE[1:0]	7:6	Select TEST_BUS[23:0] output pins.	
	TEST_BUS8B_SEL[4:0]	5:1	Select TEST_BUS[23:0] source.	
	TESTBUS_EN	0	Enable test bus output.	
03h ~ 03h (0F06h ~ 0F07h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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PM_GPIO Register (Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (0F08h)	**REG0F08**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_PM_OEN[7:0]	7:0	GPIO's output enable.	
04h (0F09h)	**REG0F09**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_PM_OEN[15:8]	7:0	See description of '0F08h'.	
05h (0F0Ah)	**REG0F0A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_PM_OEN[23:16]	7:0	See description of '0F08h'.	
05h (0F0Bh)	**REG0F0B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	GPIO_PM_OEN[24]	0	See description of '0F08h'.	
06h (0F0Ch)	**REG0F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_OUT[7:0]	7:0	GPIO's output.	
06h (0F0Dh)	**REG0F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_OUT[15:8]	7:0	See description of '0F0Ch'.	
07h (0F0Eh)	**REG0F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_OUT[23:16]	7:0	See description of '0F0Ch'.	
07h (0F0Fh)	**REG0F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GPIO_PM_OUT[24]	0	See description of '0F0Ch'.	
08h (0F10h)	**REG0F10**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_PM_IN[7:0]	7:0	GPIO's input.	
08h (0F11h)	**REG0F11**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_PM_IN[15:8]	7:0	See description of '0F10h'.	
09h (0F12h)	**REG0F12**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_PM_IN[23:16]	7:0	See description of '0F10h'.	
09h (0F13h)	**REG0F13**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	GPIO_PM_IN[24]	0	See description of '0F10h'.	

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MCU Register (Bank = 10)

MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1000h)	**REG1000**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_START_ADDR_1[7:0]	7:0	SRAM_A Start Address[23:16].	
00h (1001h)	**REG1001**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_START_ADDR_1[15:8]	7:0	See description of '1000h'.	
01h (1002h)	**REG1002**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_END_ADDR_1[7:0]	7:0	SRAM_A End Address[23:16].	
01h (1003h)	**REG1003**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_END_ADDR_1[15:8]	7:0	See description of '1002h'.	
02h (1004h)	**REG1004**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_START_ADDR_0[7:0]	7:0	SRAM_A End Address[15:0],bit[7:0] don't care.	
02h (1005h)	**REG1005**	**7:0**	**Default : 0xF8**	**Access : R/W**
	SRAMA_START_ADDR_0[15:8]	7:0	See description of '1004h'.	
03h (1006h)	**REG1006**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SRAMA_END_ADDR_0[7:0]	7:0	SRAM_A End Address[15:0],bit[7:0] don't care.	
03h (1007h)	**REG1007**	**7:0**	**Default : 0xFB**	**Access : R/W**
	SRAMA_END_ADDR_0[15:8]	7:0	See description of '1006h'.	
04h (1008h)	**REG1008**	**7:0**	**Default : 0x01**	**Access : R/W**
	DRAM_START_ADDR_1[7:0]	7:0	DRAM Start Address[23:16].	
04h (1009h)	**REG1009**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_START_ADDR_1[15:8]	7:0	See description of '1008h'.	
05h (100Ah)	**REG100A**	**7:0**	**Default : 0x0F**	**Access : R/W**
	DRAM_END_ADDR_1[7:0]	7:0	DRAM End Address[23:16].	
05h (100Bh)	**REG100B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_END_ADDR_1[15:8]	7:0	See description of '100Ah'.	
06h (100Ch)	**REG100C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_START_ADDR_0[7:0]	7:0	DRAM Start Address[15:0],bit[7:0] don't care.	
06h (100Dh)	**REG100D**	**7:0**	**Default : 0x80**	**Access : R/W**
	DRAM_START_ADDR_0[15:8]	7:0	See description of '100Ch'.	
07h (100Eh)	**REG100E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DRAM_END_ADDR_0[7:0]	7:0	DRAM End Address[15:0],bit[7:0] don't care.	
07h (100Fh)	**REG100F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DRAM_END_ADDR_0[15:8]	7:0	See description of '100Eh'.	

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (1010h)	**REG1010**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[7:0]	7:0	SPI Start Address[23:16].	
08h (1011h)	**REG1011**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[15:8]	7:0	See description of '1010h'.	
09h (1012h)	**REG1012**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[7:0]	7:0	SPI End Address[23:16].	
09h (1013h)	**REG1013**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[15:8]	7:0	See description of '1012h'.	
0Ah (1014h)	**REG1014**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[7:0]	7:0	SPI Start Address[15:0],bit[7:0] don't care.	
0Ah (1015h)	**REG1015**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[15:8]	7:0	See description of '1014h'.	
0Bh (1016h)	**REG1016**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[7:0]	7:0	SPI End Address[15:0],bit[7:0] don't care.	
0Bh (1017h)	**REG1017**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[15:8]	7:0	See description of '1016h'.	
0Ch (1018h)	**REG1018**	**7:0**	**Default : 0x02**	**Access : R/W**
	MCU_BANK_USE_XFR	7	Use xfr to switch bank.	
	TEST_SEL[2:0]	6:4	Test bus selection.	
	ICACHE_RSTZ	3	Icache enable.	
	DRAM_EN	2	DRAM enable.	
	SPI_EN	1	SPI enable.	
	SRAMA_EN	0	SRAM_A enable.	
0Ch (1019h)	**REG1019**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU_BANK_XFR[7:0]	7:0	Xfr BANK(64KB).	
0Dh (101Ah)	**REG101A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TWA[7:0]	7:0	TWA for RIU Bridge.	
0Dh (101Bh)	**REG101B**	**7:0**	**Default : 0x01**	**Access : R/W**
	TAW[7:0]	7:0	TAW for RIU Bridge.	
20h (1040h)	**REG1040**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OV[7:0]	7:0	P0 overide by P0_REG. 0: Disable. 1: Enable.	

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (1041h)	**REG1041**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_REG[7:0]	7:0	Data to overide P0.	
21h (1042h)	**REG1042**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OV[7:0]	7:0	P1 overide by P1_REG. 0: Disable. 1: Enable.	
21h (1043h)	**REG1043**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_REG[7:0]	7:0	Data to overide P1.	
22h (1044h)	**REG1044**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OV[7:0]	7:0	P2 overide by P2_REG. 0: Disable. 1: Enable.	
22h (1045h)	**REG1045**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_REG[7:0]	7:0	Data to overide P2.	
23h (1046h)	**REG1046**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OV[7:0]	7:0	P3 overide by P3_REG. 0: Disable. 1: Enable.	
23h (1047h)	**REG1047**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_REG[7:0]	7:0	Data to overide P3.	
24h (1048h)	**REG1048**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_CTRL[7:0]	7:0	MCU Port 0 Output Enable Control.	
25h (104Ah)	**REG104A**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OE[7:0]	7:0	MCU Port 0 output enable.	
26h (104Ch)	**REG104C**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_IN[7:0]	7:0	MCU Port 0 output enable from output data.	
27h (104Eh)	**REG104E**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_CTRL[7:0]	7:0	MCU Port 1 Output Enable Control.	
28h (1050h)	**REG1050**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OE[7:0]	7:0	MCU Port 1 output enable.	
29h (1052h)	**REG1052**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_IN[7:0]	7:0	MCU Port 1 output enable from output data.	
2Ah (1054h)	**REG1054**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_CTRL[7:0]	7:0	MCU Port 2 Output Enable Control.	

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Bh (1056h)	**REG1056**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OE[7:0]	7:0	MCU Port 2 output enable.	
2Ch (1058h)	**REG1058**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_IN[7:0]	7:0	MCU Port 2 output enable from output data.	
2Dh (105Ah)	**REG105A**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_CTRL[7:0]	7:0	MCU Port 3 Output Enable Control.	
2Eh (105Ch)	**REG105C**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OE[7:0]	7:0	MCU Port 3 output enable.	
2Fh (105Eh)	**REG105E**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.	
40h (1080h)	**REG1080**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESET_CPU0[7:0]	7:0	Reset cpu0.	
40h (1081h)	**REG1081**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RESET_CPU0[15:8]	7:0	See description of '1080h'.	
41h (1082h)	**REG1082**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESET_CPU1[7:0]	7:0	Reset cpu1.	
41h (1083h)	**REG1083**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RESET_CPU1[15:8]	7:0	See description of '1082h'.	
42h (1084h)	**REG1084**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU0[7:0]	7:0	Sw reset cpu0(8051).	
42h (1085h)	**REG1085**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU0[15:8]	7:0	See description of '1084h'.	
43h (1086h)	**REG1086**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU1[7:0]	7:0	Sw reset cpu1(aeon).	
43h (1087h)	**REG1087**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU1[15:8]	7:0	See description of '1086h'.	
60h (10C0h)	**REG10C0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	BUFFER_MUX	7	Use 512 bytes as menuload buffer. 0: X51 xdata SRAM. 1: Menuload SRAM.	
	MENULOAD_DONE	6	Menuload done, will be cleared when menuload enabled.	
	MENULOAD_BUSY	5	Menuload busy, will be cleared when menuload done.	
	-	4:2	Reserved.	

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MENULOAD_CTRL_MODE[1:0]	1:0	Menuload trigger src select.	
60h (10C1h)	**REG10C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	ENABLE_MENULOAD_SRAM	7	Enable 512bytes menuload sram. 1: X51 xdata SRAM. 0: Xdata2miu.	
	-	6:0	Reserved.	
61h (10C2h)	**REG10C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MENULOAD_NUMBER[7:0]	7:0	Menuload numbers.	
62h (10C4h)	**REG10C4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	MENULOAD_ABORTED_ONCE	0	Menuload was aborted once.	
63h (10C6h)	**REG10C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SYNC_TRIG2_SEL	2	Select negated sync.	
	SYNC_TRIG1_SEL	1	Select negated sync.	
	SYNC_TRIG0_SEL	0	Select negated sync.	
64h (10C8h)	**REG10C8**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	MENULOAD_REALTIME_TRIG	0	Menuload realtime trigger one shot.	
65h (10CAh)	**REG10CA**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	MENULOAD_ABORT	0	Menuload abort one shot.	
66h (10CCh)	**REG10CC**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	MENULOAD_ENABLE	0	Menuload enable one shot.	
67h (10CEh)	**REG10CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MENULOAD_RIU_MODE	0	1: Download data to 512bytes SRAM thru riu, Aeon CPU can use it. 0: Download data to 512bytes SRAM thru xdata mapping.	
68h (10D0h)	**REG10D0**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	CLR_ADR	0	Clear "reg_menuload_addr" as "zero".	
70h	**REG10E0**	**7:0**	**Default : 0x14**	**Access : R/W**

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10E0h)	XB_ERAM_LB[7:0]	7:0	Eram map hk xdata low bondary(unit: 1k), suggested: 0x14.	
70h (10E1h)	**REG10E1**	**7:0**	**Default : 0x14**	**Access : R/W**
	XB_ERAM_HB[7:0]	7:0	Eram map hk xdata high bondary(unit: 1k), suggested: 0x14.	
72h (10E4h)	**REG10E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	XD2ERAM_ADRH[7:0]	7:0	Eram base address (unit: 1k, 0x000-0x3FF).	
73h (10E6h)	**REG10E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XD2ERAM_HK_MCU_PSRAM_EN	3	Enable eram mapping for hk mcu program SRAM.	
	XD2ERAM_PM_EN	2	Enable eram mapping for pm SRAM.	
	XD2ERAM_CACHE_EN	1	Enable eram mapping for 51 cache SRAM.	
	XD2ERAM_VD_MCU_EN	0	Enable eram mapping for vd mcu SRAM.	
7Ch (10F8h)	**REG10F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SPI_OFFSET_EN	0	Enable spi_offset_addr.	
7Ch (10F9h)	**REG10F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_OFFSET_ADDR[7:0]	7:0	SPI_OFFSET_ADDR[7:0].	
7Dh (10FAh)	**REG10FA**	**7:0**	**Default : 0x00**	**Access : RO**
	PROGRAM_BANK[7:0]	7:0		
7Dh (10FBh)	**REG10FB**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_BANK[7:0]	7:0		
7Eh (10FCh)	**REG10FC**	**7:0**	**Default : 0x00**	**Access : RO**
	PC_ADDR_L[7:0]	7:0	HK mcu program counter [15:0].	
7Eh (10FDh)	**REG10FD**	**7:0**	**Default : 0x00**	**Access : RO**
	PC_ADDR_L[15:8]	7:0	See description of '10FCh'.	
7Fh (10FEh)	**REG10FE**	**7:0**	**Default : 0x00**	**Access : RO**
	PC_ADDR_H[7:0]	7:0	HK mcu program counter [23:16].	
7Fh (10FFh)	**REG10FF**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA[7:0]	7:0	Return instruction to HK MCU.	

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PM_CEC Register (Bank = 11)

PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1100h)	**REG1100**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CEC_TX_LEN[3:0]	3:0	The number of bytes of data that the initiator wants to send. Write this register to trigger a new TX request. 0: Only header block is to be sent.	
00h (1101h)	**REG1101**	**7:0**	**Default : 0x03**	**Access : R/W**
	CEC_SAMPLE_SEL[2:0]	7:5	Sample times select for CEC line high/low detection. 000: 1X. 001: 2X. 010: 4X. ..... 110: 12X. 111: 14X.	
	TX_LOW_BIT_SEL[1:0]	4:3	The period select for follower generating a low bit period when the current received bit is too short to be a valid bit. 00: 1X nominal data bit period. 01: 1.4X nominal data bit period. 10: 1.5X nominal data bit period. 11: 1.6X nominal data bit period.	
	RETRY_CNT[2:0]	2:0	The retry times for re-transmitting a message (MAX).	
01h (1102h)	**REG1102**	**7:0**	**Default : 0x00**	**Access : R/W**
	CEC_CTRL_EN	7	Enable PD CEC controller. 0: Disable. 1: Enable.	
	-	6:5	Reserved.	
	CANCEL_TX_REQ	4	Cancel current TX request. 0: Normal. 1: Cancel.	
	TX_FALLING_SHIFT_SEL[1:0]	3:2	TX falling edge is shifted backward. 00: 0us. 01: 50us. 10: 100us. 11: 200us.	

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_RISING_SHIFT_SEL[1:0]	1:0	TX rising edge is shifted backward. 00: 0us. 01: 50us. 10: 100us. 11: 200us.	
01h (1103h)	**REG1103**	**7:0**	**Default : 0x53**	**Access : R/W**
	CEC_FREE_CNT2[3:0]	7:4	The necessary free bit period when new initiator wants to send a frame.	
	CEC_FREE_CNT1[3:0]	3:0	The necessary free bit period when pervious attempt to send frame is unsuccessful.	
02h (1104h)	**REG1104**	**7:0**	**Default : 0x07**	**Access : R/W**
	CEC_LOGICAL_ADDR[3:0]	7:4	Device logical address.	
	CEC_FREE_CNT3[3:0]	3:0	The necessary free bit period when present initiator wants to send another frame immediately after its previous frame.	
02h (1105h)	**REG1105**	**7:0**	**Default : 0x8F**	**Access : R/W**
	CNT_10US_VALUE[7:0]	7:0	Number of counts to achieve 10us (integer part). 0: 256 clock cycles. 1: 1 clock cycle. 2: 2 clock cycles. ..... 255: 255 clock cycles. (Unit: clock cycle).	
03h (1106h)	**REG1106**	**7:0**	**Default : 0x03**	**Access : R/W**
	RX_BOUND_SHIFT[3:0]	7:4	RX upper/lower bound is shifted forward/backward N*10us.	
	F_CNT_10US_VALUE[3:0]	3:0	Number of counts to achieve 10us (fractional part). This part is useless when CNT_10US_VALUE=1 (clock cycle). (Unit: 0.0625 clock cycle).	
03h (1107h)	**REG1107**	**7:0**	**Default : 0x08**	**Access : R/W**
	IGNORE_UNEXP_OP_LEN	7	Ignore un-expected length for OPCODE 0~3.	
	NSUP_CMD_ACT[1:0]	6:5	Action for non-supported command. 00: Ignore and ACK. 01: NACK. 1x: Feature abort.	
	CEC_CTRL_SEL	4	Select which PD CEC controller is active. 0: Software CEC controller (Standby). 1: Power down hardware CEC controller (Sleep).	

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LOST_ABT_SEL	3	Cancel TX request or retry if TX lost arbitration to a second initiator. 0: Retry. 1: Cancel.	
	CEC_OVERRIDE_FUN	2	Force CEC line low. 0: Disable. 1: Enable.	
	-	1	Reserved.	
	DIS_EH	0	Disable CEC error handling. 0: Normal. 1: Disable.	
04h (1108h)	**REG1108**	**7:0**	**Default : 0x00**	**Access : RO**
	HW_CEC_STS	7	Hardware CEC controller status. 0: Busy. 1: Idle.	
	CEC_TX_REQ_STS	6	Indicate the TX request status (read only). 0: End. 1: On going.	
	CEC_LINE	5	CEC line status.	
	CEC_RX_LEN[4:0]	4:0	The length of received message (read only). 0: Only header block is received.	
07h (110Eh)	**REG110E**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAKEUP_INT_MASK	7	Mask wakeup event interrupt.	
	OP3_OPERAND1_EN	6	Wakeup enable for the second operand specific to OPCODE 3.	
	OP2_OPERAND1_EN	5	Wakeup enable for the second operand specific to OPCODE 2.	
	OP_EN[4:0]	4:0	Wakeup enable for OPCODE 0~4.	
07h (110Fh)	**REG110F**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXP_OP4_LEN[3:0]	7:4	Expected RX length for OPCODE 4. Header and OPCODE are not included.	
	OPERAND_EN[3:0]	3:0	Wakeup enable for operand specific to OPCODE 0~3.	
08h (1110h)	**REG1110**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE0[7:0]	7:0	Receive OPCODE 0 to wakeup.	
08h (1111h)	**REG1111**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE1[7:0]	7:0	Receive OPCODE 1 to wakeup.	

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
09h (1112h)	**REG1112**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE2[7:0]	7:0	Receive OPCODE 2 to wakeup.	
09h (1113h)	**REG1113**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE3[7:0]	7:0	Receive OPCODE 3 to wakeup.	
0Ah (1114h)	**REG1114**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE4[7:0]	7:0	Receive OPCODE 4 to wakeup.	
0Ah (1115h)	**REG1115**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP0_OPERAND[7:0]	7:0	Receive the operand specific to OPCODE 0 to wakeup.	
0Bh (1116h)	**REG1116**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1_OPERAND[7:0]	7:0	Receive the operand specific to OPCODE 1 to wakeup.	
0Bh (1117h)	**REG1117**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP2_OPERAND0[7:0]	7:0	Receive the operand specific to OPCODE 2 to wakeup.	
0Ch (1118h)	**REG1118**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP2_OPERAND1[7:0]	7:0	Receive the operand specific to OPCODE 2 to wakeup.	
0Ch (1119h)	**REG1119**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP3_OPERAND0[7:0]	7:0	Receive the operand specific to OPCODE 3 to wakeup.	
0Dh (111Ah)	**REG111A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP3_OPERAND1[7:0]	7:0	Receive the operand specific to OPCODE 3 to wakeup.	
0Dh (111Bh)	**REG111B**	**7:0**	**Default : 0x04**	**Access : R/W**
	OP_ACC_TYPE[4:0]	7:3	Access type for OPCODE 0~4. 0: Direct. 1: Broadcast.	
	CEC_VERSION[2:0]	2:0	CEC version. 000: Version 1.1. 001: Version 1.2. 010: Version 1.2a. 011: Version 1.3. 1xx: Version 1.3a.	
0Eh (111Ch)	**REG111C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHYSICAL_ADDR[7:0]	7:0	Device physical address.	
0Eh (111Dh)	**REG111D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHYSICAL_ADDR[15:8]	7:0	See description of '111Ch'.	
0Fh (111Eh)	**REG111E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VENDOR_ID[7:0]	7:0	Device vendor ID.	

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (111Fh)	**REG111F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VENDOR_ID[15:8]	7:0	See description of '111Eh'.	
10h (1120h)	**REG1120**	**7:0**	**Default : 0x00**	**Access : R/W**
	VENDOR_ID[23:16]	7:0	See description of '111Eh'.	
10h (1121h)	**REG1121**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ABORT_REASON[2:0]	2:0	Feature abort reason. 000: "Unrecognized OPCODE". 001: "Not in correct mode to respond". 010: "Cannot provide source". 011: "Invalid operand". 100: "Refused".	
11h (1122h)	**REG1122**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	WAKEUP_INT	6	Wakeup interrupt event.	
	RX_BIT_TOO_LONG	5	RX bit too long.	
	RX_BIT_TOO_SHORT	4	RX bit too short.	
	HW_RX_EVENT_STS3	3	Receive Give_Device_Vendor ID message in power down mode.	
	HW_RX_EVENT_STS2	2	Receive Get_CEC_Version message in power down mode.	
	HW_RX_EVENT_STS1	1	Receive Give_Physical_Address message in power down mode.	
	HW_RX_EVENT_STS0	0	Receive Give_Device_Power_Status message in power down mode.	
11h (1123h)	**REG1123**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	CEC_EVENT_INT[6:0]	6:0	CEC event status. [0]: Receive a new message successfully. [1]: Send message successfully. [2]: Retry fail. [3]: Lost arbitration to the second initiator. [4]: Transmit NACK. [5]: The second CEC receives a new message successfully. [6]: The second CEC transmits NACK.	
12h (1124h)	**REG1124**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CEC_EVENT_INT_FORCE[6:0]	6:0	Force CEC event interrupt.	
12h (1125h)	**REG1125**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CEC_EVENT_INT_CLEAR[6:0]	6:0	Clear CEC event interrupt.	
13h (1126h)	**REG1126**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CEC_EVENT_INT_MASK[6:0]	6:0	Mask CEC event interrupt.	
14h (1128h)	**REG1128**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CEC_SRC_CK_SEL	1	CEC source clock select. 0: External OSC. 1: Internal OSC.	
	PD_NORMAL_SEL	0	Power down or normal CEC controller select. 0: Normal. 1: Power down.	
14h (1129h)	**REG1129**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEV_TYPE[7:0]	7:0	Device Type for <Report Physical Address> message.	
18h (1130h)	**REG1130**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA0[7:0]	7:0	Data block 0 for TX.	
18h (1131h)	**REG1131**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA1[7:0]	7:0	Data block 1 for TX.	
19h (1132h)	**REG1132**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA2[7:0]	7:0	Data block 2 for TX.	
19h (1133h)	**REG1133**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA3[7:0]	7:0	Data block 3 for TX.	
1Ah (1134h)	**REG1134**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA4[7:0]	7:0	Data block 4 for TX.	
1Ah (1135h)	**REG1135**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA5[7:0]	7:0	Data block 5 for TX.	
1Bh (1136h)	**REG1136**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA6[7:0]	7:0	Data block 6 for TX.	
1Bh (1137h)	**REG1137**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA7[7:0]	7:0	Data block 7 for TX.	
1Ch	**REG1138**	**7:0**	**Default : 0x00**	**Access : R/W**

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1138h)	TX_DATA8[7:0]	7:0	Data block 8 for TX.	
1Ch (1139h)	**REG1139**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA9[7:0]	7:0	Data block 9 for TX.	
1Dh (113Ah)	**REG113A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA10[7:0]	7:0	Data block 10 for TX.	
1Dh (113Bh)	**REG113B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA11[7:0]	7:0	Data block 11 for TX.	
1Eh (113Ch)	**REG113C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA12[7:0]	7:0	Data block 12 for TX.	
1Eh (113Dh)	**REG113D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA13[7:0]	7:0	Data block 13 for TX.	
1Fh (113Eh)	**REG113E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA14[7:0]	7:0	Data block 14 for TX.	
1Fh (113Fh)	**REG113F**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA15[7:0]	7:0	Data block 15 for TX.	
20h (1140h)	**REG1140**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA0[7:0]	7:0	Data block 0 for RX.	
20h (1141h)	**REG1141**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA1[7:0]	7:0	Data block 1 for RX.	
21h (1142h)	**REG1142**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA2[7:0]	7:0	Data block 2 for RX.	
21h (1143h)	**REG1143**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA3[7:0]	7:0	Data block 3 for RX.	
22h (1144h)	**REG1144**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA4[7:0]	7:0	Data block 4 for RX.	
22h (1145h)	**REG1145**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA5[7:0]	7:0	Data block 5 for RX.	
23h (1146h)	**REG1146**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA6[7:0]	7:0	Data block 6 for RX.	
23h (1147h)	**REG1147**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA7[7:0]	7:0	Data block 7 for RX.	
24h (1148h)	**REG1148**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA8[7:0]	7:0	Data block 8 for RX.	

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (1149h)	**REG1149**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA9[7:0]	7:0	Data block 9 for RX.	
25h (114Ah)	**REG114A**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA10[7:0]	7:0	Data block 10 for RX.	
25h (114Bh)	**REG114B**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA11[7:0]	7:0	Data block 11 for RX.	
26h (114Ch)	**REG114C**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA12[7:0]	7:0	Data block 12 for RX.	
26h (114Dh)	**REG114D**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA13[7:0]	7:0	Data block 13 for RX.	
27h (114Eh)	**REG114E**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA14[7:0]	7:0	Data block 14 for RX.	
27h (114Fh)	**REG114F**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA15[7:0]	7:0	Data block 15 for RX.	
28h (1150h)	**REG1150**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA0[7:0]	7:0	Data block 0 for RX.	
28h (1151h)	**REG1151**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA1[7:0]	7:0	Data block 1 for the second RX.	
29h (1152h)	**REG1152**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA2[7:0]	7:0	Data block 2 for the second RX.	
29h (1153h)	**REG1153**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA3[7:0]	7:0	Data block 3 for the second RX.	
2Ah (1154h)	**REG1154**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA4[7:0]	7:0	Data block 4 for the second RX.	
2Ah (1155h)	**REG1155**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA5[7:0]	7:0	Data block 5 for the second RX.	
2Bh (1156h)	**REG1156**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA6[7:0]	7:0	Data block 6 for the second RX.	
2Bh (1157h)	**REG1157**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA7[7:0]	7:0	Data block 7 for the second RX.	
2Ch (1158h)	**REG1158**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA8[7:0]	7:0	Data block 8 for the second RX.	
2Ch	**REG1159**	**7:0**	**Default : 0x00**	**Access : RO**

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1159h)	RX1_DATA9[7:0]	7:0	Data block 9 for the second RX.	
2Dh (115Ah)	**REG115A**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA10[7:0]	7:0	Data block 10 for the second RX.	
2Dh (115Bh)	**REG115B**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA11[7:0]	7:0	Data block 11 for the second RX.	
2Eh (115Ch)	**REG115C**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA12[7:0]	7:0	Data block 12 for the second RX.	
2Eh (115Dh)	**REG115D**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA13[7:0]	7:0	Data block 13 for the second RX.	
2Fh (115Eh)	**REG115E**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA14[7:0]	7:0	Data block 14 for the second RX.	
2Fh (115Fh)	**REG115F**	**7:0**	**Default : 0x00**	**Access : RO**
	RX1_DATA15[7:0]	7:0	Data block 15 for the second RX.	
30h (1160h)	**REG1160**	**7:0**	**Default : 0x30**	**Access : R/W, WO**
	-	7:6	Reserved.	
	CEC_INT_NORMAL_MASK	5	CEC interrupt mask for normal funciton. 0: Normal. 1: Mask.	
	CEC_INT_PD_MASK	4	CEC interrupt mask for PM function. 0: Normal. 1: Mask.	
	INT_CLR_TYPE_SEL	3	Interrupt clear type select. 0: Edge. 1: Level.	
	TX_REQ	2	Trigger TX request select. 0: Write TE_LEN register to trigger a new TX request. 1: Write TX_REQ bit to trigger a new TX request.	
	TX_REQ_SEL	1	Trigger TX request select. 0: Write TE_LEN register to trigger a new TX request. 1: Write TX_REQ bit to trigger a new TX request.	
	EN_CEC_MULTI_FUN	0	Enable CEC multiple function.	
30h (1161h)	**REG1161**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	CEC1_LOGICAL_ADDR[3:0]	3:0	The second CEC logical address.	
31h	**REG1162**	**7:0**	**Default : 0x00**	**Access : RO**

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PM_CEC Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1162h)	-	7:5	Reserved.	
	CEC1_RX_LEN[4:0]	4:0	The length of received message for the second CEC. (read only). 0: Only header block is received.	
31h (1163h)	**REG1163**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEV_TYPE_1[7:0]	7:0	Device type for the second CEC controller.	
32h (1164h)	**REG1164**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHYSICAL_ADDR_1[7:0]	7:0	Physical address for the second CEC controller.	
32h (1165h)	**REG1165**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHYSICAL_ADDR_1[15:8]	7:0	See description of '1164h'.	

PM_RTC Register (Bank = 12)

PM_RTC Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1200h)	**REG1200**	**7:0**	**Default : 0x30**	**Access : RO, R/W**
	PG_RTC	7	Power good of rtc ldo.	
	VDD_RTC_STATUS	6	VDD_RTC power good status. Auto set to 1 when reg_load_en. Can be sw reset by reg_pg_rst.	
	EN_MSKCMP_SUBCNT	5	Enable mask compare subcnt. 0: Mask compare subcnt (default). 1: Unmask compare subcnt.	
	CNT_EN	4	Enable RTC count.	
	PG_RST	3	Reset power good register.	
	-	2	Reserved.	
	LOAD_EN	1	Enable load for loading value into RTC counter.	
	VDD_RTC_GOOD	0	VDD_RTC power good status.	
00h (1201h)	**REG1201**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PG_PMU	0	Power grant of pmu mtcmos.	
01h (1202h)	**REG1202**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOAD_VAL[7:0]	7:0	RTC counter load value.	
01h	**REG1203**	**7:0**	**Default : 0x00**	**Access : R/W**

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PM_RTC Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1203h)	LOAD_VAL[15:8]	7:0	See description of '1202h'.	
02h (1204h)	**REG1204**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOAD_VAL[23:16]	7:0	See description of '1202h'.	
02h (1205h)	**REG1205**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOAD_VAL[31:24]	7:0	See description of '1202h'.	
03h (1206h)	**REG1206**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[7:0]	7:0	Second counter; by snapshot.	
03h (1207h)	**REG1207**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[15:8]	7:0	See description of '1206h'.	
04h (1208h)	**REG1208**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[23:16]	7:0	See description of '1206h'.	
04h (1209h)	**REG1209**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[31:24]	7:0	See description of '1206h'.	
05h (120Ah)	**REG120A**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_CNT[7:0]	7:0	Sub counter by snapshot (for dividing XTAL to 1 Hz).	
05h (120Bh)	**REG120B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	SUB_CNT[14:8]	6:0	See description of '120Ah'.	
06h (120Ch)	**REG120C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MSKCMP_SUBCNT[7:0]	7:0	MSKCMP_SUBCNT[15:0], 1 to mask sub_cnt comapre.	
06h (120Dh)	**REG120D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MSKCMP_SUBCNT[15:8]	7:0	See description of '120Ch'.	
07h (120Eh)	**REG120E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREQ_CW[7:0]	7:0	Frequency to add second counter (default is 1s).	
07h (120Fh)	**REG120F**	**7:0**	**Default : 0x80**	**Access : R/W**
	FREQ_CW[15:8]	7:0	See description of '120Eh'.	
08h (1210h)	**REG1210**	**7:0**	**Default : 0x00**	**Access : R/W**
	MATCH_VALUE[7:0]	7:0	Match value for alarm interrupt.	
08h (1211h)	**REG1211**	**7:0**	**Default : 0x00**	**Access : R/W**
	MATCH_VALUE[15:8]	7:0	See description of '1210h'.	
09h (1212h)	**REG1212**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MATCH_VALUE[23:16]	7:0	See description of '1210h'.	
09h	**REG1213**	**7:0**	**Default : 0xFF**	**Access : R/W**

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PM_RTC Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1213h)	MATCH_VALUE[31:24]	7:0	See description of '1210h'.	
0Ah (1214h)	**REG1214**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	PMTEST	6	Pm test mode ; read only flag.	
	32K_FLAG	5	Rtc 32k flag ; read only flag.	
	RTC_32K_OK	4	Rtc 32k ok flag; read only flag.	
	ABBRESETB	3	Hardware reset debounce; read only flag.	
	ONOFF	2	System on/off; read only flag.	
	RESETB	1	Hardware reset; read only flag.	
	CHRGDET	0	Charger detection; read only flag.	
0Ah (1215h)	**REG1215**	**7:0**	**Default : 0x00**	**Access : R/W**
	TESTBUS_SEL[3:0]	7:4	Select output testbus.	
	-	3:1	Reserved.	
	ONOFF_SEL	0	System on/off active decision. 0: Active low. 1: Active high.	
0Bh (1216h)	**REG1216**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[7:0]	7:0	Raw second counter.	
0Bh (1217h)	**REG1217**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[15:8]	7:0	See description of '1216h'.	
0Ch (1218h)	**REG1218**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[23:16]	7:0	See description of '1216h'.	
0Ch (1219h)	**REG1219**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[31:24]	7:0	See description of '1216h'.	
0Dh (121Ah)	**REG121A**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SUB_CNT[7:0]	7:0	Raw sub counter (for dividing XTAL to 1 Hz).	
0Dh (121Bh)	**REG121B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	RAW_SUB_CNT[14:8]	6:0	See description of '121Ah'.	
0Eh (121Ch)	**REG121C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RTC_SNAPSHOT	0	Snapshot for real time clock. 0: No active. 1: Snapshot reg_sec_cnt and reg_sub_cnt.	

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PM_RTC Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (121Eh)	**REG121E**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_FSM_STATE[7:0]	7:0	Rtc fsm state.	
0Fh (121Fh)	**REG121F**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_FSM_STATE[15:8]	7:0	See description of '121Eh'.	
10h (1220h)	**REG1220**	**7:0**	**Default : 0x00**	**Access : R/W**
	INITIAL_FLAG[7:0]	7:0	RTC initial current time.	
10h (1221h)	**REG1221**	**7:0**	**Default : 0x00**	**Access : R/W**
	INITIAL_FLAG[15:8]	7:0	See description of '1220h'.	
11h (1222h)	**REG1222**	**7:0**	**Default : 0x00**	**Access : R/W**
	INITIAL_FLAG[23:16]	7:0	See description of '1220h'.	
11h (1223h)	**REG1223**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INITIAL_FLAG[30:24]	6:0	See description of '1220h'.	
12h (1224h)	**REG1224**	**7:0**	**Default : 0x00**	**Access : R/W**
	OFFSET_FLAG[7:0]	7:0	RTC offset time.	
12h (1225h)	**REG1225**	**7:0**	**Default : 0x00**	**Access : R/W**
	OFFSET_FLAG[15:8]	7:0	See description of '1224h'.	
13h (1226h)	**REG1226**	**7:0**	**Default : 0x00**	**Access : R/W**
	OFFSET_FLAG[23:16]	7:0	See description of '1224h'.	
13h (1227h)	**REG1227**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OFFSET_FLAG[30:24]	6:0	See description of '1224h'.	
14h (1228h)	**REG1228**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ALARM_FLAG[7:0]	7:0	RTC alarm flag register.	
14h (1229h)	**REG1229**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ALARM_FLAG[15:8]	7:0	See description of '1228h'.	
15h (122Ah)	**REG122A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ALARM_FLAG[23:16]	7:0	See description of '1228h'.	
15h (122Bh)	**REG122B**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	ALARM_FLAG[30:24]	6:0	See description of '1228h'.	
16h (122Ch)	**REG122C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT1_FLAG[7:0]	7:0	RTC interrupt event1 register.	

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PM_RTC Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (122Dh)	**REG122D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT1_FLAG[15:8]	7:0	See description of '122Ch'.	
17h (122Eh)	**REG122E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT1_FLAG[23:16]	7:0	See description of '122Ch'.	
17h (122Fh)	**REG122F**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	EVENT1_FLAG[30:24]	6:0	See description of '122Ch'.	
18h (1230h)	**REG1230**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT2_FLAG[7:0]	7:0	RTC interrupt event2 register.	
18h (1231h)	**REG1231**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT2_FLAG[15:8]	7:0	See description of '1230h'.	
19h (1232h)	**REG1232**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT2_FLAG[23:16]	7:0	See description of '1230h'.	
19h (1233h)	**REG1233**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	EVENT2_FLAG[30:24]	6:0	See description of '1230h'.	
1Ah (1234h)	**REG1234**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT3_FLAG[7:0]	7:0	RTC interrupt event3 register.	
1Ah (1235h)	**REG1235**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT3_FLAG[15:8]	7:0	See description of '1234h'.	
1Bh (1236h)	**REG1236**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT3_FLAG[23:16]	7:0	See description of '1234h'.	
1Bh (1237h)	**REG1237**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	EVENT3_FLAG[30:24]	6:0	See description of '1234h'.	
1Ch (1238h)	**REG1238**	**7:0**	**Default : 0x00**	**Access : RO**
	CURRENT_FLAG[7:0]	7:0	RTCcurrent flag.	
1Ch (1239h)	**REG1239**	**7:0**	**Default : 0x00**	**Access : RO**
	CURRENT_FLAG[15:8]	7:0	See description of '1238h'.	
1Dh (123Ah)	**REG123A**	**7:0**	**Default : 0x00**	**Access : RO**
	CURRENT_FLAG[23:16]	7:0	See description of '1238h'.	
1Dh (123Bh)	**REG123B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	

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PM_RTC Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CURRENT_FLAG[30:24]	6:0	See description of '1238h'.	
1Eh (123Ch)	**REG123C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	EVENT3_FLAG_UPDATE	5	Update RTC interrupt event3 register.	
	EVENT2_FLAG_UPDATE	4	Update RTC interrupt event2 register.	
	EVENT1_FLAG_UPDATE	3	Update RTC interrupt event1 register.	
	ALARM_FLAG_UPDATE	2	Update RTC alarm register.	
	OFFSET_FLAG_UPDATE	1	Update RTC offset time.	
	INITIAL_FLAG_UPDATE	0	Update RTC initial current time.	
1Fh (123Eh)	**REG123E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EVENT3_INT_EN	3	RTC interrupt event3 interrupt enable.	
	EVENT2_INT_EN	2	RTC interrupt event2 interrupt enable.	
	EVENT1_INT_EN	1	RTC interrupt event1 interrupt enable.	
	ALARM_INT_EN	0	RTC alarm interrupt enable.	
20h (1240h)	**REG1240**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[7:0]	7:0	RTC LIFE register.	
20h (1241h)	**REG1241**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[15:8]	7:0	See description of '1240h'.	
21h (1242h)	**REG1242**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[23:16]	7:0	See description of '1240h'.	
21h (1243h)	**REG1243**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[31:24]	7:0	See description of '1240h'.	
22h (1244h)	**REG1244**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[39:32]	7:0	See description of '1240h'.	
22h (1245h)	**REG1245**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[47:40]	7:0	See description of '1240h'.	
23h (1246h)	**REG1246**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[55:48]	7:0	See description of '1240h'.	
23h (1247h)	**REG1247**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LIFE[57:56]	1:0	See description of '1240h'.	
27h	**REG124E**	**7:0**	**Default : 0x00**	**Access : R/W**

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PM_RTC Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(124Eh)	WD_EXPIRE[7:0]	7:0	Watch dog expired value (128hz). Need set this register at first, then set reg_watchdat_en.	
27h (124Fh)	**REG124F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	WATCHDOG_EN	4	Enable watch dog for !PAD_PWRHLD & !PMU_OFF 1second.	
	WD_EXPIRE[11:8]	3:0	See description of '124Eh'.	
2Bh (1256h)	**REG1256**	**7:0**	**Default : 0x7F**	**Access : R/W**
	RTC_IRQ_MASK[7:0]	7:0	Mask alarm interrupt.	
2Ch (1258h)	**REG1258**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_IRQ_FORCE[7:0]	7:0	Force alarm interrupt to be 1.	
2Dh (125Ah)	**REG125A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_IRQ_CLR[7:0]	7:0	Clear alarm interrupt.	
2Eh (125Ch)	**REG125C**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_IRQ_RAW_STATUS[7:0]	7:0	RTC IRQ raw status : [7]: Reserved. [6]: Reg_event3_int, [5]: Reg_event2_int, [4]: Reg_event1_int, [3]: Reg_alarm_int, [2]: Rtc_match_int, [1]: Sub_cnt_match_int, [0]: ~reg_rtc_32k_ok.	
2Eh (125Dh)	**REG125D**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_IRQ_FINAL_STATUS[7:0]	7:0	RTC IRQ final status.	
2Fh (125Eh)	**REG125E**	**7:0**	**Default : 0x67**	**Access : R/W**
	RTC_INT_PASSWD[7:0]	7:0	RTC pass word.	
2Fh (125Fh)	**REG125F**	**7:0**	**Default : 0x04**	**Access : R/W**
	RTC_INT_PASSWD[15:8]	7:0	See description of '125Eh'.	

PM_TOP Register (Bank = 1E)

PM_TOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**REG1E00**	**7:0**	**Default : 0x00**	**Access : RO**

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PM_TOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1E00h)	CHIP_ID[7:0]	7:0	Chip ID.	
00h (1E01h)	**REG1E01**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_ID[15:8]	7:0	See description of '1E00h'.	
01h (1E02h)	**REG1E02**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_VERSION[7:0]	7:0	Chip Version.	
01h (1E03h)	**REG1E03**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_REVISION[7:0]	7:0	Chip Revision.	
10h (1E20h)	**REG1E20**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_ADC[7:0]	7:0	Version ID of adcdvipll in dig_top.	
10h (1E21h)	**REG1E21**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_APVR[7:0]	7:0	Version ID of disp_ipath and M4VE in dig_top (no use).	
11h (1E22h)	**REG1E22**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_ATSC_DEMOD[7:0]	7:0	Version ID of ATSC demod in dig_top.	
11h (1E23h)	**REG1E23**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_AUDIO[7:0]	7:0	Version ID of Audio in dig_top.	
12h (1E24h)	**REG1E24**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_DISP_MISC[7:0]	7:0	Version ID of disp_misc in dig_top.	
12h (1E25h)	**REG1E25**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_DSCRMB[7:0]	7:0	Version ID of DSCRMB_TOP in dig_top.	
13h (1E26h)	**REG1E26**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_DVBC_DEMOD[7:0]	7:0	Version ID of DVBC demod in dig_top.	
13h (1E27h)	**REG1E27**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_DVBT_DEMOD[7:0]	7:0	Version ID of DVBT demod in dig_top.	
14h (1E28h)	**REG1E28**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_DVI_HDMI_HDCP[7:0]	7:0	Version ID of dvi_hdmi_hdcp_top in dig_top.	
14h (1E29h)	**REG1E29**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_EMAC[7:0]	7:0	Version ID of EMAC in dig_top.	
15h (1E2Ah)	**REG1E2A**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_FCIE[7:0]	7:0	Version ID of FCIE in dig_top.	
15h (1E2Bh)	**REG1E2B**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_GE[7:0]	7:0	Version ID of GE in dig_top.	
16h (1E2Ch)	**REG1E2C**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_GOP[7:0]	7:0	Version ID of GOP in dig_top.	

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PM_TOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (1E2Dh)	**REG1E2D**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_HDMITX[7:0]	7:0	Version ID of HDMI Tx in dig_top.	
17h (1E2Eh)	**REG1E2E**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_HEMCU[7:0]	7:0	Version ID of MIPS in dig_top.	
17h (1E2Fh)	**REG1E2F**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_HKMCU[7:0]	7:0	Version ID of HK MCU in dig_top_pm.	
18h (1E30h)	**REG1E30**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_HVD[7:0]	7:0	Version ID of HVD in dig_top.	
18h (1E31h)	**REG1E31**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_IDAC[7:0]	7:0	Version ID of DAC_Top in dig_top.	
19h (1E32h)	**REG1E32**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_INTERNAL_LA[7:0]	7:0	Version ID of LA_sc and LA_DMD in dig_top.	
19h (1E33h)	**REG1E33**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_JPD[7:0]	7:0	Version ID of JPD in dig_top.	
1Ah (1E34h)	**REG1E34**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MCU32[7:0]	7:0	Version ID of MCU32 in dig_top.	
1Ah (1E35h)	**REG1E35**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MIU[7:0]	7:0	Version ID of MIU in dig_top.	
1Bh (1E36h)	**REG1E36**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MOBF[7:0]	7:0	Version ID of mobf in dig_top.	
1Bh (1E37h)	**REG1E37**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MPIF[7:0]	7:0	Version ID of MPIF in dig_top.	
1Ch (1E38h)	**REG1E38**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MVD[7:0]	7:0	Version ID of MVD in dig_top.	
1Ch (1E39h)	**REG1E39**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MVOP[7:0]	7:0	Version ID of DC_Top in dig_top.	
1Dh (1E3Ah)	**REG1E3A**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_PATGEN[7:0]	7:0	Version ID of BIST Pattern gen in dig_top.	
1Dh (1E3Bh)	**REG1E3B**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_PIU[7:0]	7:0	Version ID of PIU_Top in dig_top.	
1Eh (1E3Ch)	**REG1E3C**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_PM[7:0]	7:0	Version ID of PM_Top in dig_top.	
1Eh	**REG1E3D**	**7:0**	**Default : 0x00**	**Access : RO**

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PM_TOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1E3Dh)	VER_RIU[7:0]	7:0	Version ID of RIU in dig_top.	
1Fh (1E3Eh)	**REG1E3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_SAR[7:0]	7:0	Version ID of SAR in dig_top.	
1Fh (1E3Fh)	**REG1E3F**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_SCALER[7:0]	7:0	Version ID of SC_Top in dig_top.	
20h (1E40h)	**REG1E40**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_STRLD[7:0]	7:0	Version ID of STRLD in dig_top.	
20h (1E41h)	**REG1E41**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_TSP[7:0]	7:0	Version ID of TSP in dig_top.	
21h (1E42h)	**REG1E42**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_USB20[7:0]	7:0	Version ID of USB 2.0 in dig_top.	
21h (1E43h)	**REG1E43**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_VD[7:0]	7:0	Version ID of VD in dig_top.	
22h (1E44h)	**REG1E44**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_VD_MCU[7:0]	7:0	Version ID of VD_MCU in dig_top.	
22h (1E45h)	**REG1E45**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_VD_MCU32[7:0]	7:0	Version ID of VD_MHEG5 in dig_top.	
23h (1E46h)	**REG1E46**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_VE[7:0]	7:0	Version ID of VE in dig_top.	
23h (1E47h)	**REG1E47**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_VIF[7:0]	7:0	Version ID of VIF in dig_top.	
24h (1E48h)	**REG1E48**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_ANA_MISC[7:0]	7:0	Version ID of ANA_MISC in dig_top.	
24h (1E49h)	**REG1E49**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_G3D[7:0]	7:0	Version ID of G3D in dig_top.	
25h (1E4Ah)	**REG1E4A**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_R2[7:0]	7:0	Version ID of R2 in dig_top.	
25h (1E4Bh)	**REG1E4B**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MCU_IF[7:0]	7:0	Version ID of MCU_IF in dig_top.	
26h (1E4Ch)	**REG1E4C**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_DB_BUS[7:0]	7:0	Version ID of db_bus (debug bus) in dig_top.	
26h (1E4Dh)	**REG1E4D**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_DISP_IPATH[7:0]	7:0	Version ID of DISP_IPATH in dig_top.	

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PM_TOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
27h (1E4Eh)	**REG1E4E**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_MFE[7:0]	7:0	Version ID of MFE (H.264+M4VE) in dig_top.	
27h (1E4Fh)	**REG1E4F**	**7:0**	**Default : 0x00**	**Access : RO**
	VER_AVLINK[7:0]	7:0	Version ID of AV_Link in dig_top.	
66h (1ECCh)	**REG1ECC**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_ID_SHADOW[7:0]	7:0	Chip ID.	
66h (1ECDh)	**REG1ECD**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_ID_SHADOW[15:8]	7:0	See description of '1ECCh'.	
67h (1ECEh)	**REG1ECE**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_VERSION_SHADOW[7:0]	7:0	Chip Version.	
67h (1ECFh)	**REG1ECF**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_REVISION_SHADOW[7:0]	7:0	Chip Revision.	

IRQ Register (Bank = 2B)

IRQ Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2B00h)	**REG2B00**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst0; 0/1 : not force/force.	
00h (2B01h)	**REG2B01**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_15_0_[15:8]	7:0	See description of '2B00h'.	
04h (2B08h)	**REG2B08**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst0; 0/1: not mask/mask.	
04h (2B09h)	**REG2B09**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_15_0_[15:8]	7:0	See description of '2B08h'.	
08h (2B10h)	**REG2B10**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
08h (2B11h)	**REG2B11**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '2B10h'.	
0Ch	**REG2B18**	**7:0**	**Default : 0xFF**	**Access : R/W**

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IRQ Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2B18h)	HST0_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst0; Write 1 to clear fiq interrupt[15:0] of hst0.	
0Ch (2B19h)	**REG2B19**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_STATUS_15_0_[15:8]	7:0	See description of '2B18h'.	
10h (2B20h)	**REG2B20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst0; 0/1 : not force/force.	
10h (2B21h)	**REG2B21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_15_0_[15:8]	7:0	See description of '2B20h'.	
14h (2B28h)	**REG2B28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst0; 0/1: not mask/mask.	
14h (2B29h)	**REG2B29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_15_0_[15:8]	7:0	See description of '2B28h'.	
18h (2B30h)	**REG2B30**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
18h (2B31h)	**REG2B31**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '2B30h'.	
1Ch (2B38h)	**REG2B38**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst0;	
1Ch (2B39h)	**REG2B39**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_15_0_[15:8]	7:0	See description of '2B38h'.	

ICACHE Register (Bank = 2B)

ICACHE Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
80h	**REG2B00**	**7:0**	**Default : 0x00**	**Access : R/W**

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ICACHE Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2B00h)	SDRAM_CODE_MAP[7:0]	7:0	SDRAM CODE MAP ADDRESS, 64Kbyte UNIT. Bit[15:12] is don't core. The DRAM byte address would be. DRAM_adr[15:0] = cpu_addr[15:0]. DRAM_adr[27:16] = cpu_adr[23:16] + SDRAM_CODE_MAP[11:0]. Note: Cpu_addr[23:0] is the 8051's instruction address.	
80h (2B01h)	**REG2B01**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDRAM_CODE_MAP[15:8]	7:0	See description of '2B00h'.	
81h (2B02h)	**REG2B02**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_L[7:0]	7:0	CPU address[15:0].	
81h (2B03h)	**REG2B03**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_L[15:8]	7:0	See description of '2B02h'.	
82h (2B04h)	**REG2B04**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_H[7:0]	7:0	CPU address[23:16].	
82h (2B05h)	**REG2B05**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_H[15:8]	7:0	See description of '2B04h'.	
83h (2B06h)	**REG2B06**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA0[7:0]	7:0	Icache Return data[7:0] to CPU.	
83h (2B07h)	**REG2B07**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA0[15:8]	7:0	See description of '2B06h'.	
84h (2B08h)	**REG2B08**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA1[7:0]	7:0	Reserved.	
84h (2B09h)	**REG2B09**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA1[15:8]	7:0	See description of '2B08h'.	
85h (2B0Ah)	**REG2B0A**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_MISS_COUNT[7:0]	7:0	Cahce MISS COUNTER.	
85h (2B0Bh)	**REG2B0B**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_MISS_COUNT[15:8]	7:0	See description of '2B0Ah'.	
86h (2B0Ch)	**REG2B0C**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_HIT_COUNT[7:0]	7:0	Cahce HIT COUNTER.	
86h (2B0Dh)	**REG2B0D**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_HIT_COUNT[15:8]	7:0	See description of '2B0Ch'.	
87h	**REG2B0E**	**7:0**	**Default : 0x00**	**Access : RO**

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ICACHE Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2B0Eh)	-	7:3	Reserved.	
	REQUEST2DRAM	2	Request to DRAM flag.	
	CPU_WAIT	1	Cpu wait flag, 1: wait, 0: hit.	
	REQUEST2SPI	0	Request to SPI flag.	
88h (2B10h)	**REG2B10**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CACHE_FSM[3:0]	3:0	Cache fsm.	
8Ah (2B14h)	**REG2B14**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMP[5:0]	7:2	Reserved.	
	HIT_RATE_COUNTER_START	1	Start counter for hit rate calculater.	
	HIT_RATE_COUNTER_CLEAR	0	Clearcounter for hit rate calculater.	
8Ah (2B15h)	**REG2B15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMP[13:6]	7:0	See description of '2B14h'.	
8Bh (2B16h)	**REG2B16**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ICACHE_ABORT_EN	1	Enable icache abort. 1: Enable. 0: Disable. This bit will be ignored, once HK mcu run at DRAM.	
	ICACHE_PRE_FETCH_EN	0	Enable icache pre-fetch. 1: Enable. 0: Disable. This bit will be ignored, once HK mcu run at DRAM.	
90h (2B20h)	**REG2B20**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	CACHE_BY_PASS	0	Icache By-pass. 1: Bypass. 0: Not bypass.	

XDMIU Register (Bank = 2B)

XDMIU Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
C0h	**REG2B80**	**7:0**	**Default : 0x00**	**Access : R/W**

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XDMIU Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2B80h)	-	7:1	Reserved.	
	SOFTWARE_RST	0	Set 1 to reset HK_MCU XDATA2MIU.	
C1h (2B82h)	**REG2B82**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED1[7:0]	7:0	RESERVED1.	
C1h (2B83h)	**REG2B83**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED1[15:8]	7:0	See description of '2B82h'.	
C2h (2B84h)	**REG2B84**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	XB_SDR_MAP_EN	2	Set 1 to enable the mapping of HK_MCU XDATA to MIU.	
	XD2MIU_WPRI	1	XDATA2MIU write Priority.	
	XD2MIU_RPRI	0	XDATA2MIU read Priority.	
C3h (2B86h)	**REG2B86**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR[7:0]	7:0	The low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR[15:8] > xdata_addr[15:10] >= XB_ADDR[7:0]),	
C3h (2B87h)	**REG2B87**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR[15:8]	7:0	See description of '2B86h'.	
C4h (2B88h)	**REG2B88**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP[7:0]	7:0	The low byte address to access xdata from MIU. The granularity is 64k bytes. The actual address[23:0] to miu would be{SDR_XD_MAP[11:8], SDR_XD_MAP[7:0],xdata_addr[15:4]}, where xdata_addr[15:0] is mcu xdata address of 64k bytes.	
C4h (2B89h)	**REG2B89**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP[15:8]	7:0	See description of '2B88h'.	
C5h (2B8Ah)	**REG2B8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR_1[7:0]	7:0	The low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR_1[15:8] > xdata_addr[15:10] >= XB_ADDR_1[7:0]),	
C5h (2B8Bh)	**REG2B8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR_1[15:8]	7:0	See description of '2B8Ah'.	
C6h	**REG2B8C**	**7:0**	**Default : 0x00**	**Access : R/W**

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XDMIU Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2B8Ch)	SDR_XD_MAP_1_0[7:0]	7:0	The low byte address to access xdata from MIU. The granularity is 4k bytes. Where xdata_addr[15:0] is mcu xdata address of 64k bytes.	
C6h (2B8Dh)	**REG2B8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_0[15:8]	7:0	See description of '2B8Ch'.	
C7h (2B8Eh)	**REG2B8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_1[7:0]	7:0	The actual byte address for SDRAM would be. {SDR_XD_MAP_1_1[3:0], reg_sdr_xd_map_1_0[15:0], xdata_addr[11:0]}. Note: Xdata_addr[11:0] comes from MCU51.	
C7h (2B8Fh)	**REG2B8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_1[15:8]	7:0	See description of '2B8Eh'.	

PM_MISC Register (Bank = 2E)

PM_MISC Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2E00h)	**REG2E00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MIIC_TRIG_BY_WFI	2	0: Miic dma is triggered by riu. 1: Miic dma is triggered by wfi.	
	NONPM_REQ_MASK	1	Mask requests from NonPM domain.	
	-	0	Reserved.	
02h ~ 03h (2E04h ~ 2E07h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
09h (2E13h)	**REG2E13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HK51_UART0_EN	4	Select uart source via PAD_DDCA. 1 => HK MCU51 uart0. 0 => dig_mux (reg_uart_sel0). Please refer to "reg_uart_sel0" in reg_chip_top.xls.	
	UART_RX_ENABLE	3	1: Enable uart rx via PAD_DDCA for dig_mux (reg_uart_sel0). Please refer to "reg_uart_sel0" in reg_chip_top.xls.	

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PM_MISC Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	2:0	Reserved.	
1Eh (2E3Ch)	**REG2E3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	CHIP_CONFIG_VALUE[5:0]	5:0	Chip_config value. {PAD_32kout, PAD_NAND_CE1Z, PAD_NAND_ALE, PAD_NAND_CLE, PAD_NAND_WEZ, PAD_NAND_REZ}.	
1Fh (2E3Eh)	**REG2E3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CHIP_CONFIG_OVERWRITE_EN[5:0]	5:0	Chip_config overwrite enable ([5] for pmic, [4] for xtal, [3:0] for boot).	
1Fh (2E3Fh)	**REG2E3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CHIP_CONFIG_OVERWRITE_VAL[5:0]	5:0	Chip_config overwrite value. [5]: 0 - without pmic ; 1 - with pmic. [4]: 0 - 24m xtal ; 1 - 16m tcxo. [3:0] : refer to tmux.	
20h (2E40h)	**REG2E40**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_MCU_CLK	7	Switch clk_mcu by glitch-free clock switch (between clk_mcu_p and int_xtali_buf).	
	-	6:4	Reserved.	
	CKG_MCU[3:0]	3:0	Clock selection for clk_mcu. [0]: Gate; [1]: inv; [3:2]: as following. 'd0: 144MHz (mpll). 'd1: 24MHz (xtal). 'd2: 4MHz (rc). 'd3: 32KHz (xtal).	
20h (2E41h)	**REG2E41**	**7:0**	**Default : 0x01**	**Access : R/W**
	PWRGD_SW_EN	7	Clk_mcu & clk_spi can be switched to ext_xtali automatically by pwrgd (DVDD_CORE & VD33_SHUTDN). 0: Disable this function. 1: Enable this function.	
	SW_SPI_CLK	6	Switch clk_spi by glitch-free clock switch (between clk_spi_p and int_xtali_buf).	
	-	5:4	Reserved.	

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PM_MISC Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_SPI[3:0]	3:0	Clock selection for clk_spi. [0]: Gate; [1]: inv; [3:2]: as following. 'd0: 36MHz (mpll/4). 'd1: 24MHz (xtal). 'd2: 4MHz (rc). 'd3: 32KHz (xtal).	
21h (2E42h)	**REG2E42**	**7:0**	**Default : 0x20**	**Access : R/W**
	CKG_IR[2:0]	7:5	Clock selection for clk_ir. [0]: Gate; [1]: inv; [3:2]: as following. 'd0: 24MHz (xtal). 'd1: 4MHz (rc). 'd2: 1MHz (xtal div to 1). 'd3: 1MHz (rc div to 1).	
	-	4:0	Reserved.	
21h (2E43h)	**REG2E43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CKG_IR[3]	0	See description of '2E42h'.	
23h (2E46h)	**REG2E46**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_CEC[3:0]	3:0	Clock selection for clk_cec. [0]: Gate; [1]: inv; [3:2]: as following. 'd0: 1MHz (xtal div to 1). 'd1: 1MHz (rc div to 1). 'd2: 24MHz (xtal). 'd3: 4MHz (rc).	
25h (2E4Ah)	**REG2E4A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CKG_MCU_XTAL[3:0]	3:0		
25h (2E4Bh)	**REG2E4B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CKG_SPI_XTAL[3:0]	3:0		
29h (2E52h)	**REG2E52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:3	Reserved.	
	MCU51_PWR_GNT	2	Mcu51_top power grant.	
	MCU51_PWR_RQ	1	Mcu51_top power request.	
	MCU51_ISO_OFF	0	Mcu51_top isolation off.	

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PM_MISC Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
29h (2E53h)	**REG2E53**	**7:0**	**Default : 0x80**	**Access : R/W**
	CPUX_SW_RSTZ[3:0]	7:4	Sw rstz toggle, active low. [0]: 8051 sw rstz. [1]: Aeon sw rstz. [2]: Mips sw rstz. [3]: Die-domain's global sw rstz.	
	FIRE[3:0]	3:0	Sw rst FIRE, active high. [0]: 8051 sw rst. [1]: Aeon sw rst. [2]: Mips sw rst. [3]: Die-domain's global sw rst.	
2Ah (2E54h)	**REG2E54**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU0[7:0]	7:0	Rst_ctrl's password of 8051 (16'h829f).	
2Ah (2E55h)	**REG2E55**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU0[15:8]	7:0	See description of '2E54h'.	
2Bh (2E56h)	**REG2E56**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU1[7:0]	7:0	Rst_ctrl's password of aeon (16'hb8d2).	
2Bh (2E57h)	**REG2E57**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU1[15:8]	7:0	See description of '2E56h'.	
2Ch (2E58h)	**REG2E58**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU2[7:0]	7:0	Rst_ctrl's password of mips (16'hb8d3).	
2Ch (2E59h)	**REG2E59**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU2[15:8]	7:0	See description of '2E58h'.	
2Dh (2E5Ah)	**REG2E5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU3[7:0]	7:0	Rst_ctrl's password of die-domain (16'hb8d4).	
2Dh (2E5Bh)	**REG2E5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_CPU3[15:8]	7:0	See description of '2E5Ah'.	
2Eh (2E5Ch)	**REG2E5C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TOP_SW_RST[7:0]	7:0	Fire reset for global chip, active by password (8'h79).	
2Eh (2E5Dh)	**REG2E5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MCU_QUICK_RST	0	Quick reset for 8051, aeon & mips. 0: 30ms, 1: 1us.	
3Fh	**REG2E7E**	**7:0**	**Default : 0x00**	**Access : RO**

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PM_MISC Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2E7Eh)	FRO_CLK_CNT[7:0]	7:0	Fro clock counter value.	
3Fh (2E7Fh)	**REG2E7F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:5	Reserved.	
	FRO_CLK_DET_EN	4	Fro clock detection enable.	
	FRO_CLK_CNT[11:8]	3:0	See description of '2E7Eh'.	
49h (2E92h)	**REG2E92**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:6	Reserved.	
	PWRGD_CLKSW	5	Register power good clock gating status.	
	PWRGD_CLKSW_WC	4	Register to clear power good clock switch.	
	ONCE_VDD_NG_WC3	3	Register to clear once vdd not good.	
	ONCE_VDD_NG_WC2	2	Register to clear once vdd not good.	
	ONCE_VDD_NG_WC1	1	Register to clear once vdd not good.	
	ONCE_VDD_NG_WC0	0	Register to clear once vdd not good.	
52h (2EA4h)	**REG2EA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[7:0]	7:0	SCRATCHPAD.	
52h (2EA5h)	**REG2EA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[15:8]	7:0	See description of '2EA4h'.	
53h (2EA6h)	**REG2EA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[23:16]	7:0	See description of '2EA4h'.	
53h (2EA7h)	**REG2EA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[31:24]	7:0	See description of '2EA4h'.	
54h (2EA8h)	**REG2EA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[39:32]	7:0	See description of '2EA4h'.	
54h (2EA9h)	**REG2EA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[47:40]	7:0	See description of '2EA4h'.	
55h (2EAAh)	**REG2EAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[55:48]	7:0	See description of '2EA4h'.	
55h (2EABh)	**REG2EAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCHPAD[63:56]	7:0	See description of '2EA4h'.	
61h	**REG2EC2**	**7:0**	**Default : 0x00**	**Access : RO**

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PM_MISC Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2EC2h)	POWER_NOT_GOOD[2:0]	7:5	Chip_top's power is not good once. [0]: DVDD_ARM_PWRGD. [1]: DVDD_CORE_PWRGD. [2]: AVDD_IO_PWRGD. [3]: AVDD_ANA_PWRGD. (This is one-way register).	
	CHIP_TOP_POWERGOOD	4	CHIP_TOP_POWERGOOD after iso_control.	
	-	3:0	Reserved.	
61h (2EC3h)	**REG2EC3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	POWER_NOT_GOOD[3]	0	See description of '2EC2h'.	

WDT Register (Bank = 30)

WDT Register (Bank = 30)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3000h)	**REG3000**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	WDT_CLR	0	Write "1' to re-start WDT.	
02h (3004h)	**REG3004**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_RST_FLAG	0	assert: WDT reset has been occurred; Write "1" to clear.	
02h (3005h)	**REG3005**	**7:0**	**Default : 0x09**	**Access : R/W**
	WDT_RST_LEN[7:0]	7:0	Length of WDT reset. 0: One xtal clock; 1: two xtal clock; 3.....	
03h (3006h)	**REG3006**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_INT[7:0]	7:0	WDT interrupt period; Interrupt asserts when "WDT counter [31:16]" is equal to WDT_INT and "WDT counter[15:0]" is equal to 0x0000.	
03h (3007h)	**REG3007**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_INT[15:8]	7:0	See description of '3006h'.	
04h	**REG3008**	**7:0**	**Default : 0xFF**	**Access : R/W**

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WDT Register (Bank = 30)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3008h)	WDT_MAX[7:0]	7:0	WDT period maximum value. WDT enable if WDT_MAX is not equal to 0x00000000.	
04h (3009h)	**REG3009**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_MAX[15:8]	7:0	See description of '3008h'.	
05h (300Ah)	**REG300A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_MAX[23:16]	7:0	See description of '3008h'.	
05h (300Bh)	**REG300B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_MAX[31:24]	7:0	See description of '3008h'.	

TIMER0 Register (Bank = 30)

TIMER0 Register (Bank = 30)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (3020h)	**REG3020**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER_TRIG	1	set: Enable timer counting one time (from 0 to max, then stop). clear: By reset itself OR set reg_timer_en.	
	TIMER_EN	0	set: Enable timer counting rolled (from 0 to max, then rolled). clear: By reset itself OR set reg_timer_trig.	
10h (3021h)	**REG3021**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TIMER_INT_EN	0	set: Enable interrupt. clear: By reset itself.	
11h (3022h)	**REG3022**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	TIMER_HIT	0	assert: When counter enabled and matches reg_timer_max. deassert: By write 1 OR set reg_timer_en, reg_timer_once, reg_timer_max.	
12h (3024h)	**REG3024**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
12h (3025h)	**REG3025**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[15:8]	7:0	See description of '3024h'.	

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TIMER0 Register (Bank = 30)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
13h (3026h)	**REG3026**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[23:16]	7:0	See description of '3024h'.	
13h (3027h)	**REG3027**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[31:24]	7:0	See description of '3024h'.	
14h (3028h)	**REG3028**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
14h (3029h)	**REG3029**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[15:8]	7:0	See description of '3028h'.	
15h (302Ah)	**REG302A**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[23:16]	7:0	See description of '3028h'.	
15h (302Bh)	**REG302B**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[31:24]	7:0	See description of '3028h'.	

TIMER1 Register (Bank = 30)

TIMER1 Register (Bank = 30)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (3040h)	**REG3040**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER_TRIG	1	set: Enable timer counting one time (from 0 to max, then stop). clear: By reset itself OR set reg_timer_en.	
	TIMER_EN	0	set: Enable timer counting rolled (from 0 to max, then rolled). clear: By reset itself OR set reg_timer_trig.	
20h (3041h)	**REG3041**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TIMER_INT_EN	0	set: Enable interrupt. clear: By reset itself.	
21h (3042h)	**REG3042**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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TIMER1 Register (Bank = 30)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TIMER_HIT	0	assert: When counter enabled and matches reg_timer_max. deassert: By write 1 OR set reg_timer_en, reg_timer_once, reg_timer_max.	
22h (3044h)	**REG3044**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
22h (3045h)	**REG3045**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[15:8]	7:0	See description of '3044h'.	
23h (3046h)	**REG3046**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[23:16]	7:0	See description of '3044h'.	
23h (3047h)	**REG3047**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[31:24]	7:0	See description of '3044h'.	
24h (3048h)	**REG3048**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
24h (3049h)	**REG3049**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[15:8]	7:0	See description of '3048h'.	
25h (304Ah)	**REG304A**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[23:16]	7:0	See description of '3048h'.	
25h (304Bh)	**REG304B**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[31:24]	7:0	See description of '3048h'.	

PIU_MISC0 Register (Bank = 3C)

PIU_MISC0 Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (3C1Ch)	**REG3C1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CSZ_SPI_FLASH1	0	Multi-SPI Flash chip select. 1: Disable #1 SPI flash. 0: Enable #1 SPI flash.	
0Eh (3C1Dh)	**REG3C1D**	**7:0**	**Default : 0xE0**	**Access : R/W**
	CSZ_SPI_FLASH4	7	Multi-SPI Flash chip select. 1: Disable #4 SPI flash. 0: Enable #4 SPI flash.	

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PIU_MISC0 Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CSZ_SPI_FLASH3	6	Multi-SPI Flash chip select. 1: Disable #3 SPI flash. 0: Enable #3 SPI flash.	
	CSZ_SPI_FLASH2	5	Multi-SPI Flash chip select. 1: Disable #2 SPI flash. 0: Enable #2 SPI flash.	
	-	4:0	Reserved.	
26h (3C4Ch)	**REG3C4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[7:0]	7:0	RESERVED0[5:0]: for spi clock selection. Bit[0]: for gating clock. Bit[1]: for clock invert. Bit[5]: 0 select xtal. 1 clock gen. Bit [4:2]. 000: XTAL. 001: 27M. 010: 36M. 011: 43M. 100: 54M. 101: 72M. 110: 86M. 111: 108M. Bit[8]: 0: not reset SPI. 1: Reset SPI (please ensure code executed in DRAM). Bit[9]: 2x read SPI Flash command for MXIC. Bit[10]: 2x read SPI Flash command for Winbond.	
26h (3C4Dh)	**REG3C4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[15:8]	7:0	See description of '3C4Ch'.	
27h (3C4Eh)	**REG3C4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[23:16]	7:0	See description of '3C4Ch'.	
27h (3C4Fh)	**REG3C4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[31:24]	7:0	See description of '3C4Ch'.	
7Fh (3CFEh)	**REG3CFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TEST_SEL[2:0]	2:0		

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IR Register (Bank = 3D)

IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3D00h)	**REG3D00**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RC_FIFO_WFIRST	7	RC FIFO write first. 0: Read first; 1: write first.	
	RC_FIFO_CLEAR	6	RC FIFO clear. 0: Disable; 1: enable.	
	RC_AUTOCONFIG	5	Auto config RC5 and RC6 setting.	
	RC6_LS_THR_L[4:0]	4:0	RC6 leading pulse threshold * 32.	
00h (3D01h)	**REG3D01**	**7:0**	**Default : 0x70**	**Access : R/W**
	RCIN_INV	7	RC input invert. 0=disabe;1=enable.	
	RC_DEBUG_SEL[2:0]	6:4	111: PM RC anykey wakeup fix enable. Others: Reserved.	
	RC_WKUP_EN	3	RC wake up enable. 0=disable; 1=enable.	
	RC5EXT_EN	2	Extended RC-5 enable. 0=disable; 1=enable.	
	RC6_EN	1	0= RC5;1= RC6.	
	RC_EN	0	RC reciever enable. 0=disbale; 1=enable.	
01h (3D02h)	**REG3D02**	**7:0**	**Default : 0xA0**	**Access : R/W**
	RC_LONGPULSE_THR[7:0]	7:0	RC long pulse threshold. To judge long pulse or not.	
01h (3D03h)	**REG3D03**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	RC_LONGPULSE_THR[12:8]	4:0	See description of '3D02h'.	
02h (3D04h)	**REG3D04**	**7:0**	**Default : 0xC0**	**Access : R/W**
	RC_LONGPULSE_MAR[7:0]	7:0	RC6 long pulse margin, only for RC6.	
02h (3D05h)	**REG3D05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RC6_LS_THR_H[2:0]	4:2	RC6 leading pulse threshold * 1024.	
	RC_LONGPULSE_MAR[9:8]	1:0	See description of '3D04h'.	
03h	**REG3D06**	**7:0**	**Default : 0x41**	**Access : R/W**

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3D06h)	RC_INT_THR[6:0]	7:1	RC Integrator threshold * 8. To judge 0 or 1.	
	RC6_ECO_EN	0	RC6 ECO function enable.	
03h (3D07h)	**REG3D07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RC_CLKDIV[4:0]	4:0	RC operating clock divisor ratio.	
04h (3D08h)	**REG3D08**	**7:0**	**Default : 0x3C**	**Access : R/W**
	RC_WDOG_COUNT[7:0]	7:0	RC watch dog counter (based on 2kHz for 1MHz clock input).	
04h (3D09h)	**REG3D09**	**7:0**	**Default : 0x10**	**Access : R/W**
	RC_TIMEOUT_COUNT[7:0]	7:0	RC timeout counter (based on 0.5kHz for 1MHz clock input).	
05h (3D0Ah)	**REG3D0A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	COMP_RCKEY1[7:0]	7:0	RC power wakeup key1.	
05h (3D0Bh)	**REG3D0B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	COMP_RCKEY2[7:0]	7:0	RC power wakeup key2.	
06h (3D0Ch)	**REG3D0C**	**7:0**	**Default : 0x00**	**Access : RO**
	RCKEY_ADDRESS[7:0]	7:0	RC decode address. RC5: {2'b0,toggle,address[4:0]}. RC6: Address[7:0].	
06h (3D0Dh)	**REG3D0D**	**7:0**	**Default : 0x00**	**Access : RO**
	RCKEY_COMMAND[7:0]	7:0	RC decode command. RC5: {repeat,1'b0,command[5:0]}. RC5EXT: {repeat,command[6:0]}. RC6: Command[7:0].	
07h (3D0Eh)	**REG3D0E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RCKEY_MISC[4:0]	4:0	RC6 decode MISC data. [2:0]: MODE[2:0]. [3]: Toggle. [4]: Repeat.	
08h (3D10h)	**REG3D10**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	RC_FIFO_WPTR[2:0]	6:4	RC FIFO write pointer.	
	-	3	Reserved.	
	RC_FIFO_FULL	2	RC FIFO full.	

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RC_TIMEOUT_FLAG	1	RC time-out flag. 1: Time-out.	
	RC_FIFO_EMPTY	0	RC FIFO empty.	
08h (3D11h)	**REG3D11**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	RC_FIFO_RPTR[2:0]	2:0	RC FIFO read pointer.	
09h (3D12h)	**REG3D12**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	RC_FIFO_RD_PULSE	0	RC FIFO read pulse gen.	
09h (3D13h)	**REG3D13**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	RC_WKUP_CLR	0	RC wake up clear pulse generator.	
0Ah (3D14h)	**REG3D14**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RC_ADDRESS[7:0]	7:0	RC power wakeup address.	
0Ah (3D15h)	**REG3D15**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	RC_ANYKEY_EN	1	RC anykey wakeup enable.	
	RCADR_CMP_EN	0	RC power wakeup address enable.	
40h (3D80h)	**REG3D80**	**7:0**	**Default : 0xBE**	**Access : R/W**
	IR_INV	7	Invert the polarity for input IR signal.	
	IR_INT_MASK	6	IR Interrupt request Mask for mcu.	
	IR_RPCODE_EN	5	IR Repeat Code check enable.	
	IR_LG01H_CHK_EN	4	IR Logic 0/1 High level edge Check Enable.	
	IR_DCODE_PCHK_EN	3	IR Data Code Parity Check Enable.	
	IR_CCODE0_CHK_EN	2	IR Customer Code 0 Check Enable. (There are two customer codes could be set for decoding different remote controller.).	
	IR_LDCCHK_EN	1	IR Leader Code (header + off code) Check Enable.	
	IR_EN	0	IR decode Enable for Full/Raw mode.	
40h (3D81h)	**REG3D81**	**7:0**	**Default : 0xC1**	**Access : R/W**
	IR_INT_CRC_MASK	7	Interrupt Mask for IR CRC check.	
	RAW_RPT_INT_MASK	6	Interrupt Mask for Repeat code in RAW mode.	
	-	5:4	Reserved.	

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IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	IR_BIT_INV_EN	3	Enable for IR decode logic bit inverse. 0: Disable. 1: Enable.	
	IR_KEY_MSB_FIRST	2	Enable for IR key MSB first. 0: The key data format is LSB first. (ie, key[0:7]). 1: The key data format is MSB first (ie, key[7:0]).	
	IR_SEPR_EN	1	IR Separator Code check Enable (for Mitsubishi only).	
	IR_TIMEOUT_CHK_EN	0	IR Time-Out Check Enable.	
41h (3D82h)	**REG3D82**	**7:0**	**Default : 0xF2**	**Access : R/W**
	IR_HDC_UPB[7:0]	7:0	The counter Upper Bound for Header Code.	
41h (3D83h)	**REG3D83**	**7:0**	**Default : 0x2B**	**Access : R/W**
	-	7:6	Reserved.	
	IR_HDC_UPB[13:8]	5:0	See description of '3D82h'.	
42h (3D84h)	**REG3D84**	**7:0**	**Default : 0x5E**	**Access : R/W**
	IR_HDC_LOB[7:0]	7:0	The counter Lower Bound for Header Code.	
42h (3D85h)	**REG3D85**	**7:0**	**Default : 0x1A**	**Access : R/W**
	-	7:6	Reserved.	
	IR_HDC_LOB[13:8]	5:0	See description of '3D84h'.	
43h (3D86h)	**REG3D86**	**7:0**	**Default : 0xF9**	**Access : R/W**
	IR_OFC_UPB[7:0]	7:0	The counter Upper Bound for Off Code.	
43h (3D87h)	**REG3D87**	**7:0**	**Default : 0x15**	**Access : R/W**
	-	7:5	Reserved.	
	IR_OFC_UPB[12:8]	4:0	See description of '3D86h'.	
44h (3D88h)	**REG3D88**	**7:0**	**Default : 0x2F**	**Access : R/W**
	IR_OFC_LOB[7:0]	7:0	The counter Lower Bound for Off Code.	
44h (3D89h)	**REG3D89**	**7:0**	**Default : 0x0D**	**Access : R/W**
	-	7:5	Reserved.	
	IR_OFC_LOB[12:8]	4:0	See description of '3D88h'.	
45h (3D8Ah)	**REG3D8A**	**7:0**	**Default : 0x35**	**Access : R/W**
	IR_OFC_RP_UPB[7:0]	7:0	The counter Upper Bound for Repeat Off Code.	
45h (3D8Bh)	**REG3D8B**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	IR_OFC_RP_UPB[11:8]	3:0	See description of '3D8Ah'.	

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (3D8Ch)	**REG3D8C**	**7:0**	**Default : 0x53**	**Access : R/W**
	IR_OFC_RP_LOB[7:0]	7:0	The counter Lower Bound for Repeat Off Code.	
46h (3D8Dh)	**REG3D8D**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	IR_OFC_RP_LOB[11:8]	3:0	See description of '3D8Ch'.	
47h (3D8Eh)	**REG3D8E**	**7:0**	**Default : 0xBC**	**Access : R/W**
	IR_LG01H_UPB[7:0]	7:0	The counter Upper Bound for Logic 0/1 High level width.	
47h (3D8Fh)	**REG3D8F**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	IR_LG01H_UPB[9:8]	1:0	See description of '3D8Eh'.	
48h (3D90h)	**REG3D90**	**7:0**	**Default : 0xA4**	**Access : R/W**
	IR_LG01H_LOB[7:0]	7:0	The counter Lower Bound for Logic 0/1 High level width.	
48h (3D91h)	**REG3D91**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	IR_LG01H_LOB[9:8]	1:0	See description of '3D90h'.	
49h (3D92h)	**REG3D92**	**7:0**	**Default : 0x78**	**Access : R/W**
	IR_LG0_UPB[7:0]	7:0	The counter Upper Bound for Logic 0 width.	
49h (3D93h)	**REG3D93**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:3	Reserved.	
	IR_LG0_UPB[10:8]	2:0	See description of '3D92h'.	
4Ah (3D94h)	**REG3D94**	**7:0**	**Default : 0x48**	**Access : R/W**
	IR_LG0_LOB[7:0]	7:0	The counter Lower Bound for Logic 0 width.	
4Ah (3D95h)	**REG3D95**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	IR_LG0_LOB[10:8]	2:0	See description of '3D94h'.	
4Bh (3D96h)	**REG3D96**	**7:0**	**Default : 0xF0**	**Access : R/W**
	IR_LG1_UPB[7:0]	7:0	The counter Upper Bound for Logic 1 width.	
4Bh (3D97h)	**REG3D97**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	IR_LG1_UPB[11:8]	3:0	See description of '3D96h'.	
4Ch (3D98h)	**REG3D98**	**7:0**	**Default : 0x90**	**Access : R/W**
	IR_LG1_LOB[7:0]	7:0	The counter Lower Bound for Logic 1 width.	
4Ch	**REG3D99**	**7:0**	**Default : 0x06**	**Access : R/W**

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3D99h)	-	7:4	Reserved.	
	IR_LG1_LOB[11:8]	3:0	See description of '3D98h'.	
4Dh (3D9Ah)	**REG3D9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_SEPR_UPB[7:0]	7:0	The counter Upper Bound for Separator Code width.	
4Dh (3D9Bh)	**REG3D9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_SEPR_UPB[11:8]	3:0	See description of '3D9Ah'.	
4Eh (3D9Ch)	**REG3D9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_SEPR_LOB[7:0]	7:0	The counter Lower Bound for Separator Code width.	
4Eh (3D9Dh)	**REG3D9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_SEPR_LOB[11:8]	3:0	See description of '3D9Ch'.	
4Fh (3D9Eh)	**REG3D9E**	**7:0**	**Default : 0x8C**	**Access : R/W**
	IR_TIMEOUT_CYC[7:0]	7:0	The counter value for IR Timeout Cycles. Timeout check will start when under below condition. 1. IR_TIMEOUT_CHK_EN=1. 2. Counter value > IR_TIMEOUT_CYC.	
4Fh (3D9Fh)	**REG3D9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_TIMEOUT_CYC[15:8]	7:0	See description of '3D9Eh'.	
50h (3DA0h)	**REG3DA0**	**7:0**	**Default : 0x30**	**Access : R/W**
	IR_TIMEOUT_CLR_SW	7	IR Timeout Clear by SoftWare. 1: Enable. 0: Disable.	
	IR_TIMEOUT_CLR_SET[2:0]	6:4	IR Timeout Clear Set. 000: Timeout be clear at HDC check pass. 001: Timeout be clear at OFC check pass & Decode 0 state. 010: Timeout be clear at Customer Code check pass. 011: Timeout be clear at Key Data Code check pass. 100: S/w clear, need also to set "TIMEOUT_CLR_SW=1". . Recommend: Set 011 for NEC-like format.	
	-	3	Reserved.	
	IR_TIMEOUT_CYC[18:16]	2:0	See description of '3D9Eh'.	

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IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
50h (3DA1h)	**REG3DA1**	**7:0**	**Default : 0x1F**	**Access : R/W**
	IR_CCODE_BYTE	7	IR Customer Code Byte setting (full mode use only). 0: 1 byte customer code. 1: 2 bytes customer code. default: 1'b1 (for NEC format).	
	IR_CODE_BIT_NUM[6:0]	6:0	IR data code total bits. 00: 1 bit. 01: 2 bits. 10: 3 bits. .. 7f: 128 bits.	
51h (3DA2h)	**REG3DA2**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	RPT_FLAG_CLR_RAW	7	Interrupt Flag Clear for "IR repeat code flag in RAW mode". 1: Clear interrupt flag. 0: Not clear interrupt flag.	
	-	6	Reserved.	
	IR_SEPR_BIT[5:0]	5:0	IR Separator Bits setting (Only used for Mitsubishi format in full mode). The code data bit decode after this bit will into separator state when REG_IR_SEPR_EN=1 (3D81h[1]).	
51h (3DA3h)	**REG3DA3**	**7:0**	**Default : 0x0F**	**Access : R/W, WO**
	IR_FIFO_CLR	7	IR FIFO Clear Pulse Generation. 1: Generate 1T fifo clear pulse. 0: Normal operation. It is recommended to clear ir fifo when leaving power down mode.	
	IR_SW_FIFO_EN	6	SW FIFO mode enable (Decoder will help to save sw counter value and its pn_shot_flag into FIFO). 0: Disable. 1: Enable.	
	IR_SHOT_SEL[1:0]	5:4	The pshot/nshot selection for internal counter (Only used in S/W mode). 2'b01 : only pshot edge detect for counter. 2'b10 : only nshot edge detect for counter. 2'b00/11 : both pshot and nshot edge detect for counter.	

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IR_FIFO_FULL_EN	3	IR FIFO Full Enable (Used in Full/Raw mode). 0: Disable FIOF Full (data can be written over when FIFO is full). 1: Enable FIFO Full (data will be discarded when FIFO is full).	
	IR_FIFO_DEPTH[2:0]	2:0	FIFO Depth (for decoded IR code data or IR raw data, not for S/W mode counter data), totally support 16 bytes depth. 000: 9 bytes. 001: 10 bytes. 010: 11 bytes. 011: 12 bytes. 100: 13 bytes. 101: 14 bytes. 110: 15 bytes. 111: 16 bytes. Recommend: 16'bytes (3'b111).	
52h (3DA4h)	**REG3DA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CCODE0[7:0]	7:0	IR Customer Code 0. (There are two customer codes could be set for decoding different remote controller. That is, we can decode 2 different remote controllers with same format. Also, each key have its flag to identify the key is come from which remote TX.).	
52h (3DA5h)	**REG3DA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CCODE0[15:8]	7:0	See description of '3DA4h'.	
53h (3DA6h)	**REG3DA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_GLHRM_NUM[7:0]	7:0	Glitch Removal Number for crystal based counter. The glitches will be removed whenever their cycle width below the GLHRM_NUM cycle.	
53h (3DA7h)	**REG3DA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_GLHRM_NUM_H[1:0]	7:6	Glitch Removal Number for crystal based counter. (exteneded).	
	IR_DECOMODE[1:0]	5:4	IR Decode Mode selection. 00/11 : Full decode mode (NEC and NEC-like format). 01: S/W mode (shot mode, output edge count value). 10: Raw mode (header decode only, output raw data).	

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IR_GLHRM_EN	3	Glitch Removal Enable.	
	IR_GLHRM_NUM[10:8]	2:0	See description of '3DA6h'.	
54h (3DA8h)	**REG3DA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CKDIV_NUM[7:0]	7:0	The Divided Number of IR decoder input clock, the divided clock is for internal counter use. The input clock source of IR decoder is (XTAL/4) MHz. 8_h00: Divided by 1. 8_h01: Divided by 2. .. 8_hFF: Divided by 256. Recommend: 8_h02 for Xtal clock=14.318MHz. 8_h05 for Xtal clock=25.00MHz.	
54h (3DA9h)	**REG3DA9**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_KEY_DATA[7:0]	7:0	IR Key Data output. (for Full/Raw mode data). After reading IR_KEY_DATA (3DA9h), you must set IR_FIFO_RD_PULSE=1 (3DB0h[0]) for internal fifo read pointer go to the next one.	
55h (3DAAh)	**REG3DAA**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_SHOT_CNT[7:0]	7:0	IR Shot Count value output in s/w mode, the type of shot is select from IR_SHOT_SEL (3DA3h[5:4]).	
55h (3DABh)	**REG3DAB**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_SHOT_CNT[15:8]	7:0	See description of '3DAAh'.	
56h (3DACh)	**REG3DAC**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	IR_TX1_FLAG	6	IR remote controller TX1 send flag (This flag is only used for Full Decode Mode). 0: IR key data was sent from TX0. 1: IR key data was sent from TX1. PS: Before using this flag, you must set ir_ccode0_chk_en/ ir_ccode1_chk_en/ ir_ccode0/ ir_ccode1 for this feature.	

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IR_DATA_LOST_STATUS	5	IR data lost flag (Just for testing and system monitor purpose). This flag can only be used for those cases which decoded data been saved into FIFO. (1) full decode mode. (2) raw decode mode. (3) SW decode FIFO mode (pure "SW decode mode" cannot supported !).	
	IR_SHOT_P	4	IR shot type (pshot/nshot) in s/w mode. 0: Nshot occurs. 1: Pshot occurs.	
	-	3	Reserved.	
	IR_SHOT_CNT[18:16]	2:0	See description of '3DAAh'.	
56h (3DADh)	**REG3DAD**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_RC_WKUP_FLAG	7	IR RC wakeup function flag.	
	IR_NEC_WKUP_FLAG	6	IR NEC wakeup function flag.	
	IR_INT_CRC_FLAG	5	IR CRC function interrupt flag.	
	IR_INT_FLAG	4	IR normal function interrupt flag.	
	IR_FIFO_FULL	3	IR FIFO Full Flag. 1: FIFO is full. 0: FIFO is not full yet.	
	IR_TIMEOUT_FLAG	2	IR Timeout Flag. 1: Timeout occurs. 0: Not timeout yet.	
	IR_FIFO_EMPTY	1	IR FIFO Empty flag for Full/Raw mode.	
	IR_RPT_FLAG	0	IR FIFO data Repeat Flag for Full mode.	
57h (3DAEh)	**REG3DAE**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_CRC_GOLDEN[7:0]	7:0	IR CRC Golden value, calculated by hardware while entering into power down mode.This value can be read just for reference, software don't need to fill any value. (Read-Only).	
57h (3DAFh)	**REG3DAF**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_CRC_GOLDEN[15:8]	7:0	See description of '3DAEh'.	
58h	**REG3DB0**	**7:0**	**Default : 0x20**	**Access : R/W, WO**

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IR Register (Bank = 3D)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(3DB0h)	IR_WKUP_KEY_SEL[3:0]	7:4	There are 2 kinds of meaning of this register for different decode modes: (1) For IR full decode mode (ir_decomode=00 or 11). IR key byte select for wakeup key compare (Just select one byte of the decoded data for compare). 0: Select byte 0 of IR signal as IR key (1st byte of IR data bytes). 1: Select byte 1 of IR signal as IR key (2nd byte of IR data bytes). 2: Select byte 2 of IR signal as IR key (3rd byte of IR data bytes). ..... F: Select byte 15 of IR signal as IR key (7th byte of IR data bytes). . (2) For IR raw decode mode (ir_decomode=10). IR raw data select for wakeup compare. Decoder will compare the selected 4-bytes of the decoded raw data with the 4- byte wakeup key {ir_nec_comp_key4, ir_nec_comp_key3, ir_nec_comp_key2, ir_nec_comp_key1}. 0: Compare raw data [31:0] to the 4 -byte wakeup key. 1: Compare raw data [39:8] to the 4 -byte wakeup key. 2: Compare raw data [47:16] to the 4 -byte wakeup key. 3: Compare raw data [55:24] to the 4 -byte wakeup key. 4: Compare raw data [63:32] to the 4 -byte wakeup key. 5: Compare raw data [71:40] to the 4 -byte wakeup key. 6: Compare raw data [79:48] to the 4 -byte wakeup key. 7: Compare raw data [87:56] to the 4 -byte wakeup key. 8: Compare raw data [95:64] to the 4 -byte wakeup key. 9: Compare raw data [103:72] to the 4 -byte wakeup key. A: Compare raw data [111:80] to the 4 -byte wakeup key. B: Compare raw data [119:88] to the 4 -byte wakeup key. C~F: reserved.
	IR_NEC_WKUP_FLAG_CLR	3	IR wakeup flag clear of NEC (or NEC-like) format. 1: Clear pulse generate. 0: No operation.
	IR_FLAG_CLR	2	IR interrupt flag clear. 1: Clear pulse generate. 0: No operation.

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IR_CRC_FLAG_CLR	1	IR crc interrupt flag clear. 1: Clear pulse generate. 0: No operation.	
	IR_FIFO_RD_PULSE	0	IR FIFO Read Pulse. 1: Read. 0: Not read. Note: Need to set this bit to 1 after s/w read "IR_KEY_DATA" (3DA9h) (to let FIFO read pointer go to the next one).	
58h (3DB1h)	**REG3DB1**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	IR_PPM_SW_RST	0	IR PPM (NEC) decoder Soft Reset. 0: Not reset. 1: Reset. ps: Write 1 clear (write-clear register, no need to write 0).	
59h (3DB2h)	**REG3DB2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_COMP_KEY1[7:0]	7:0	IR compare key1 for wakeup function of NEC (or NEC-like) format.	
59h (3DB3h)	**REG3DB3**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_COMP_KEY2[7:0]	7:0	IR compare key2 for wakeup function of NEC (or NEC-like) format.	
5Ah (3DB4h)	**REG3DB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_ANYKEY_WKUP_EN	7	Enable for IR wakeup by any key (Customer code must matched) matched function. 0: Disable. 1: Enable.	
	IR_NEC_WKUP_EN	6	Enable for IR wakeup function of NEC (or NEC-like) format. 0: Disable. 1: Enable.	
	-	5	Reserved.	

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IR_4MAT_SEL[4:0]	4:0	IR data sequence format select for NEC-like (PPM modulation) formats. 0: Format not define, decided by code_bit assignment (ir_ccode_byte (reg_3D50h[15], ir_code_bit_num (reg_3D50h[14:8])). 1: C16D8D8P format (ex: NEC, Toshiba format). 2: C8D8 format (ex: Mitsubushi, Konka format). 3: C4D8C4D8P format (ex: RCA format). 4: C26D8D8P format. 5: C32D8D8P format. 6: C5D6C5D6P format. 7: C6D6C6D6P format. 8: D7C6 format (ex: Sony-D7C6). 9: D7C8 format (ex: Sony-D7C8). 10: D8C6 format (ex: Sony-D8C6). 11: D5_only format (ex: MV500). 12: S1C4D6 format (ex: IRT1250). 13: C5D6D4 format (ex: LR3715M). 14: R1T1C3D6 format (ex: M3004 LAB1-Carrier). 15~31: Reserved. Note: S = System Code. C = Customer Code Bits, (ex: C8= customer code 8bits). D = Data (Key) Code Bits, (ex: D8= data code 8bits). P = Format with Parity Check (ex: 3th byte and 4th byte of NEC format).	
5Bh (3DB6h)	**REG3DB6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_COMP_KEY3[7:0]	7:0	IR compare key3 for wakeup function of NEC (or NEC-like) format.	
5Bh (3DB7h)	**REG3DB7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_COMP_KEY4[7:0]	7:0	IR compare key4 for wakeup function of NEC (or NEC-like) format.	
5Ch (3DB8h)	**REG3DB8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_WKEY1_BIT_EN[7:0]	7:0	IR wakeup key1 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
5Ch	**REG3DB9**	**7:0**	**Default : 0xFF**	**Access : R/W**

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IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3DB9h)	IR_NEC_WKEY2_BIT_EN[7:0]	7:0	IR wakeup key2 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
5Dh (3DBAh)	**REG3DBA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_WKEY3_BIT_EN[7:0]	7:0	IR wakeup key3 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
5Dh (3DBBh)	**REG3DBB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_WKEY4_BIT_EN[7:0]	7:0	IR wakeup key4 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
60h (3DC0h)	**REG3DC0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_CCODE1[7:0]	7:0	IR Customer Code 1. (There are two customer codes could be set for decoding different remote controllers. That is, we can decode 2 different remote controllers with same format. Also, each key have its flag to identify the key is come from which remote TX.).	
60h (3DC1h)	**REG3DC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CCODE1[15:8]	7:0	See description of '3DC0h'.	
61h (3DC2h)	**REG3DC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IR_CCODE1_CHK_EN	0	IR Customer Code 1 Check Enable. (There are two customer codes could be set for decoding different remote controllers.).	
61h (3DC3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
63h (3DC6h)	**REG3DC6**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	DATA_LOST_STS_CLR	0	IR data lost flag clear. 0: No action. 1: Clear (write clear pulse).	

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HK NONPM REGISTER TABLE

32BIT_MCU Register (Bank = 1003)

32BIT_MCU Register (Bank = 1003)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (100380h)	**REG100380**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	WPROTEN	4	Write protection region enable. 0: Disable. 1: Enable.	
	-	3:2	Reserved.	
	IOWINORDER	1	IO/MIU write in-order. 0: No in-order. 1: In-order.	
	NCDRAMPOSTW	0	NC write DRAM space post write and merge. 0: Disable. 1: Enable.	
60h (1003C0h)	**REG1003C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM1_BASE[7:0]DCCDCCD	7:0	Data dram1 address base [15:0]. . usage: Assign DRAM_WRprot = reg_WprotEn &. !((dcu_address[31:16] & DRAM1_mask[15:0]) == DRAM1_BASE[15:0] |. (dcu_address[31:16] & DRAM2_mask[15:0]) == DRAM2_base[15:0]);	
60h (1003C1h)	**REG1003C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM1_BASE[15:8]	7:0	See description of '1003C0h'.	
61h (1003C2h)	**REG1003C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM1_MASK[7:0]	7:0	Data dram1 address mask [15:0].	
61h (1003C3h)	**REG1003C3**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM1_MASK[15:8]	7:0	See description of '1003C2h'.	
62h (1003C4h)	**REG1003C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM2_BASE[7:0]	7:0	Data dram2 address base [15:0].	
62h (1003C5h)	**REG1003C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM2_BASE[15:8]	7:0	See description of '1003C4h'.	
63h	**REG1003C6**	**7:0**	**Default : 0x00**	**Access : R/W**

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32BIT_MCU Register (Bank = 1003)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1003C6h)	DRAM2_MASK[7:0]	7:0	Data dram2 address mask [15:0].	
63h (1003C7h)	**REG1003C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM2_MASK[15:8]	7:0	See description of '1003C6h'.	
74h (1003E8h)	**REG1003E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DMASK0[7:0]	7:0	Data qmem address mask [15:0].	
74h (1003E9h)	**REG1003E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DMASK0[15:8]	7:0	See description of '1003E8h'.	
75h (1003EAh)	**REG1003EA**	**7:0**	**Default : 0xF0**	**Access : R/W**
	QMEM_DMASK1[7:0]	7:0	Data qmem address mask [31:16].	
75h (1003EBh)	**REG1003EB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	QMEM_DMASK1[15:8]	7:0	See description of '1003EAh'.	
76h (1003ECh)	**REG1003EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADDR0[7:0]	7:0	Data qmem matching address [15:0].	
76h (1003EDh)	**REG1003ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADDR0[15:8]	7:0	See description of '1003ECh'.	
77h (1003EEh)	**REG1003EE**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADD1[7:0]	7:0	Data qmem matching address [31:16]. . QMEM_DMASK and QMEM_DADDR usage : Only works for data memory accesses. Let CPU_DADDR[31:0] represents CPU's data access addresses. When. ({REG16_QM_DMASK1, REG16_QM_DMASK0} && CPU_DADDR[31:0]) is equal to. .	
77h (1003EFh)	**REG1003EF**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADD1[15:8]	7:0	See description of '1003EEh'.	
78h (1003F0h)	**REG1003F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDRAM_BOOT	7	SDRAM code access bit. This will force 32BMCU to access program SDAM when set.	
	SPI_BOOT	6	SPI FLASH code access bit. This will force 32BMCU to access program from SPI FLASH when set.	
	MHG2MI_WPRIORITY	5	32BMCU to miu write priority setting.	

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32BIT_MCU Register (Bank = 1003)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MHG2MI_RPRIORITY	4	32BMCU to miu read priority setting.	
	DWB_SWAP	3	Data bus bridge endian switch. Default is 1'b0, set 1'b1 to reverse the endian.	
	IWB_SWAP	2	Instruction bus bridge endian switch. Default is 1'b0, set 1'b1 to reverse the endian.	
	SW_RSTZ	1	32BMCU local software reset, default is 1, (i.e. Not in reset mode).	
	MHEG_ENABLE	0	Enable 32BMCU cpu, when MHEG is co-processor.	
79h (1003F2h)	**REG1003F2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_SEL[7:0]	7:0	Mheg debugger select register. When [15:8] == 0xdb, debugger mode will be on.	
79h (1003F3h)	**REG1003F3**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_SEL[15:8]	7:0	See description of '1003F2h'.	
7Ah (1003F4h)	**REG1003F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE0[7:0]	7:0	32BMCU SDR base address [15:0].	
7Ah (1003F5h)	**REG1003F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE0[15:8]	7:0	See description of '1003F4h'.	
7Bh (1003F6h)	**REG1003F6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE1[7:0]	7:0	32BMCU SDR base address [23:16]. . {REG16_MHG_SDR_BASE1[7:0], REG16_MHG_SDR_BASE0} [23:0]. Mheg dram base address register. Let CPU's internal memory access address be CPU_ADDR_IN[31:0]. Let CPU's address to MIU be CPU_ADDR[31:0]. CPU_ADDR[31:0] will be. {CPU_A.	
7Ch (1003F8h)	**REG1003F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	REG32_BASE[7:0]	7:0	Register base address, mapped into addr[31:16]. . REG16_MHG_REG32_BASE [15:0]. 32BMCU RIU register access base register. Must be 0xA000 to access RIU.	
7Ch (1003F9h)	**REG1003F9**	**7:0**	**Default : 0xA0**	**Access : R/W**
	REG32_BASE[15:8]	7:0	See description of '1003F8h'.	

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32BIT_MCU Register (Bank = 1003)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Dh (1003FAh)	**REG1003FA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP0[7:0]	7:0	32BMCU SDR address mapping mask [15:0].	
7Dh (1003FBh)	**REG1003FB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP0[15:8]	7:0	See description of '1003FAh'.	
7Eh (1003FCh)	**REG1003FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP1[7:0]	7:0	32BMCU SDR address mapping mask [31:16]. . {REG16_MHG_SDR_MAP1, REG16_MHG_SDR_MAP0} [31:0]. Mheg sdram range mask address registers, when in BOOT_32BMCU mode. Only for Intruction access. Deault is 0xfff0_0000. [1Mbyte]. That is the addresses between 0 ~ 0x000F_FFFF.	
7Eh (1003FDh)	**REG1003FD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP1[15:8]	7:0	See description of '1003FCh'.	
7Fh (1003FEh)	**REG1003FE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_BASE[7:0]	7:0	32BMCU SPI base address. . REG16_MHG_SPI_BASE [15:0]. Mheg spi bank address register. {only data accesses will be constrained by this rule}. usage: When cpu's addr[31:15] == REG16_MHG_SPI_BASE[15:0], The memory access cycles will be directed to SPI Flash.	
7Fh (1003FFh)	**REG1003FF**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_BASE[15:8]	7:0	See description of '1003FEh'.	

CMDQ Register (Bank = 1004)

CMDQ Register (Bank = 1004)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (100402h)	**REG100402**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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CMDQ Register (Bank = 1004)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CMDQ_EN	0	Enable cmdq DMA read enable.	
02h (100404h)	**REG100404**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CMD_BUF_MODE	1	0: Direct, 1: increament.	
	DMA_TRIG_EN	0	Cmdq trig mode enalbe.	
03h (100406h)	**REG100406**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:3	Reserved.	
	RST_CMD_ST_PTR_TRIG	2	Trig for reset start pointer (increase mode).	
	MOV_CMD_PTR	1	Trig for update command end pointer.	
	DMA_TRIG	0	DMA trig when using trig mode.	
04h (100408h)	**REG100408**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CMD_ST_PTR[7:0]	7:0	Command buffer start pointer.	
04h (100409h)	**REG100409**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CMD_ST_PTR[15:8]	7:0	See description of '100408h'.	
05h (10040Ah)	**REG10040A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_ST_PTR[23:16]	7:0	See description of '100408h'.	
05h (10040Bh)	**REG10040B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_ST_PTR[31:24]	7:0	See description of '100408h'.	
06h (10040Ch)	**REG10040C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_END_PTR[7:0]	7:0	Command buffer end pointer.	
06h (10040Dh)	**REG10040D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_END_PTR[15:8]	7:0	See description of '10040Ch'.	
07h (10040Eh)	**REG10040E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_END_PTR[23:16]	7:0	See description of '10040Ch'.	
07h (10040Fh)	**REG10040F**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_END_PTR[31:24]	7:0	See description of '10040Ch'.	
10h (100420h)	**REG100420**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	REQ_MIU_SEL	1	Select miu.	
	REQ_PRI	0	Assert high priority for request.	
10h (100421h)	**REG100421**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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CMDQ Register (Bank = 1004)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MIU_READ_MODE	3	MIU data read mode. #h0: 128 bit. #h1: 64 bit.	
	-	2:0	Reserved.	
11h (100422h)	**REG100422**	**7:0**	**Default : 0x00**	**Access : R/W**
	REQ_LEN[7:0]	7:0	Length per request burst.	
11h (100423h)	**REG100423**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMA_BURST_MODE	4	Burst mode.	
	-	3:0	Reserved.	
12h (100424h)	**REG100424**	**7:0**	**Default : 0x20**	**Access : R/W**
	REQ_TH[7:0]	7:0	Threshold to request.	
20h (100440h)	**REG100440**	**7:0**	**Default : 0xFF**	**Access : R/W**
	INV_XIU_WMASK	7	1: ~cmdq2xarb_wmask.	
	WR_CMD_DIRECT_W	6	For write command, use riu write mask function.	
	CMDQ_RIU_BE[3:0]	5:2	Byte enable to riu_bridge.	
	CMDQ_RIU_RE	1	Riu_bridge read enable.	
	CMDQ_RIU_WE	0	Riu_bridge write enable.	
21h (100442h)	**REG100442**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_TRIG_MASK[7:0]	7:0	1: Input trig mask for wait commad.	
21h (100443h)	**REG100443**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_TRIG_MASK[15:8]	7:0	See description of '100442h'.	
22h (100444h)	**REG100444**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_TRIG_FORCE[7:0]	7:0	1: Input trig force high for wait commad.	
22h (100445h)	**REG100445**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_TRIG_FORCE[15:8]	7:0	See description of '100444h'.	
23h (100446h)	**REG100446**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CAP_WAIT_TRIG	1	1: Capture wait trigger signal.	
	SKIP_WAIT_TRIG_MASK	0	1: Skip wait trigger mask bit.	
24h (100448h)	**REG100448**	**7:0**	**Default : 0x00**	**Access : R/W**
	SKIP_POLL1_MASK	7	1: Skip polling 1 command mask(non-equivalent).	
	SKIP_POLL0_MASK	6	1: Skip polling 0 command mask(equivalent).	

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CMDQ Register (Bank = 1004)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SKIP_WAIT_MASK	5	1: Skip wait command mask.	
	SKIP_WR_MASK	4	1: Skip write command mask.	
	SKIP_POLL1_CMD	3	1: Skip polling1 command(non-equivalent).	
	SKIP_POLL0_CMD	2	1: Skip polling 0 command(equivalent).	
	SKIP_WAIT_CMD	1	1: Skip wait command.	
	SKIP_WR_CMD	0	1: Skip write command.	
24h (100449h)	**REG100449**	**7:0**	**Default : 0x00**	**Access : R/W**
	FORCE_POLL_HIT	7	1: Force polling success.	
	FORCE_POLL_MISS	6	1: Force polling fail.	
	-	5:4	Reserved.	
	FORCE_POLL1_MASK	3	1: Force polling 1 command mask(non-equivalent).	
	FORCE_POLL0_MASK	2	1: Force polling 0 command mask(equivalent).	
	FORCE_WAIT_MASK	1	1: Force wait command mask.	
	FORCE_WR_MASK	0	1: Force write command mask.	
25h (10044Ah)	**REG10044A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_WATCH_CMD	1	Force stop to watch command.	
	FORCE_WRITE_STOP	0	Force write command stop.	
2Ah (100454h)	**REG100454**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	XARB_RW_NO_TRIG	5	While sm0_st is at read/write state, ignore one step function.	
	CMD_REPLACE_EN	4	Replace command enable.	
	CMD_SEARCH_EN	3	Search command enable.	
	ONE_STEP_EN[1:0]	2:1	Step by step enable, [0]: normal mode one step, [1]: debug mode one step.	
	CMD_DEBUG_EN	0	Debug mode enable.	
2Bh (100456h)	**REG100456**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CMD_REPLACE_SEL[3:0]	7:4	Replace command byte enable.	
	CMD_SEARCH_SEL[3:0]	3:0	Search command byte enable.	
2Ch (100458h)	**REG100458**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	ONE_STEP_TRIG	0	One step trigger.	

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CMDQ Register (Bank = 1004)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Dh (10045Ah)	**REG10045A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_REPLACE_DAT1[7:0]	7:0	Replace/compare cmd of sec. 1.	
2Dh (10045Bh)	**REG10045B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_REPLACE_DAT1[15:8]	7:0	See description of '10045Ah'.	
2Eh (10045Ch)	**REG10045C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_REPLACE_DAT2[7:0]	7:0	Replace/compare cmd of sec. 2.	
2Eh (10045Dh)	**REG10045D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_REPLACE_DAT2[15:8]	7:0	See description of '10045Ch'.	
2Fh (10045Eh)	**REG10045E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_REPLACE_DAT3[7:0]	7:0	Replace/compare cmd of sec. 3.	
2Fh (10045Fh)	**REG10045F**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_REPLACE_DAT3[15:8]	7:0	See description of '10045Eh'.	
30h (100460h)	**REG100460**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EN_CLK_MIU	0	Enable local clk_miu.	
30h (100461h)	**REG100461**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	SRAM_GATE_EN	4	Enable sram clock gating when no CE.	
	-	3:1	Reserved.	
	EN_CLK_XIU	0	Enable local clk_xiu.	
31h (100462h)	**REG100462**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SOFT_RSTZ	0	Reset in xiu domain, active high.	
32h (100464h)	**REG100464**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DEBUG_SEL[1:0]	1:0	Debug out selection.	
40h (100480h)	**REG100480**	**7:0**	**Default : 0x00**	**Access : RO**
	RB_CMD[7:0]	7:0	Decode command read back.	
40h (100481h)	**REG100481**	**7:0**	**Default : 0x00**	**Access : RO**
	RB_CMD[15:8]	7:0	See description of '100480h'.	

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CMDQ Register (Bank = 1004)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (100482h)	**REG100482**	**7:0**	**Default : 0x00**	**Access : RO**
	RB_DMA_ST1[2:0]	7:5	Dma state1 read back.	
	RB_DMA_ST2[1:0]	4:3	Dma state2 read back.	
	-	2:0	Reserved.	
41h (100483h)	**REG100483**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	RB_DMA_ST0	1	Dma state0 read back.	
	RB_DMA_ST1[3]	0	See description of '100482h'.	
42h (100484h)	**REG100484**	**7:0**	**Default : 0x00**	**Access : RO**
	RB_DEC_ST0[2:0]	7:5	Decode state read back.	
	RB_DEC_ST1[2:0]	4:2	Decode state read back.	
	-	1:0	Reserved.	
42h (100485h)	**REG100485**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	RB_DEC_ST0[3]	0	See description of '100484h'.	
43h (100486h)	**REG100486**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RB_CMD_SEL[2:0]	2:0	Decode command read back selection.	
44h (100488h)	**REG100488**	**7:0**	**Default : 0x00**	**Access : RO**
	FINAL_IRQ[7:0]	7:0	[0]: Dma_trig, [1]: dma_done.	
45h (10048Ah)	**REG10048A**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_IRQ[7:0]	7:0	[0]: Dma_trig, [1]: dma_done.	
46h (10048Ch)	**REG10048C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[7:0]	7:0	Interrupt force.	
47h (10048Eh)	**REG10048E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_MASK[7:0]	7:0	Interrupt mask.	
48h (100490h)	**REG100490**	**7:0**	**Default : 0x00**	**Access : WO**
	IRQ_CLR[7:0]	7:0	Interrupt clear.	
49h (100492h)	**REG100492**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SW_TRIG_CAP_SEL	0	Sw trigger capture timing selection.	
4Ah (100494h)	**REG100494**	**7:0**	**Default : 0x00**	**Access : R/W**
	POLL_WAIT_TIME[7:0]	7:0	Period after sent next read request/just wait.	

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CMDQ Register (Bank = 1004)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Ah (100495h)	**REG100495**	**7:0**	**Default : 0x00**	**Access : R/W**
	POLL_WAIT_TIME[15:8]	7:0	See description of '100494h'.	
4Bh (100496h)	**REG100496**	**7:0**	**Default : 0x00**	**Access : R/W**
	POLL_TIMER_RATIO[7:0]	7:0	Poll timer ratio. Real poll wait time is reg_poll_wait_time * (POLL_TIMER_RATIO + 1).	
4Bh (100497h)	**REG100497**	**7:0**	**Default : 0x00**	**Access : RO**
	POLL_TIME_UP	7	Poll time up.	
	-	6:0	Reserved.	
4Ch (100498h)	**REG100498**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	RD_SRAM_EMPTY	1	Check if sram is empty.	
	CMD_PTR_VLD	0	Read if command pointer is valid.	
4Dh (10049Ah)	**REG10049A**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_MI_RADR[7:0]	7:0	Check read address position.	
4Dh (10049Bh)	**REG10049B**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_MI_RADR[15:8]	7:0	See description of '10049Ah'.	
4Eh (10049Ch)	**REG10049C**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_MI_RADR[23:16]	7:0	See description of '10049Ah'.	
4Eh (10049Dh)	**REG10049D**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_MI_RADR[31:24]	7:0	See description of '10049Ah'.	
78h (1004F0h)	**REG1004F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY[7:0]	7:0	DUMMY register.	
78h (1004F1h)	**REG1004F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY[15:8]	7:0	See description of '1004F0h'.	

POR_STATUS Register (Bank = 1005)

POR_STATUS Register (Bank = 1005)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (100500h)	**REG100500**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_0[7:0]	7:0	Power status0.	
00h	**REG100501**	**7:0**	**Default : 0x00**	**Access : R/W**

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POR_STATUS Register (Bank = 1005)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100501h)	POR_STATUS_0[15:8]	7:0	See description of '100500h'.	
01h (100502h)	**REG100502**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_1[7:0]	7:0	Power status1.	
01h (100503h)	**REG100503**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_1[15:8]	7:0	See description of '100502h'.	
02h (100504h)	**REG100504**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_2[7:0]	7:0	Power status2.	
02h (100505h)	**REG100505**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_2[15:8]	7:0	See description of '100504h'.	
03h (100506h)	**REG100506**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_3[7:0]	7:0	Power status3.	
03h (100507h)	**REG100507**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_3[15:8]	7:0	See description of '100506h'.	
04h (100508h)	**REG100508**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_4[7:0]	7:0	Power status4.	
04h (100509h)	**REG100509**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_4[15:8]	7:0	See description of '100508h'.	
05h (10050Ah)	**REG10050A**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_5[7:0]	7:0	Power status5.	
05h (10050Bh)	**REG10050B**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_5[15:8]	7:0	See description of '10050Ah'.	
06h (10050Ch)	**REG10050C**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_6[7:0]	7:0	Power status6.	
06h (10050Dh)	**REG10050D**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_6[15:8]	7:0	See description of '10050Ch'.	
07h (10050Eh)	**REG10050E**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_7[7:0]	7:0	Power status7.	
07h (10050Fh)	**REG10050F**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_7[15:8]	7:0	See description of '10050Eh'.	
08h (100510h)	**REG100510**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_8[7:0]	7:0	Power status8.	
08h (100511h)	**REG100511**	**7:0**	**Default : 0x00**	**Access : R / W**
	POR_STATUS_8[15:8]	7:0	See description of '100510h'.	

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POR_STATUS Register (Bank = 1005)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
09h (100512h)	**REG100512**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_9[7:0]	7:0	Power status9.	
09h (100513h)	**REG100513**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_9[15:8]	7:0	See description of '100512h'.	
0Ah (100514h)	**REG100514**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_A[7:0]	7:0	Power statusa.	
0Ah (100515h)	**REG100515**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_A[15:8]	7:0	See description of '100514h'.	
0Bh (100516h)	**REG100516**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_B[7:0]	7:0	Power statusb.	
0Bh (100517h)	**REG100517**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_B[15:8]	7:0	See description of '100516h'.	
0Ch (100518h)	**REG100518**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_C[7:0]	7:0	Power statusc.	
0Ch (100519h)	**REG100519**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_C[15:8]	7:0	See description of '100518h'.	
0Dh (10051Ah)	**REG10051A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_D[7:0]	7:0	Power statusd.	
0Dh (10051Bh)	**REG10051B**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_D[15:8]	7:0	See description of '10051Ah'.	
0Eh (10051Ch)	**REG10051C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_E[7:0]	7:0	Power statuse.	
0Eh (10051Dh)	**REG10051D**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_E[15:8]	7:0	See description of '10051Ch'.	
0Fh (10051Eh)	**REG10051E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_F[7:0]	7:0	Power statusf.	
0Fh (10051Fh)	**REG10051F**	**7:0**	**Default : 0x00**	**Access : R/W**
	POR_STATUS_F[15:8]	7:0	See description of '10051Eh'.	

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INTR_CPUINT Register (Bank = 1005)

INTR_CPUINT Register (Bank = 1005)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (100540h)	**REG100540**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST0TO3_INT	2	Host0 to host3 interrupt.	
	HST0TO2_INT	1	Host0 to host2 interrupt.	
	HST0TO1_INT	0	Host0 to host1 interrupt.	
22h (100544h)	**REG100544**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST1TO3_INT	2	Host1 to host3 interrupt.	
	HST1TO2_INT	1	Host1 to host2 interrupt.	
	HST1TO0_INT	0	Host1 to host0 interrupt.	
24h (100548h)	**REG100548**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST2TO3_INT	2	Host2 to host3 interrupt.	
	HST2TO1_INT	1	Host2 to host1 interrupt.	
	HST2TO0_INT	0	Host2 to host0 interrupt.	
26h (10054Ch)	**REG10054C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST3TO2_INT	2	Host3 to host2 interrupt.	
	HST3TO1_INT	1	Host3 to host1 interrupt.	
	HST3TO0_INT	0	Host3 to host0 interrupt.	
28h (100550h)	**REG100550**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host0 fiq final status[7:0]). Bit1 => OR (host0 fiq final status[15:8]). ..... Bit7 => OR (host0 fiq final status[63:56]).	
28h (100551h)	**REG100551**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host0 irq final status[7:0]). Bit1 => OR (host0 irq final status[15:8]). ..... Bit7 => OR (host0 irq final status[63:56]).	
29h	**REG100552**	**7:0**	**Default : 0x00**	**Access : RO**

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INTR_CPUINT Register (Bank = 1005)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100552h)	HST1_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host1 fiq final status[7:0]). Bit1 => OR (host1 fiq final status[15:8]). ..... Bit7 => OR (host1 fiq final status[63:56]).	
29h (100553h)	**REG100553**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host1 irq final status[7:0]). Bit1 => OR (host1 irq final status[15:8]). ..... Bit7 => OR (host1 irq final status[63:56]).	
2Ah (100554h)	**REG100554**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host2 fiq final status[7:0]). Bit1 => OR (host2 fiq final status[15:8]). ..... Bit7 => OR (host2 fiq final status[63:56]).	
2Ah (100555h)	**REG100555**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host2 irq final status[7:0]). Bit1 => OR (host2 irq final status[15:8]). ..... Bit7 => OR (host2 irq final status[63:56]).	
2Bh (100556h)	**REG100556**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host3 fiq final status[7:0]). Bit1 => OR (host3 fiq final status[15:8]). ..... Bit7 => OR (host3 fiq final status[63:56]).	
2Bh (100557h)	**REG100557**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host3 irq final status[7:0]). Bit1 => OR (host3 irq final status[15:8]). ..... Bit7 => OR (host3 irq final status[63:56]).	

USBC 0 (Single Port) Register (Bank = 1007)

USBC 0 Register (Bank = 1007)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**RST_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**

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USBC 0 Register (Bank = 1007)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100700h)	-	7	Reserved	
	OTG_XIU_ENABLE	6	The OTG XIU read and write operation are invalid if the bit is set to 1'b0.	
	UHC_XIU_ENABLE	5	The UHC XIU read and write operation are invalid if the bit is set to 1'b0.	
	-	4	Reserved for port1 in dual port design.	
	REG_SUSPEND_	3	Initial suspend control	
	OTG_RST	2	Write 1 to reset OTG controller.	
	UHC_RST	1	Write 1 to reset UHC controller.	
	USB_RST	0	Write 1 to reset USB controller.	
00h (100701h)	**-**	**7:0**	**Default : 0x02**	**Access : R/W**
		7:4	Reserved	
		3:2	Reserved for port1 in dual port design.	
	REG_VBUSVALID	1	Override vbusvalid value for port 0.	
	VBUS_SEL	0	The select option for vbusvalid in port 0. Default value is select to register value.	
01h (100702h)	**PORT_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	HSIC_EN	5	UTMI select 0: Normal UTMI 1: HSIC UTMI (UIC)	
	IDPULLUP_CTRL	4	OTG idpullup control.	
	PME_POL	3	Power management event polarity select	
	INT_POL	2	Interrupt polarity select	
	PORT_CTRL	1:0	2'b00: UHC and OTG are both disable 2'b01: UHC enable 2'b10: OTG enable 2'b11: the setting is prohibited	
02h (100704h)	**INTERRUPT_ENABLE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ID_CHG_INTEN	3	The interrupt enable of status: ID state changed.	
	BVAL_CHG_INTEN	2	The interrupt enable of status: BVALID state changed.	
	AVAL_CHG_INTEN	1	The interrupt enable of status: AVALID state changed.	
	VBUS_CHG_INTEN	0	The interrupt enable of status: VBUSVALID state	

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USBC 0 Register (Bank = 1007)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			changed.	
03h (100706h)	**INTERRUPT_STATUS1**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	-	7:4	Reserved.	
	ID_CHG_STS	3	The interrupt status: ID state changed.	
	BVAL_CHG_STS	2	The interrupt status: BVALID state changed.	
	AVAL_CHG_STS	1	The interrupt status: AVALID state changed.	
	VBUS_CHG_STS	0	The interrupt status: VBUSVALID state changed.	
04h (100708h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	LINESTATE[1:0]	7:6	DM and DP single status.	
	SESSEND	5	UTMI status.	
	HOSTDISCON	4	Device disconnect in high speed mode.	
	IDDIG	3	PAD CID status.	
	BVALID	2	The status of Power detector.	
	AVALID	1	The status of Power detector.	
	VBUSVALID	0	The status of Power detector.	
04h (100709h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	ID_DEB_CNT[2:0]	7:5	PAD CID debouncing counter	
	RXACTIVE	4	UTMI data interface.	
	RXVALID	3	UTMI data interface.	
	RXVALIDH	2	UTMI data interface.	
	RXERROR	1	UTMI data interface.	
	TXREADY	0	UTMI data interface.	
05h (10070Ah)	**Power Management Event Enable**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	11	Reserved	
	NEW_PV2MI_RD_SEL	10	Read burst size of new pv2mi bridge 2'b00=8 2'b01=16 2'b10=32 2'b11=64	
	NEW_PV2MI_WRT_SEL	9	Write burst size of new pv2mi bridge 2'b00=4 2'b01=8 2'b10=16	

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USBC 0 Register (Bank = 1007)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2'b11=32	
	UHC_DBUS_MASK	7	To mask uhc debug bus.	
	CONN_BVAL_INTEN	6	The interrupt and PME enable CONN_BVAL_STS.	
	CONN_AVAL_INTEN	5	The interrupt and PME enable CONN_AVAL_STS.	
	CONN_VBUS_INTEN	4	The interrupt and PME enable CONN_VBUS_STS.	
	RESET_INTEN	3	The interrupt and PME enable RESET_STS.	
	RESUME_INTEN	2	The interrupt and PME enable RESUME_STS.	
	DEV_DET_INTEN	1	The interrupt and PME enable DEV_DET_STS.	
	WAKEUP_INTEN	0	The interrupt and PME enable WAKEUP_STS.	
06h (10070Ch)	**Power Management Event Status**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	-	7	Reserved.	
	CONN_BVAL_STS	6	OTG detect bvalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_AVAL_STS	5	OTG detect avalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_VBUS_STS	4	OTG detect PAD_VBUS rising in the suspend mode. The status will both result interrupt and PME.	
	RESET_STS	3	OTG detect host send USB bus reset in suspend mode. The status will both result interrupt and PME.	
	RESUME_STS	2	OTG detect host send USB bus resume signaling in suspend mode. The status will both result interrupt and PME.	
	DEV_DET_STS	1	UHC detect device plug-in in suspend mode. The status will both result interrupt and PME.	
	WAKEUP_STS	0	UHC detect device remote wakeup in suspend mode. The status will both result interrupt and PME.	
07h (10070Eh)	**uh2mi_adr_mask**	**7:0**	**Default : 0x00**	**Access : R/W**
	uh2mi_adr_mask	7:0	8 bit miu address mask for uh2mi_addr[29:22]	
07h (10070Fh)	**uh2mi_adr_ctrl**	**7:0**	**Default : 0x00**	**Access : R/W**
	Override mode value	2	Uh2mi_miu1_sel value when override mode is enabled	
	Override mode enable	1	uh2mi_miu1_sel override mode enable	
	Bit-wised mode enable	0	Bit-wised mode enable for uh2mi_adr[29:22]	

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USBC 1 (Single Port) Register (Bank = 1007)

USBC 1 Register (Bank = 1007)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (100780h)	**RST_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved	
	OTG_XIU_ENABLE	6	The OTG XIU read and write operation are invalid if the bit is set to 1'b0.	
	UHC_XIU_ENABLE	5	The UHC XIU read and write operation are invalid if the bit is set to 1'b0.	
	-	4	Reserved for port1 in dual port design.	
	REG_SUSPEND_	3	Initial suspend control	
	OTG_RST	2	Write 1 to reset OTG controller.	
	UHC_RST	1	Write 1 to reset UHC controller.	
	USB_RST	0	Write 1 to reset USB controller.	
40h (100781h)	**-**	**7:0**	**Default : 0x02**	**Access : R/W**
		7:4	Reserved	
		3:2	Reserved for port1 in dual port design.	
	REG_VBUSVALID	1	Override vbusvalid value for port 0.	
	VBUS_SEL	0	The select option for vbusvalid in port 0. Default value is select to register value.	
41h (100782h)	**PORT_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	HSIC_EN	5	UTMI select 0: Normal UTMI 1: HSIC UTMI (UIC)	
	IDPULLUP_CTRL	4	OTG idpullup control.	
	PME_POL	3	Power management event polarity select	
	INT_POL	2	Interrupt polarity select	
	PORT_CTRL	1:0	2'b00: UHC and OTG are both disable 2'b01: UHC enable 2'b10: OTG enable 2'b11: the setting is prohibited	
42h (100784h)	**INTERRUPT_ENABLE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ID_CHG_INTEN	3	The interrupt enable of status: ID state changed.	
	BVAL_CHG_INTEN	2	The interrupt enable of status: BVALID state changed.	

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USBC 1 Register (Bank = 1007)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AVAL_CHG_INTEN	1	The interrupt enable of status: AVALID state changed.	
	VBUS_CHG_INTEN	0	The interrupt enable of status: VBUSVALID state changed.	
43h (100786h)	**INTERRUPT_STATUS1**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	-	7:4	Reserved.	
	ID_CHG_STS	3	The interrupt status: ID state changed.	
	BVAL_CHG_STS	2	The interrupt status: BVALID state changed.	
	AVAL_CHG_STS	1	The interrupt status: AVALID state changed.	
	VBUS_CHG_STS	0	The interrupt status: VBUSVALID state changed.	
44h (100788h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	LINESTATE[1:0]	7:6	DM and DP single status.	
	SESSEND	5	UTMI status.	
	HOSTDISCON	4	Device disconnect in high speed mode.	
	IDDIG	3	PAD CID status.	
	BVALID	2	The status of Power detector.	
	AVALID	1	The status of Power detector.	
	VBUSVALID	0	The status of Power detector.	
44h (100789h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	ID_DEB_CNT[2:0]	7:5	PAD CID debouncing counter	
	RXACTIVE	4	UTMI data interface.	
	RXVALID	3	UTMI data interface.	
	RXVALIDH	2	UTMI data interface.	
	RXERROR	1	UTMI data interface.	
	TXREADY	0	UTMI data interface.	
45h (10078Ah)	**Power Management Event Enable**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	11	Reserved	
	NEW_PV2MI_RD_SEL	10	Read burst size of new pv2mi bridge 2'b00=8 2'b01=16 2'b10=32 2'b11=64	
	NEW_PV2MI_WRT_SEL	9	Write burst size of new pv2mi bridge 2'b00=4	

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USBC 1 Register (Bank = 1007)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2'b01=8 2'b10=16 2'b11=32	
	UHC_DBUS_MASK	7	To mask uhc debug bus.	
	CONN_BVAL_INTEN	6	The interrupt and PME enable CONN_BVAL_STS.	
	CONN_AVAL_INTEN	5	The interrupt and PME enable CONN_AVAL_STS.	
	CONN_VBUS_INTEN	4	The interrupt and PME enable CONN_VBUS_STS.	
	RESET_INTEN	3	The interrupt and PME enable RESET_STS.	
	RESUME_INTEN	2	The interrupt and PME enable RESUME_STS.	
	DEV_DET_INTEN	1	The interrupt and PME enable DEV_DET_STS.	
	WAKEUP_INTEN	0	The interrupt and PME enable WAKEUP_STS.	
46h (10078Ch)	**Power Management Event Status**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	-	7	Reserved.	
	CONN_BVAL_STS	6	OTG detect bvalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_AVAL_STS	5	OTG detect avalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_VBUS_STS	4	OTG detect PAD_VBUS rising in the suspend mode. The status will both result interrupt and PME.	
	RESET_STS	3	OTG detect host send USB bus reset in suspend mode. The status will both result interrupt and PME.	
	RESUME_STS	2	OTG detect host send USB bus resume signaling in suspend mode. The status will both result interrupt and PME.	
	DEV_DET_STS	1	UHC detect device plug-in in suspend mode. The status will both result interrupt and PME.	
	WAKEUP_STS	0	UHC detect device remote wakeup in suspend mode. The status will both result interrupt and PME.	
47h (10078Eh)	**uh2mi_adr_mask**	**7:0**	**Default : 0x00**	**Access : R/W**
	uh2mi_adr_mask	7:0	8 bit miu address mask for uh2mi_addr[29:22]	
47h (10078Fh)	**uh2mi_adr_ctrl**	**7:0**	**Default : 0x00**	**Access : R/W**
	Override mode value	2	Uh2mi_miu1_sel value when override mode is enabled	
	Override mode enable	1	uh2mi_miu1_sel override mode enable	
	Bit-wised mode enable	0	Bit-wised mode enable for uh2mi_adr[29:22]	

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BDMA Register (Bank = 1009)

BDMA Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (100900h)	**REG100900**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CH0_TRIG	0	Write 1 to trigger DMA engine; no need to clear it.	
01h (100902h)	**REG100902**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:5	Reserved.	
	CH0_RESULT0	4	Report MISC-device status. Read: Asserted when find matched pattern with reg_dst_sel = 0x2. "cleared" by write 1 to "CH0_RESULT0" or "reg_ch0_trig". Write: Write 1 to clear this bit.	
	CH0_DONE	3	Read: Asserted after DMA done. "cleared" by write 1 to "CH0_DONE" or "reg_ch0_trig". Write: Write 1 to clear this bit.	
	CH0_INT_BDMA	2	Read: Asserted after DMA interrupt cours. "cleared" by write 1 to "CH0_INT_BDMA" or "reg_ch0_trig". Write: Write 1 to clear this bit.	
	CH0_BUSY	1	Assert when DMA engine is busy.	
	CH0_QUEUED	0	Assert when this cmd channel has been triggered and not DMA-done.	
02h (100904h)	**REG100904**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CH0_SRC_DW[2:0]	6:4	Source device data width. 0 => 1 byte; 1=> 2 bytes; 2 => 4 bytes; 3 => 8 bytes; 4 => 16 bytes.	

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BDMA Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CH0_SRC_SEL[3:0]	3:0	Select source device; 0: MIU channel0 (16 bytes). 1: MIU channel1 (16 bytes). 2: N/A. 3: N/A. 4: Memory fill (optional) (1 byte, 2 bytes or 4 bytes). 5: SPI (16 byte). 6: N/A. 7. N/A. 8. N/A. 9. N/A. 10. N/A.	
02h (100905h)	**REG100905**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CH0_DST_DW[2:0]	6:4	Destination device data width. 0 => 1 byte; 1=> 2 bytes; 2 => 4 bytes; 3 => 8 bytes; 4 => 16 bytes.	
	CH0_DST_SEL[3:0]	3:0	Select destination device; 0: MIU channel0 (16 bytes). 1: MIU channel1 (16 bytes). 2: Pattern search (optional) (1 byte). 3: CRC32 (optional) (1 byte). 4: N/A. 5: N/A. 6: VDMCU (1 byte). 7. DMDMCU (1 byte). 8. DSP (1 byte). 9. N/A. 10. HKMCU (1 byte).	
03h (100906h)	**REG100906**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CFG[3:0]	7:4	Configuration for misc device. CRC32: 0x1: Reflect data-in. Pattern Search: Bit[0] = 1: find anti-match. Bit[1] = 1: turn on MOBF.	
	-	3:2	Reserved.	
	CH0_INT_EN	1	Enable interrupt.	

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BDMA Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CH0_DEC	0	Address direction; 0/1; increase/decrease.	
04h (100908h)	**REG100908**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SRC_A[7:0]	7:0	Source device begin address.	
04h (100909h)	**REG100909**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SRC_A[15:8]	7:0	See description of '100908h'.	
05h (10090Ah)	**REG10090A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SRC_A[23:16]	7:0	See description of '100908h'.	
05h (10090Bh)	**REG10090B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SRC_A[31:24]	7:0	See description of '100908h'.	
06h (10090Ch)	**REG10090C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_DST_A[7:0]	7:0	Destination device begin address.	
06h (10090Dh)	**REG10090D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_DST_A[15:8]	7:0	See description of '10090Ch'.	
07h (10090Eh)	**REG10090E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_DST_A[23:16]	7:0	See description of '10090Ch'.	
07h (10090Fh)	**REG10090F**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_DST_A[31:24]	7:0	See description of '10090Ch'.	
08h (100910h)	**REG100910**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SIZE[7:0]	7:0	Size (byte).	
08h (100911h)	**REG100911**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SIZE[15:8]	7:0	See description of '100910h'.	
09h (100912h)	**REG100912**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SIZE[23:16]	7:0	See description of '100910h'.	
09h (100913h)	**REG100913**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_SIZE[31:24]	7:0	See description of '100910h'.	
0Ah (100914h)	**REG100914**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CMD0[7:0]	7:0	Special cmd0. 1. Pattern for pattern search. 2. Polynomial for CRC32. 3. Pattern for memory fill.	
0Ah	**REG100915**	**7:0**	**Default : 0x00**	**Access : R/W**

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BDMA Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100915h)	CH0_CMD0[15:8]	7:0	See description of '100914h'.	
0Bh (100916h)	**REG100916**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CMD0[23:16]	7:0	See description of '100914h'.	
0Bh (100917h)	**REG100917**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CMD0[31:24]	7:0	See description of '100914h'.	
0Ch (100918h)	**REG100918**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CMD1[7:0]	7:0	Special cmd1. 1. Exclude bit for pattern search. 2. Seed value for CRC32.	
0Ch (100919h)	**REG100919**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CMD1[15:8]	7:0	See description of '100918h'.	
0Dh (10091Ah)	**REG10091A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CMD1[23:16]	7:0	See description of '100918h'.	
0Dh (10091Bh)	**REG10091B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH0_CMD1[31:24]	7:0	See description of '100918h'.	
10h (100920h)	**REG100920**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	-	7:1	Reserved.	
	CH1_TRIG	0	Write 1 to trigger DMA engine; no need to clear it.	
11h (100922h)	**REG100922**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:5	Reserved.	
	CH1_RESULT0	4	Report MISC-device status. Read: Asserted when find matched pattern with reg_dst_sel = 0x2. "cleared" by write 1 to "CH1_RESULT0" or "reg_ch1_trig". Write: Write 1 to clear this bit.	
	CH1_DONE	3	Read: Asserted after DMA done. "cleared" by write 1 to "CH1_DONE" or "reg_ch1_trig". Write: Write 1 to clear this bit.	
	CH1_INT_BDMA	2	Read: Asserted after DMA interrupt cours. "cleared" by write 1 to "CH1_INT_BDMA" or "reg_ch1_trig". Write: Write 1 to clear this bit.	
	CH1_BUSY	1	Assert when DMA engine is busy.	

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BDMA Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CH1_QUEUED	0	Assert when this cmd channel has been triggered and not DMA-done.	
12h (100924h)	**REG100924**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CH1_SRC_DW[2:0]	6:4	Source device data width. 0 => 1 byte; 1=> 2 bytes; 2 => 4 bytes; 3 => 8 bytes; 4 => 16 bytes.	
	CH1_SRC_SEL[3:0]	3:0	Select source device; 0: MIU channel0 (16 bytes). 1: MIU channel1 (16 bytes). 2: N/A. 3: N/A. 4: Memory fill (optional) (1 byte, 2 bytes or 4 bytes). 5: SPI (16 byte). 6: N/A. 7. N/A. 8. N/A. 9. N/A. 10. N/A.	
12h (100925h)	**REG100925**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CH1_DST_DW[2:0]	6:4	Destination device data width. 0 => 1 byte; 1=> 2 bytes; 2 => 4 bytes; 3 => 8 bytes; 4 => 16 bytes.	
	CH1_DST_SEL[3:0]	3:0	Select destination device; 0: MIU channel0 (16 bytes). 1: MIU channel1 (16 bytes). 2: Pattern search (optional) (1 byte). 3: CRC32 (optional) (1 byte). 4: N/A. 5: N/A. 6: VDMCU (1 byte). 7. DMDMCU (1 byte). 8. DSP (1 byte). 9. N/A. 10. HKMCU (1 byte).	
13h	**REG100926**	**7:0**	**Default : 0x00**	**Access : R/W**

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BDMA Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100926h)	CH1_CFG[3:0]	7:4	Configuration for misc device. CRC32: 0x1: Reflect data-in. Pattern Search: Bit[0] = 1: find anti-match. Bit[1] = 1: turn on MOBF.	
	-	3:2	Reserved.	
	CH1_INT_EN	1	Enable interrupt.	
	CH1_DEC	0	Address direction; 0/1; increase/decrease.	
14h (100928h)	**REG100928**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SRC_A[7:0]	7:0	Source device begin address.	
14h (100929h)	**REG100929**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SRC_A[15:8]	7:0	See description of '100928h'.	
15h (10092Ah)	**REG10092A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SRC_A[23:16]	7:0	See description of '100928h'.	
15h (10092Bh)	**REG10092B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SRC_A[31:24]	7:0	See description of '100928h'.	
16h (10092Ch)	**REG10092C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DST_A[7:0]	7:0	Destination device begin address.	
16h (10092Dh)	**REG10092D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DST_A[15:8]	7:0	See description of '10092Ch'.	
17h (10092Eh)	**REG10092E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DST_A[23:16]	7:0	See description of '10092Ch'.	
17h (10092Fh)	**REG10092F**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DST_A[31:24]	7:0	See description of '10092Ch'.	
18h (100930h)	**REG100930**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SIZE[7:0]	7:0	Size (byte).	
18h (100931h)	**REG100931**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SIZE[15:8]	7:0	See description of '100930h'.	
19h (100932h)	**REG100932**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SIZE[23:16]	7:0	See description of '100930h'.	
19h (100933h)	**REG100933**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_SIZE[31:24]	7:0	See description of '100930h'.	
1Ah	**REG100934**	**7:0**	**Default : 0x00**	**Access : R/W**

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BDMA Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100934h)	CH1_CMD0[7:0]	7:0	Special cmd0. 1. Pattern for pattern search. 2. Polynomial for CRC32. 3. Pattern for memory fill.	
1Ah	**REG100935**	**7:0**	**Default : 0x00**	**Access : R / W**
(100935h)	CH1_CMD0[15:8]	7:0	See description of '100934h'.	
1Bh	**REG100936**	**7:0**	**Default : 0x00**	**Access : R / W**
(100936h)	CH1_CMD0[23:16]	7:0	See description of '100934h'.	
1Bh	**REG100937**	**7:0**	**Default : 0x00**	**Access : R / W**
(100937h)	CH1_CMD0[31:24]	7:0	See description of '100934h'.	
1Ch	**REG100938**	**7:0**	**Default : 0x00**	**Access : R / W**
(100938h)	CH1_CMD1[7:0]	7:0	Special cmd1. 1. Exclude bit for pattern search. 2. Seed value for CRC32.	
1Ch	**REG100939**	**7:0**	**Default : 0x00**	**Access : R / W**
(100939h)	CH1_CMD1[15:8]	7:0	See description of '100938h'.	
1Dh	**REG10093A**	**7:0**	**Default : 0x00**	**Access : R / W**
(10093Ah)	CH1_CMD1[23:16]	7:0	See description of '100938h'.	
1Dh	**REG10093B**	**7:0**	**Default : 0x00**	**Access : R / W**
(10093Bh)	CH1_CMD1[31:24]	7:0	See description of '100938h'.	
1Eh	**REG10093C**	**7:0**	**Default : 0x00**	**Access : R / W**
(10093Ch)	CH1_CMD2[7:0]	7:0	Special cmd2. 1. MOBF key for pattern search;	
1Eh	**REG10093D**	**7:0**	**Default : 0x00**	**Access : R / W**
(10093Dh)	CH1_CMD2[15:8]	7:0	See description of '10093Ch'.	
1Fh	**REG10093E**	**7:0**	**Default : 0x00**	**Access : R / W**
(10093Eh)	CH1_CMD2[23:16]	7:0	See description of '10093Ch'.	
1Fh	**REG10093F**	**7:0**	**Default : 0x00**	**Access : R / W**
(10093Fh)	CH1_CMD2[31:24]	7:0	See description of '10093Ch'.	

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UART0 Register (Bank = 1009)

UART0 Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (100980h)	**REG100980**	**7:0**	**Default : 0x00**	**Access : R/W**
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; Note that Writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; Note that any incoming data are lost whenFIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
42h (100984h)	**REG100984**	**7:0**	**Default : 0x00**	**Access : R/W**
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Boud rate = (serial clock freq.) / (16 * divisor).	
44h	**REG100988**	**7:0**	**Default : 0x00**	**Access : R/W**

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UART0 Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100988h)	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00" - FIFO empty; "01" - 2 characters in the FIFO; "10" - FIFO 1/4 full; "11" - FIFO 1/2 full; Bit [7:6]: Receiver FIFO Interrupt trigger level. "00" - 1 character in the FIFO; "01" - FIFO 1/4 full; "10" - FIFO 1/2 full; "11" - FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt idenfy. "110" - character timeout. "011" - Receiver Line Status. "010" - Receiver Data Available. "001" - Transmitter Holding Register empty. "000" - Modem Status.	
46h (10098Ch)	**REG10098C**	**7:0**	**Default : 0x03**	**Access : R/W**
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.	
	-	6:5	Reserved.	
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.	
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.	
	LCR_STOP_BITS	2	Specify the number of stop bits. "0" - 1 stop bit; "1" - 1.5 stop bits when 5-bit character length selected and 2 bits otherwise.	
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00" - 5 bits; "01" - 6 bits; "10" - 7 bits; "11" - 8 bits.	
48h	**REG100990**	**7:0**	**Default : 0x00**	**Access : R/W**

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UART0 Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100990h)	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN. RTS-> CTS.	
	-	3:2	Reserved.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0" - RTS is "1"; "1" - RTS is "0".	
	-	0	Reserved.	
4Ah (100994h)	**REG100994**	**7:0**	**Default : 0x00**	**Access : RO**
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO;	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO; Gen a Transmitter Holding Register Empty interrupt.	
	-	4	Reserved.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
4Ch (100998h)	**REG100998**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	-	3:1	Reserved.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1" - the "CTS" line has changed its state. Clear when reading;	
4Eh	**REG10099C**	**7:0**	**Default : 0x00**	**Access : RO**

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UART0 Register (Bank = 1009)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10099Ch)	-	7:1	Reserved.	
	USR_BUSY	0	UART busy.	
54h (1009A8h)	**REG1009A8**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RSTZ	0	Software reset UART; 0: enable.	

CLKGEN0 Register (Bank = 100B)

CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (100B00h)	**REG100B00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_RIU	4	Reserved. 0: Clk_vd_p_temp. 1: Clk_dmplldiv10_div2.	
	-	3:0	Reserved.	
01h (100B02h)	**REG100B02**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_432_AU[1:0]	5:4	CLK_432_AU clock setting. 00: 216 MHz. 01: 432 MHz. 10: 240 MHz. 11: 480 MHz.	
	-	3	Reserved.	
	CKG_BIST[2:0]	2:0	CLK_BIST clock setting. 000: 216 MHz. 001: 172 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: 86 MHz. 110: 62 MHz. 111: Select XTAL.	
02h (100B04h)	**REG100B04**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EN_GPSPLLL_CLK_IN	5	CLK_GPSPLL clock enable. 0: Disable clock. 1: Enable clock.	
	EN_G3DPLLL_CLK_IN	4	CLK_G3DPLL clock enable. 0: Disable clock. 1: Enable clock.	
	EN_MIPSPLL_CLK_IN	3	CLK_MIPSPLL clock enable. 0: Disable clock. 1: Enable clock.	
	EN_MPLL_CLK_IN	2	CLK_MPLL clock enable. 0: Disable clock. 1: Enable clock.	
	CKG_BIST_MDTREE	1	CLK_BIST clock gated. 0: Disable gated clock. 1: Enable gated clock.	
	-	0	Reserved.	
02h (100B05h)	**REG100B05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SRAM2P_TEST_SEL[2:0]	6:4	Reserved.	
	-	3	Reserved.	
	CKG_EXT_CLKO[2:0]	2:0	CLK_EXT_CLKO clock setting. 000: Reserved. 001: 12 MHz. 010: 24 MHz. 011: 27 MHz. 100: 32 MHz. 101: 36 MHz. 110: 48 MHz. 111: Clock synth USB.	
04h (100B08h)	**REG100B08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STC0_REF_DIV2_EN	3	Enable Reference DIV2 for STC0.	
	UPDATE_STC0_CW	2	Update control word of the synthesizer STC0.	
	STC0_CW_SEL	1	Select from which STC0 word is controlled. 0: Register controlled by House Keeping MCU. 1: Register controlled by TSP.	
	STC0SYN_RST	0	STC0 synthesizer software reset, active high.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (100B09h)	**REG100B09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STC1_REF_DIV2_EN	3	Enable Reference DIV2 for STC1.	
	UPDATE_STC1_CW	2	Update control word of the synthesizer STC1.	
	STC1_CW_SEL	1	Select from which STC1 word is controlled. 0: Register controlled by House Keeping MCU. 1: Register controlled by TSP.	
	STC1SYN_RST	0	STC1 synthesizer software reset, active high.	
05h (100B0Ah)	**REG100B0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[7:0]	7:0	Control word of the synthesizer of STC0 clocks.	
05h (100B0Bh)	**REG100B0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[15:8]	7:0	See description of '100B0Ah'.	
06h (100B0Ch)	**REG100B0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[23:16]	7:0	See description of '100B0Ah'.	
06h (100B0Dh)	**REG100B0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[31:24]	7:0	See description of '100B0Ah'.	
07h (100B0Eh)	**REG100B0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC1SYN_CW[7:0]	7:0	Control word of the synthesizer of STC1 clocks.	
07h (100B0Fh)	**REG100B0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC1SYN_CW[15:8]	7:0	See description of '100B0Eh'.	
08h (100B10h)	**REG100B10**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC1SYN_CW[23:16]	7:0	See description of '100B0Eh'.	
08h (100B11h)	**REG100B11**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC1SYN_CW[31:24]	7:0	See description of '100B0Eh'.	
0Bh (100B16h)	**REG100B16**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_TIMER_TOP_1[3:0]	7:4	CLK_TIMER1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: 000: 24MHz. 001: 32KMHz. 010: 128Mz. 011: Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_TIMER_TOP_0[3:0]	3:0	CLK_TIMER0 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: 000: 24MHz. 001: 32KMHz. 010: 128Mz. 011: Reserved.	
0Ch (100B18h)	**REG100B18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_SAR_ADC[1:0]	1:0	CLK_SAR_ADC clock setting. [0]: Disable clock. [1]: Invert clock.	
0Dh (100B1Ah)	**REG100B1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	USBSYN_RST	0	USB synthesizer software reset, active high.	
0Eh (100B1Ch)	**REG100B1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[7:0]	7:0	Control word of the synthesizer for USB PHY.	
0Eh (100B1Dh)	**REG100B1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[15:8]	7:0	See description of '100B1Ch'.	
0Fh (100B1Eh)	**REG100B1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[23:16]	7:0	See description of '100B1Ch'.	
0Fh (100B1Fh)	**REG100B1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[31:24]	7:0	See description of '100B1Ch'.	
10h (100B20h)	**REG100B20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SW_MCU_CLK	0	MCU clock setting. 0: DFT_LIVE. 1: Select the output according to reg_ckg_mcu.	
10h (100B21h)	**REG100B21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_MCU[4:0]	4:0	CLK_MCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: 216MHz. 001: 192MHz. 010: 172HMz. 011: 160MHz. 100: 144MHz. 101: 108MHz. 110: Mem_clock. 111: Mem_clock div 2.	
11h (100B22h)	**REG100B22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_OCP[1:0]	1:0	CLK_OCP clock setting. [0]: Disable clock. [1]: Invert clock.	
11h (100B23h)	**REG100B23**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_MIPS_CLK	7	CLK_MIPS switching. 0: DFT_LIVE. 1: Select the output according to reg_ckg_mips.	
	-	6:5	Reserved.	
	CKG_MIPS[4:0]	4:0	CLK_MIPS clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select clk_mipspll_vco. 001: Select clk_xtali. 010: 240 MHz. 1xx: Select XTALI.	
12h (100B24h)	**REG100B24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_32BMCU_CLK	7	32BMCU clock setting. 0: DFT_LIVE. 1: Select the output according to reg_ckg_32BMCU.	
	-	6:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_32BMCU[4:0]	4:0	CLK_32BMCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: 240MHz. 001: 216MHz. 010: 192HMz. 011: 172MHz.	
13h (100B27h)	**REG100B27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_UART0[4:0]	4:0	CLK_UART0 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Reserved.	
14h (100B28h)	**REG100B28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_UART1[4:0]	4:0	CLK_UART1 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Reserved.	
14h (100B29h)	**REG100B29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_UART2[4:0]	4:0	CLK_UART2 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Reserved.	
15h (100B2Ah)	**REG100B2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_FUART[4:0]	4:0	CLK_FUART clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Reserved.	
15h (100B2Bh)	**REG100B2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_SSI[5:0]	5:0	Clock selection for clk_ssi; [0]: Gate; [1]: Inv; [5:2]: Select clock source.	
16h (100B2Ch)	**REG100B2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_SPI[6:0]	6:0	Clock selection for clk_spi; [0]: Gate; [1]: Inv; [5:2]: Select clock source. 0000: XTAL. 0001: 54 MHz. 0010: 86 MHz. 0011: 108 MHz. 0100: 5.4 MHz. 0101: 27 MHz. 0110: 43.2 MHz. 0111: 62 MHz. 1000: 72 MHz. others: Reserved. [6]: Switch clk_spi by glitch-free clock switch. 0: XTAL. 1: Select the output according to CKG_SPI[5:2].	
16h (100B2Dh)	**REG100B2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_SPI_M[5:0]	5:0	Clock selection for clk_spi_m; [0]: Gate; [1]: Inv; [5:2]: Select clock source.	
17h (100B2Eh)	**REG100B2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_UART3[4:0]	4:0	CLK_UART3 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Reserved.	
17h	**REG100B2F**	**7:0**	**Default : 0x00**	**Access : R/W**

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100B2Fh)	-	7:5	Reserved.	
	CKG_UART4[4:0]	4:0	CLK_UART4 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Reserved.	
18h (100B30h)	**REG100B30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_UART5[4:0]	4:0	CLK_UART5 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Reserved.	
19h (100B32h)	**REG100B32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_FCIE[5:0]	5:0	CLK_FCIE clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source.	
19h (100B33h)	**REG100B33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_FCIE_4X[6:0]	6:0	CLK_FCIE_4X clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source.	
1Ah (100B34h)	**REG100B34**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_NFIE_SPREAD[3:0]	3:0	CLK_NFIE clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: 000: 432MHz. 001: 216MHz. 010: 12MHz. 011: Reserved.	
1Ah (100B35h)	**REG100B35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_TCK[1:0]	1:0	CLK_TCK clock setting. [0]: Disable clock. [1]: Invert clock.	
1Bh (100B36h)	**REG100B36**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_MIIC1[3:0]	7:4	CLK_MIIC1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source.	
	CKG_MIIC0[3:0]	3:0	CLK_MIIC0 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source.	
1Ch (100B38h)	**REG100B38**	**7:0**	**Default : 0x17**	**Access : R/W**
	-	7:5	Reserved.	
	SW_MIU_RSTZ	4	CLK_MIU RESET for DIAMOND.	
	-	3	Reserved.	
	CKG_MEMPLL[2:0]	2:0	MEMPLL_CLK_BUF clock setting. .	
1Ch (100B39h)	**REG100B39**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_MPLL_SYN[3:0]	3:0	CLK_MPLL_SYN clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source.	
1Dh (100B3Ah)	**REG100B3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_MIU[4:0]	4:0	CLK_MIU clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Mempll_clk_buf. 01: Mempll_clk_buf_div2. 10: MIU_128BUS_PLL_CLK_VCO_OUT. 11: 216 MHz. [4]: Select HEMCU fast way. 0: Clock select by [3:2]. 1: Clock for HEMCU fast way.	
1Dh (100B3Bh)	**REG100B3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_MIU_256BUS[4:0]	4:0	CLK_MIU_256BUS clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Mempll_clk_buf. 01: Mempll_clk_buf_div2. 10: MIU_128BUS_PLL_CLK_VCO_OUT. 11: 216 MHz. [4]: Select HEMCU fast way. 0: Clock select by [3:2]. 1: Clock for HEMCU fast way.	
1Eh (100B3Ch)	**REG100B3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_MIU_REC[3:0]	3:0	CLK_MIU_REC clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: XTAL div 8. 01: XTAL div 16. 10: XTAL div 64. 11: XTAL div 128.	
1Fh (100B3Eh)	**REG100B3E**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_R2[4:0]	4:0	CLK_R2 clock setting. [0]: Disable clock. [1]: Invert clock.	
1Fh (100B3Fh)	**REG100B3F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_RC[3:0]	3:0	CLK_RC clock setting. [0]: Disable clock. [1]: Invert clock.	
20h (100B40h)	**REG100B40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VEDAC_DIGITAL_P_FOR_VD	1		
	CLK_VD_SEL	0	Select VD clock from ADC1 or ADC2. 0: Select VD_ADC_CLK. 1: Select ADC_CLK.	
20h (100B41h)	**REG100B41**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_VD[3:0]	3:0	CLK_VD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select CLK_VD. 01: Select CLK_VEDAC (TEST_IN Mode). 10: Select VD_TestMode_CLK. 11: Reserved.	
21h (100B42h)	**REG100B42**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_VDMCU[4:0]	4:0	CLK_VDMCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: 172MHz. 001: 160HMz. 010: 144MHz. 011: 123MHz. 100: 108MHz. 101: Mem_clock. 110: Mem_clock div 2. 111: Select XTAL.	
22h (100B44h)	**REG100B44**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_MCU_MAIL0[3:0]	3:0	Clk_mcu_mail0 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select output according to reg_ckg_mcu. 01: Select output according to reg_ckg_vdmcu. 10: Reserved. 11: Reserved.	
22h (100B45h)	**REG100B45**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_MCU_MAIL1[3:0]	3:0	Clk_mcu_mail1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select output according to reg_ckg_mcu. 01: Select output according to reg_ckg_vdmcu. 10: Reserved. 11: Reserved.	
23h (100B46h)	**REG100B46**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_VD2X[1:0]	1:0	CLK_VD2X clock setting. [0]: Disable clock. [1]: Invert clock.	
23h	**REG100B47**	**7:0**	**Default : 0x01**	**Access : R/W**

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100B47h)	-	7:4	Reserved.	
	CKG_VD_32FSC[3:0]	3:0	CLK_VD_32FSC clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: VD_ADC_CLK. 01: Reserved. 10: Reserved. 11: Reserved.	
24h (100B48h)	**REG100B48**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_VE[3:0]	3:0	CLK_VE clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select 27MHz. 01: Reserved. 10: Select XTAL. 11: Reserved.	
24h (100B49h)	**REG100B49**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_VEDAC[4:0]	4:0	CLK_VEDAC clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 27MHz. 001: 54MHz. 010: 108MHz. 011: XTAL. 100: Clk_dac_external_buf. others: Reserved.	
25h (100B4Ah)	**REG100B4A**	**7:0**	**Default : 0x0D**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_VE_IN[4:0]	4:0	CLK_VE_IN clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select CLK_ADC. 001: Select CLK_DVI. 010: Select CLK_VD. 011: Select CLK_DC0. 100: CLK_IDCLK2. 101: Clk_extdi_buf. 110: Clk_sub_dc0_p. 111: Clk_odclk_p.	
26h (100B4Ch)	**REG100B4C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DACA2[3:0]	3:0	CLK_DACA2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select VIF clock (clk_vifdbb_dac_p). 01: Select VD clock. 10: Clk_dac_external_buf. 11: Reserved.	
26h (100B4Dh)	**REG100B4D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DACB2[3:0]	3:0	CLK_DACB2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select VIF clock (clk_vifdbb_dac_p). 01: Select VD clock. 10: Clk_dac_external_buf. 11: Reserved.	
27h (100B4Eh)	**REG100B4E**	**7:0**	**Default : 0x01**	**Access : R/W**
	CKG_TSP_AESDMA[3:0]	7:4	CLK_TSP_AESDMA clock setting.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_TSO_TRACE[3:0]	3:0	CLK_TSO tracing clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 216MHz.	
27h (100B4Fh)	**REG100B4F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TSO_IN[4:0]	4:0	CLK_TSO input clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select TS0_CLK. 001: Select TS1_CLK. 010: Select TS2_CLK. 110: Select TS_CB_CLK. 111: From DeMOD.	
28h (100B50h)	**REG100B50**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TS0[4:0]	4:0	CLK_TS0 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select TS0_CLK. 001: Select TS1_CLK. 010: Select TS2_CLK. 101: Select TSO_out CLK. 110: Select TS_CB_CLK. 111: From DeMOD.	
28h (100B51h)	**REG100B51**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_TS1[4:0]	4:0	CLK_TS1 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select TS0_CLK. 001: Select TS1_CLK. 010: Select TS2_CLK. 101: Select TSO_out CLK. 100: Select TS_CB_CLK. 111: From DeMOD.	
29h (100B52h)	**REG100B52**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TS2[4:0]	4:0	CLK_TS2 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select TS0_CLK. 001: Select TS1_CLK. 010: Select TS2_CLK. 101: Select TSO_out CLK. 110: Select TS_CB_CLK. 111: From DeMOD.	
29h (100B53h)	**REG100B53**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TS_CB[4:0]	4:0	CLK_TS_CB clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select TS0_CLK. 001: Select TS1_CLK. 010: Select TS2_CLK. 101: Select TSO_out CLK. 110: Select TS_CB_CLK. 111: From DeMOD.	
2Ah (100B54h)	**REG100B54**	**7:0**	**Default : 0x1D**	**Access : R/W**
	-	7	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_PARSER[2:0]	6:4	CLK_TSP clock setting. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: 172 MHz. 1: Clk_miu_p.	
	CKG_TSP[3:0]	3:0	CLK_TSP clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 172 MHz. 01: 144 MHz. 10: 123 MHz. 11: 108 MHz.	
2Ah (100B55h)	**REG100B55**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_STC1[3:0]	7:4	CLK_STC1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Clock source. 00: Select STC1 synthesizer output. 01: 1. 10: 27MHz. 11: Reserved.	
	CKG_STC0[3:0]	3:0	CLK_STC0 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Clock source. 00: Select STC0 synthesizer output. 01: 1. 10: 27MHz. 11: Reserved.	
2Bh	**REG100B56**	**7:0**	**Default : 0x22**	**Access : R/W**

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100B56h)	CKG_SYN_STC1[3:0]	7:4	CLK_SYN_STC1 clock setting. 000: Mpll_clk_buf. 001: 432 MHz. 010: Select XTAL. 011: Reserved. 100: 345.6 MHz. 101: Reserved. 110: Reserved. 111: Select XTAL.	
	CKG_SYN_STC0[3:0]	3:0	CLK_SYN_STC0 clock setting. 000: Mpll_clk_buf. 001: 432 MHz. 010: Select XTAL. 011: Reserved. 100: 345.6 MHz. 101: Reserved. 110: Reserved. 111: Select XTAL.	
2Bh (100B57h)	**REG100B57**	**7:0**	**Default : 0xD1**	**Access : R/W**
	CKG_AESDMA[3:0]	7:4	CLK_AESDMA clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source.	
	CKG_STAMP[3:0]	3:0	CLK_STAMP clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: 27 MHz. 01: Reserved. 10: Reserved. 11: Reserved.	
2Ch (100B58h)	**REG100B58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TS_CB_CLK_SAMPLE_EN	0	Enable clk_ts_cb phase adjustment. 0: Disable. 1: Enable.	
2Ch (100B59h)	**REG100B59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TS_CB_CLK_SAMPLE_CNT[3:0]	3:0	CLK_TS_CB phase adjustment counter.	
2Dh (100B5Ah)	**REG100B5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TS0_CLK_SAMPLE_EN	0	Enable clk_ts0 phase adjustment. 0: Disable. 1: Enable.	
2Dh (100B5Bh)	**REG100B5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TS0_CLK_SAMPLE_CNT[3:0]	3:0	CLK_TS0 phase adjustment counter.	
2Eh (100B5Ch)	**REG100B5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TS1_CLK_SAMPLE_EN	0	Enable clk_ts1 phase adjustment. 0: Disable. 1: Enable.	
2Eh (100B5Dh)	**REG100B5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TS1_CLK_SAMPLE_CNT[3:0]	3:0	CLK_TS1 phase adjustment counter.	
2Fh (100B5Eh)	**REG100B5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TS2_CLK_SAMPLE_EN	0	Enable clk_ts2 phase adjustment. 0: Disable. 1: Enable.	
2Fh (100B5Fh)	**REG100B5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TS2_CLK_SAMPLE_CNT[3:0]	3:0	CLK_TS2 phase adjustment counter.	
30h (100B60h)	**REG100B60**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_VD_32BMCU[4:0]	4:0	CLK_VD_32BMCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 160 MHz. 001: 144 MHz. 010: 123 MHz. 011: 108 MHz. 100: 216 MHz. 101: 192 MHz. 110: Reserved. 111: Reserved.	
31h (100B62h)	**REG100B62**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_HVD[3:0]	3:0	CLK_HVD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 216 MHz. 01: 172 MHz. 10: 160 MHz. 11: 144 MHz.	
31h (100B63h)	**REG100B63**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_VP6[3:0]	7:4	CLK_VP6 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 192 MHz. 01: 172 MHz. 10: 160 MHz. 11: 144 MHz.	
	CKG_VP8[3:0]	3:0	CLK_VP8 clock settings. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: 172 MHz. 01: 144 MHz. 10: 120 MHz. 00: Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
32h (100B64h)	**REG100B64**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_APB_VP6[3:0]	3:0	CLK_APB_VP6 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Reserved.	
33h (100B66h)	**REG100B66**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_HDGEN_FIR[4:0]	4:0	Reserved.	
33h (100B67h)	**REG100B67**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_HDGEN_SRC_SEL	5	Reserved.	
	CKG_HDGEN[4:0]	4:0	Reserved.	
34h (100B68h)	**REG100B68**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_HDMI_TX[3:0]	3:0	CLK_HDMI_TX clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : reserved.	
35h (100B6Ah)	**REG100B6A**	**7:0**	**Default : 0x0D**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_JPD[3:0]	3:0	CLK_JPD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 123 MHz. 01: 144 MHz. 10: 160 MHz. 11: 192 MHz.	
37h (100B6Eh)	**REG100B6E**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_DAC1[4:0]	4:0	CLK_DAC1 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Reserved. 001: Clk_vedac_digital. 010: Clk_vd. 011: 12 MHz. 100: Clk_dac_external.	
37h (100B6Fh)	**REG100B6F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_DAC2[4:0]	4:0	Reserved.	
38h (100B71h)	**REG100B71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CKG_MVD_SYNC	0	Set MVD all clock sources equal to clk_miu_p. 0: Disable. 1: Enable.	
39h (100B72h)	**REG100B72**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_MVD[4:0]	4:0	CLK_MVD clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 216 MHz. 001: 192 MHz. 010: 172 MHz. 011: 144 MHz. 100: Clk_miu_p. 101: 123 MHz. 100: Mempll_clk_buf_div2. 111: XTAL clock.	
39h (100B73h)	**REG100B73**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_MVD2[4:0]	4:0	CLK_MVD2 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 216 MHz. 001: 192 MHz. 010: 172 MHz. 011: 144 MHz. 100: Clk_miu_p. 101: 123 MHz. 100: Mempll_clk_buf_div2. 111: XTAL clock.	
3Ah (100B75h)	**REG100B75**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_MVD_LUMA_A[1:0]	1:0	CLK_MVD_LUMMA_A clock setting. [0]: Disable clock. [1]: Invert clock.	
3Bh (100B76h)	**REG100B76**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_MVD_LUMA_B[1:0]	1:0	CLK_MVD_LUMMA_B clock setting. [0]: Disable clock. [1]: Invert clock.	
3Bh (100B77h)	**REG100B77**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_MVD_LUMA_C[1:0]	1:0	CLK_MVD_LUMMA_C clock setting. [0]: Disable clock. [1]: Invert clock.	
3Ch (100B78h)	**REG100B78**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_MVD_RMEM[1:0]	1:0	CLK_MVD_RMEM clock setting. [0]: Disable clock. [1]: Invert clock.	
3Ch (100B79h)	**REG100B79**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_MVD_RMEM1[1:0]	1:0	CLK_MVD_RMEM1 clock setting. [0]: Disable clock. [1]: Invert clock.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (100B7Ah)	**REG100B7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_MVD_CHROMA_B[1:0]	5:4	CLK_MVD_CHROMA_B clock setting. [0]: Disable clock. [1]: Invert clock.	
	-	3:2	Reserved.	
	CKG_MVD_CHROMA_A[1:0]	1:0	CLK_MVD_CHROMA_A clock setting. [0]: Disable clock. [1]: Invert clock.	
3Dh (100B7Bh)	**REG100B7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_MVD_CHROMA_C[1:0]	1:0	CLK_MVD_CHROMA_C clock setting. [0]: Disable clock. [1]: Invert clock.	
3Eh (100B7Ch)	**REG100B7C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_MVD_RREFDAT[1:0]	1:0	CLK_MVD_RREFDAT clock setting. [0]: Disable clock. [1]: Invert clock.	
40h (100B80h)	**REG100B80**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_GOPG0[4:0]	4:0	CLK_GOPG0 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select clk_odclk_p. 01: Select clk_idclk2_p_gate. 10: Select clk_idclk1_p_gate. 11: Select XTAL select clk_occ_frc_p.	
40h (100B81h)	**REG100B81**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_GOPG1[4:0]	4:0	CLK_GOPG1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select clk_odclk_p. 01: Select clk_idclk2_p_gate. 10: Select clk_idclk1_p_gate. 11: Select XTAL select clk_occ_frc_p.	
41h (100B82h)	**REG100B82**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_GOPG2[4:0]	4:0	CLK_GOPG2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select clk_odclk_p. 01: Select clk_idclk2_p_gate. 10: Select clk_idclk1_p_gate. 11: Select XTAL select clk_occ_frc_p.	
41h (100B83h)	**REG100B83**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_GOPD[3:0]	3:0	CLK_GOPD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] select clock source. 00: Select clk_idclk2. 01: Select CLK_ODCLK. 10: Select CLK_DC0. 11: Select clk_sub_dc0.	
42h (100B84h)	**REG100B84**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_GOPG3[4:0]	4:0	CLK_GOPG3 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 00: Select clk_odclk_p. 01: Select clk_idclk2_p_gate. 10: Select clk_idclk1_p_gate. 11: Select XTAL select clk_occ_frc_p.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (100B86h)	**REG100B86**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_PSRAM0[1:0]	1:0	CLK_PSRAM0 clock setting. [0]: Disable clock. [1]: Invert clock.	
43h (100B87h)	**REG100B87**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_PSRAM1[1:0]	1:0	CLK_PSRAM1 clock setting. [0]: Disable clock. [1]: Invert clock.	
45h (100B8Ah)	**REG100B8A**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_ICP[4:0]	4:0	CLK_ICP clock setting. [4:2]: Select clock source. 000: 123MHz. 001: 108MHz. 010: 96MHz. 011: 86MHz.	
45h (100B8Bh)	**REG100B8B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_SENSOR[4:0]	4:0	CLK_SENSOR clock setting. [4:2]: Select clock source. 000: 96MHz. 001: 54MHz. 010: 36MHz. 011: 27MHz. 100: 24MHz. 101: 18MHz. 110: 12MHz. 111: 123MHz.	
48h (100B90h)	**REG100B90**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_GE[3:0]	3:0	CLK_GE clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 216MHz. 01: 172MHz. 10: 160MHz. 11: 144MHz.	
49h (100B92h)	**REG100B92**	**7:0**	**Default : 0x00**	**Access : R/W**
	SC_ODCLK_SYNTH_CTRL_0[7:0]	7:0	SC ODCLK synthesizer control 0.	
49h (100B93h)	**REG100B93**	**7:0**	**Default : 0x00**	**Access : R/W**
	SC_ODCLK_SYNTH_CTRL_0[15:8]	7:0	See description of '100B92h'.	
4Ah (100B94h)	**REG100B94**	**7:0**	**Default : 0x00**	**Access : R/W**
	SC_ODCLK_SYNTH_CTRL_1[7:0]	7:0	SC ODCLK synthesizer control 1.	
4Ah (100B95h)	**REG100B95**	**7:0**	**Default : 0x00**	**Access : R/W**
	SC_ODCLK_SYNTH_CTRL_1[15:8]	7:0	See description of '100B94h'.	
4Bh (100B96h)	**REG100B96**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_SC_ODCLK_SYN[3:0]	3:0	CLK_SC_ODCLK clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 432 MHz. 01: 216 MHz. 10: 12 MHz. 11: Reserved.	
4Ch (100B98h)	**REG100B98**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DC0[3:0]	3:0	CLK_DC0 clock setting (consider with CKG_DC0_4 as REG_CKG_DC[4:0]). [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Synchronous mode. 01: Free-run mode. 10: 160MHz. 11: 144MHz.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Ch (100B99h)	**REG100B99**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DC1[3:0]	3:0	CLK_DC1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Clk_dc0_p. 01: Reserved. 10: 27MHz. 11: Reserved.	
4Dh (100B9Ah)	**REG100B9A**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_SUB_DC0[3:0]	3:0	CLK_DC0 clock setting (consider with REG_CKG_DC0_4 as REG_CKG_DC[4:0]). [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Synchronous mode. 01: Free-run mode. 10: 160MHz. 11: 144MHz.	
4Dh (100B9Bh)	**REG100B9B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_SUB_DC1[3:0]	3:0	CLK_DC1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Synchronous mode. 01: Free-run mode. 10: 27MHz. 11: Reserved.	
4Eh (100B9Dh)	**REG100B9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_DC_F3[3:0]	3:0	CLK_DC_F3 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 160MHz. 01: 86MHz. 10: 54MHz. 11: 27MHz.	
50h (100BA0h)	**REG100BA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DE_ONLY_F3	3	DE only mode for SC_TOP.	
	DE_ONLY_F2	2	DE only mode for SC_TOP.	
	DE_ONLY_F1	1	DE only mode for SC_TOP.	
	DE_ONLY_F0	0	DE only mode for SC_TOP.	
51h (100BA2h)	**REG100BA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_FECLK_F1[3:0]	3:0	CLK_FECLK_F1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select CLK_EDCLK. 01: Select CLK_FCLK. 10: Reserved. 11: Reserved.	
51h (100BA3h)	**REG100BA3**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_FECLK2_F2[3:0]	7:4	CLK_FECLK2_F2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select CLK_EDCLK. 01: Select CLK_FCLK. 10: Reserved. 11: Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_FECLK_F2[3:0]	3:0	CLK_FECLK_F2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select CLK_EDCLK. 01: Select CLK_FCLK. 10: Reserved. 11: Reserved.	
52h (100BA4h)	**REG100BA4**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_MOCLK[2:0]	2:0	CLK_MOCLK clock setting. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: Clk_odclk. 1: Clk_miu.	
52h (100BA5h)	**REG100BA5**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_FCLK[4:0]	4:0	CLK_VCLK clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select 172 MHz. 001: Select CLK_MIU. 010: Select CLK_ODCLK. 011: 216 MHz. 100: 192 MHz. 101: Reserved. 110: Reserved. 111: Select XTAL.	
53h (100BA6h)	**REG100BA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_ODCLK1[3:0]	7:4	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_ODCLK[3:0]	3:0	CLK_ODCLK clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Synthetic clock out. 01: LPLL output clock div2. 10: 27 MHz. 11: LPLL output clock.	
53h (100BA7h)	**REG100BA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_BT656[3:0]	3:0	CLK_BT656 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: SC_PLL_CLK_OUT. 01: LPLL output clock div2. 10: 27 MHz. 11: LPLL output clock.	
54h (100BA8h)	**REG100BA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_IDCLK0[4:0]	4:0	CLK_IDCLK_F0 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: CLK_ADC. 001: CLK_DVI. 010: CLK_VD. 011: CLK_DC0. 100: ODCLK. 101: XTAL. 110: CLK_VD_ADC. 111: CLK_SUB_DC0.	
54h (100BA9h)	**REG100BA9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_IDCLK1[4:0]	4:0	CLK_IDCLK_F1 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: CLK_ADC. 001: CLK_DVI. 010: CLK_VD. 011: CLK_DC0. 100: ODCLK. 101: XTAL. 110: CLK_VD_ADC. 111: CLK_SUB_DC0.	
55h (100BAAh)	**REG100BAA**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_IDCLK2[4:0]	4:0	CLK_IDCLK_F2 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: CLK_ADC. 001: CLK_DVI. 010: CLK_VD. 011: CLK_DC0. 100: ODCLK. 101: XTAL. 110: CLK_VD_ADC. 111: CLK_SUB_DC0.	
55h (100BABh)	**REG100BAB**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_IDCLK3[4:0]	4:0	CLK_IDCLK_F3 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select CLK_ADC. 0001: Select CLK_DVI. 0010: Select CLK_VD. 0011: Select CLK_DC0. 0100: Select ODCLK. 0101: 0. 0110: Select CLK_VD_ADC. 0111: 0. 1xxx: Select XTAL.	
56h (100BACh)	**REG100BAC**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DOT_MINI[3:0]	3:0	CLK_DOT_MINI clock setting. [0]: Disable clock. [1]: Invert clock. [1:0]: Select clock source. 00: CLK_LPLL (from LPLL_TOP). 01: FIFO_CLK (from LPLL_TOP). 10: Reserved. 11: DFT_LIVE.	
56h (100BADh)	**REG100BAD**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DOT_MINI_PRE[3:0]	3:0	CLK_DOT_MINI_PRE clock setting. [0]: Disable clock. [1]: Invert clock. [1:0]: Select clock source. 00: CLK_LPLL (from LPLL_TOP). 01: FIFO_CLK (from LPLL_TOP). 10: Reserved. 11: DFT_LIVE.	
57h (100BAEh)	**REG100BAE**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_FIFO_MINI[3:0]	3:0	CLK_FIFO_MINI clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: CLK_LPLL (from LPLL_TOP). 01: FIFO_CLK (from LPLL_TOP). 10: Reserved. 11: Reserved.	
57h (100BAFh)	**REG100BAF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_TEST_MOD[3:0]	3:0	CLK_TEST_MOD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select clk_test_mod1 (clk_dmdadc). 01: Select clk_test_mod2 (clk_vifdbb_vdac_p0). 10: Select clk_test_mod3. 11: Select clk_test_mod4.	
58h (100BB0h)	**REG100BB0**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_OSD2MOD[3:0]	7:4	CLK_OSD2MOD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: Clk_lpll_buf. 01: Clk_lpll_osd_buf. 10: Clk_fifo_clk_buf. others: Reserved.	
	CKG_TX_MOD[3:0]	3:0	CLK_TX_MOD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: Select CLKO_1X_4XDIGITAL. others: Reserved.	
58h	**REG100BB1**	**7:0**	**Default : 0x11**	**Access : R/W**

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100BB1h)	CKG_SC_OSDC[3:0]	7:4	CLK_SC_OSDC clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. others: Reserved.	
	CKG_OSD_SR_RCLK[3:0]	3:0	CLK_OSD_SR_RCLK clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: Clk_tx_mod_buf. 01: Clk_tx_mod_osd_buf. others: Reserved.	
59h (100BB2h)	**REG100BB2**	**7:0**	**Default : 0x01**	**Access : R/W**
	CKG_DDR_SYN[3:0]	7:4	CLK_DDR_SYN clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: 432 MHz. 01: 216 MHz. 10: 12 MHz. 11: Reserved.	
	CKG_LPLL_SYN[3:0]	3:0	CLK_LPLL_SYN clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: 432 MHz. 01: 216 MHz. 10: 12 MHz. 11: Reserved.	
59h (100BB3h)	**REG100BB3**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_IDCLK_LPLL[3:0]	3:0	CLK_IDCLK_LPLL clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: Select clk_idclk0. 01: Select clk_idclk1. 10: Select clk_idclk2. 11: Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Bh (100BB6h)	**REG100BB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_FLOCK_CLK_SYNTH_OCC_DIV_M[7:0]	7:0	Divider factor for flock_clk_synthetic_occ.	
5Bh (100BB7h)	**REG100BB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_FLOCK_CLK_SYNTH_OCC_DIV_M[15:8]	7:0	See description of '100BB6h'.	
5Ch (100BB8h)	**REG100BB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_FLOCK_CLK_SYNTH_OCC_DIV_N[7:0]	7:0	Divider factor for flock_clk_synthetic_occ.	
5Ch (100BB9h)	**REG100BB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_FLOCK_CLK_SYNTH_OCC_DIV_N[15:8]	7:0	See description of '100BB8h'.	
5Dh (100BBAh)	**REG100BBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_FLOCK_CLK_SYNTH_OCC_DIV_EN_SEL	1	Selection for Enable flock_clk_synthetic_occ divider.	
	CKG_FLOCK_CLK_SYNTH_OCC_DIV_EN	0	Enable flock_clk_synthetic_occ divider.	
5Eh (100BBCh)	**REG100BBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_PRE_IDCLK2[1:0]	7:6	CLK_IDCLK_F2 pre_mux clock setting. [1:0]: select clock source. 00: Clk_adc_buf. 01: Clk_dvi_buf. 10: Clk_extdi_buf. 11: Clk_vd_adc_buf.	
	-	5	Reserved.	
	CKG_PRE_IDCLK1[1:0]	4:3	CLK_IDCLK_F1 pre_mux clock setting. [1:0]: select clock source. 00: Clk_adc_buf. 01: Clk_dvi_buf. 10: Clk_extdi_buf. 11: Clk_vd_adc_buf.	
	-	2	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_PRE_IDCLK0[1:0]	1:0	CLK_IDCLK_F0 pre_mux clock setting. [1:0]: select clock source. 00: Clk_adc_buf. 01: Clk_dvi_buf. 10: Clk_extdi_buf. 11: Clk_vd_adc_buf.	
5Eh (100BBDh)	**REG100BBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_PRE_VE_IN[2:0]	6:4	CLK_VE_IN pre_mux clock setting. [1:0]: select clock source. 00: Clk_adc_buf. 01: Clk_dvi_buf. 10: Clk_extdi_buf. 11: Clk_vd_adc_buf.	
	-	3	Reserved.	
	CKG_PRE_IDCLK3[1:0]	2:1	CLK_IDCLK_F3 pre_mux clock setting. [1:0]: select clock source. 00: Clk_adc_buf. 01: Clk_dvi_buf. 10: Clk_exted_buf. 11: Clk_vd_adc_buf.	
	-	0	Reserved.	
5Fh (100BBEh)	**REG100BBE**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_EDCLK[2:0]	2:0	CLK_edclk clock setting. [0]: Disable clock. [1]: Invert clock. [2:]. 0: Clk_172_buf. others: Reserved.	
5Fh (100BBFh)	**REG100BBF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_SC_HDMIPLL[4:0]	4:0	CLK_SC_HDMIPLL clock setting. [1:0]. 00: Dac_clk_div1_hdmi. 01: Dac_clk_div2_hdmi. 10: Dac_clk_div4_hdmi. 11: Dac_clk_div8_ve.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (100BC0h)	**REG100BC0**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_EMAC_AHB[3:0]	3:0	CLK_emac_ahb clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 123MHz. 01: 86MHz. 10: 62MHz. 11: Reserved.	
60h (100BC1h)	**REG100BC1**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_EMAC_RX[2:0]	2:0	CLK_EMAC_RX clock setting. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: Select CLK_EMAC_RX_in (1007 MHz). 1: Select CLK_EMAC_REF /2 (1007 MHz).	
61h (100BC2h)	**REG100BC2**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_EMAC_TX[2:0]	2:0	CLK_EMAC_TX clock setting. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: Select CLK_EMAC_TX_IN (1007 MHz). 1: Select CLK_EMAC_REF /2 (1007 MHz).	
61h (100BC3h)	**REG100BC3**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_EMAC_TX_REF[2:0]	2:0	CLK_EMAC_TX_REF clock setting. [0]: Disable clock. [1]: Invert clock for CLK_EMAC_TX_REF. [2]: Select clock source. 0: Select CLK_EMAC_TX_IN (50 MHz). 1: Reserved.	
62h (100BC4h)	**REG100BC4**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_EMAC_RX_REF[2:0]	2:0	CLK_EMAC_RX_REF clock setting. [0]: Disable clock. [1]: Invert clock for CLK_EMAC_RX_REF. [2]: Select clock source. 0: Select CLK_EMAC_RX_IN (50 MHz). 1: Reserved.	
64h (100BC8h)	**REG100BC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_NFIE[6:0]	6:0	CLK_NFIE clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: XTAL. 0001: 20 MHz. 0010: 27 MHz. 0011: 32 MHz. 0100: 36 MHz. 0101: 40 MHz. 0110: 43.2MHz. 0111: 54 MHz. 1000: 62 MHz. 1001: 72 MHz. 1010: 80 MHz. 1011: 86 MHz. 1100: Clk_nfie_spread. 1101: 300 KHz. 1110: 24 MHz. 1111: 48 MHz. [6]: Glitch free enable.	
65h (100BCAh)	**REG100BCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_NFIE_DENOMINATOR[7:0]	7:0	Denominator for clk_nfie_spread.	
65h (100BCBh)	**REG100BCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_NFIE_DIVIDER_EN	7	Divider enable for clk_nfie_spread.	
	-	6:2	Reserved.	
	CKG_NFIE_DENOMINATOR[9:8]	1:0	See description of '100BCAh'.	
66h (100BCCh)	**REG100BCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_ONIF[5:0]	5:0	CLK_ONIF clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: XTAL. 001: 62 MHz. 010: 27 MHz. 011: 54 MHz. 100: 72 MHz. 101: 86 MHz. 110: 43.2 MHz. 111: 96 MHz. [5]: Switch clk_spi by glitch-free clock switch. 0: XTAL. 1: Select the output according to CKG_ONIF[4:2].	
68h (100BD0h)	**REG100BD0**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_MPIF[4:0]	4:0	Clk_mpif clock setting; [0]: Disable clock; [1]: Invert clock; [4:2]: select clock source; 000: 72 MHz. 001: 120 MHz. 010: 108 MHz. 011: 86 MHz. 100: 160 MHz. 101: 54 MHz. 110: 27 MHz. 111: 13.5 MHz.	
69h (100BD2h)	**REG100BD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_SDIO0[5:0]	5:0	CLK_SDIO0 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source.	
69h (100BD3h)	**REG100BD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_SDIO1[5:0]	5:0	CLK_SDIO1 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source.	
6Ah (100BD4h)	**REG100BD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_SDIO2[6:0]	6:0	CLK_SDIO1 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source.	
6Ch (100BD8h)	**REG100BD8**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_SMART[4:0]	4:0	Clk_smart clock settings. [0]: Disable clock. [1]: Invert clock. [4:2] : Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. otherwise: Reserved.	
6Ch (100BD9h)	**REG100BD9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_SMART_CA[3:0]	3:0	Clk_smart_ca clock settings. [0]: Disable clock. [1]: Invert clock. [3:2]: switcher_no_jitter selection. [3:2]-0: 27MHz/6. [3:2]-1: 27MHz/2. [3:2]-2: 27MHz/4. [3:2]-3: 27MHz/8.	
6Eh (100BDCh)	**REG100BDC**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_COMBO_WDT[3:0]	3:0	CLK_COMBO_WDT clock settings. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Eh (100BDDh)	**REG100BDD**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_COMBO_BT[3:0]	3:0	CLK_COMBO_BT clock settings. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source.	
6Fh (100BDEh)	**REG100BDE**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_COMBO_GPS[3:0]	3:0	CLK_COMBO_GPS clock settings. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source.	
6Fh (100BDFh)	**REG100BDF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	COMBO_PLL_DVFS_PD	4	CLK_COMBO_PLL_SEL control selection.	
	CKG_COMBO_PLL_SEL[3:0]	3:0	CLK_COMBO_PLL_SEL clock settings. [3:2]: Select clock source. 00: 240 MHz. 01: 216 MHz. 10: 192 MHz. 11: Reserved.	
70h (100BE0h)	**REG100BE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	UPDATE_DC0_SYNC_CW	1	Update the control words of DC0 synthesizer that is synchronized to STC0.	
	UPDATE_DC0_FREERUN_CW	0	Update the control words of DC0 free-running synthesizer.	
70h (100BE1h)	**REG100BE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	UPDATE_DC1_SYNC_CW	1	Update the control words of DC1 synthesizer that is synchronized to STC1.	
	UPDATE_DC1_FREERUN_CW	0	Update the control words of DC1 free-running synthesizer.	
71h (100BE2h)	**REG100BE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SYNC_EN_CMDQ	0	Reserved.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
72h (100BE4h)	**REG100BE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[7:0]	7:0	Control word of the synthesizer of MPEG VOP0 clocks.	
72h (100BE5h)	**REG100BE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[15:8]	7:0	See description of '100BE4h'.	
73h (100BE6h)	**REG100BE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[23:16]	7:0	See description of '100BE4h'.	
73h (100BE7h)	**REG100BE7**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[31:24]	7:0	See description of '100BE4h'.	
74h (100BE8h)	**REG100BE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_NUM[7:0]	7:0	Numerator of the synthesizer of DC0.	
74h (100BE9h)	**REG100BE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_NUM[15:8]	7:0	See description of '100BE8h'.	
75h (100BEAh)	**REG100BEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_DEN[7:0]	7:0	Denominator of the synthesizer of DC0.	
75h (100BEBh)	**REG100BEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_DEN[15:8]	7:0	See description of '100BEAh'.	
76h (100BECh)	**REG100BEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC1_FREERUN_CW[7:0]	7:0	Control word of the synthesizer of MPEG VOP0 clocks.	
76h (100BEDh)	**REG100BED**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC1_FREERUN_CW[15:8]	7:0	See description of '100BECh'.	
77h (100BEEh)	**REG100BEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC1_FREERUN_CW[23:16]	7:0	See description of '100BECh'.	
77h (100BEFh)	**REG100BEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC1_FREERUN_CW[31:24]	7:0	See description of '100BECh'.	
78h (100BF0h)	**REG100BF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC1_NUM[7:0]	7:0	Numerator of the synthesizer of DC1.	
78h (100BF1h)	**REG100BF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC1_NUM[15:8]	7:0	See description of '100BF0h'.	
79h (100BF2h)	**REG100BF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC1_DEN[7:0]	7:0	Denominator of the synthesizer of DC1.	
79h	**REG100BF3**	**7:0**	**Default : 0x00**	**Access : R/W**

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100BF3h)	DC1_DEN[15:8]	7:0	See description of '100BF2h'.	
7Ch (100BF8h)	**REG100BF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TSO_OUT_DIVNUM[4:0]	4:0	CLK_TSO_OUT divider factor.	
7Ch (100BF9h)	**REG100BF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TSO_OUT_PH_TUN_NUM[4:0]	4:0	TSP TSO output clock phase tuning number.	
7Dh (100BFAh)	**REG100BFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_P_TSO_OUT[1:0]	5:4	Pre tso out clock setting. [1:0]: Select clock source. 00: Clk_ts0_in. 01: Clk_ts1_in. 10: Clk_ts2_in. 11: Clk_ts_cb_in.	
	-	3	Reserved.	
	CKG_TSO_OUT_PH_TUN_EN	2	Enable TSO OUT output clock phase tuning. 0: Disable. 1: Enable.	
	CKG_TSO_OUT_INV	1	TSO_OUT_CLK (to pad) clock setting. 0: Normal phase to pad. 1: Invert phase to pad.	
	CKG_TSO_OUT_DIV_SEL	0	CLK_TSO_OUT_DIV source selection. 0: Select clk_dmplldiv2. 1: Select clk_dmplldiv3.	
7Dh (100BFBh)	**REG100BFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TSO_OUT[4:0]	4:0	Tso out clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Tso_out_div. 001: 62MHz. 010: 54MHz. 011: Clk_p_tso_out. 100: Clk_p_tso_out_div8. 101: Clk_demod_ts.	

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CLKGEN0 Register (Bank = 100B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Eh ~ 7Fh (100BFCh ~ 100BFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

UHC1 Register (Bank = 100D)

UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (100D00h)	**HCCAP**	**7:0**	**Default : 0x10**	**Access : RO**
	CAPLENGTH	7:0	Capability Register Length. This register is used as an offset to be added to register base to determine the beginning of the Operational Register Space.	
01h (100D02h)	**HCCAP**	**7:0**	**Default : 0x00**	**Access : RO**
	HCIVERSION[7:0]	7:0	Host Controller Interface Version Number. This register is a two-byte register containing a BCD encoding of the EHCI revision number supported by the Host Controller.	
01h (100D03h)	**HCCAP**	**7:0**	**Default : 0x01**	**Access : RO**
	HCIVERSION[15:8]	7:0	See description of '2402h'.	
02h (100D04h)	**HCSPARAMS**	**7:0**	**Default : 0x01**	**Access : RO**
	-	7:4	Reserved.	
	N_PORTS	3:0	Number of Ports. This field specifies the number of physical downstream ports implemented on the Host Controller.	
04h (100D08h)	**HCCPARAMS**	**7:0**	**Default : 0x06**	**Access : RO**
	-	7:3	Reserved.	
	ASYN_SCH_PARK_CAP	2	Asynchronous Schedule Park Capability. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via the Frame List Size field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	PROG_FR_LIST_FLAG	1	Programmable Frame List Flag. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Controller via Frame List Size Field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	-	0	Reserved.	
08h (100D10h)	**USBCMD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INT_OAAD	6	Interrupt on Asynchronous Advance Doorbell. This bit is used as a doorbell by software to ring the Host Controller to issue an interrupt at the next advance of Asynchronous Schedule.	
	ASCH_EN	5	Asynchronous Schedule Enable. This bit controls whether the Host Controller skips the processing of Asynchronous Schedule. 0: Do not process Asynchronous Schedule. 1: Use the ASYNCLISTADDR register to access the Asynchronous Schedule.	
	PSCH_EN	4	Periodic Schedule Enable. This bit controls whether the Host Controller skips the processing of Periodic Schedule. 0: Do not process Periodic Schedule. 1: Use the PERIODICKISTBASE register to access the Periodic Schedule.	
	FRL_SIZE	3:2	Frame List Size. This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value). 01: 512 elements (2048 bytes). 10: 256 elements (1024 bytes). 11: Reserved.	
	HC_RESET	1	Host Controller Reset. This control bit is used by software to reset the Host Controller.	
	RS	0	Run/Stop. When this bit is set to '1', the Host Controller proceeds with the execution of schedule. 0: Stop. 1: Run.	
08h (100D11h)	**USBCMD**	**7:0**	**Default : 0x0b**	**Access : R/W**
	-	7:4	Reserved.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ASYN_PK_EN	3	Asynchronous Schedule Park Mode Enable. Software uses this register to enable or disable the Park mode. When this register is set to 1, the Park mode is enabled.	
	-	2	Reserved.	
	ASYN_PK_CNT	1:0	Asynchronous Schedule Park Mode Count. This field contains a count for the number of successive transactions that the Host Controller is allowed to execute from a high-speed queue head on Asynchronous Schedule.	
09h (100D12h)	**USBCMD**	**7:0**	**Default : 0x08**	**Access : R/W**
	INT_THRC	7:0	Interrupt Threshold Control. This field is used by system software to select the maximum rate at which the Host Controller will issue interrupts. The only valid values are described below: Value — Maximum Interrupt Interval for High Speed 00h — Reserved. 01h — 1 micro-frame. 02h — 2 micro-frames. 04h — 4 micro-frames. 08h — 8 micro-frames (default, equals to 1ms). 10h — 16 micro-frames (2 ms). 20h — 32 micro-frames (4 ms). 40h — 64 micro-frames (8 ms). Note: For Full Speed, these registers are reserved.	
0Ah (100D14h)	**USBSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:6	Reserved.	
	INT_OAA	5	Interrupt on Async Advance. This status bit indicates the assertion of interrupt on Async Advance Doorbell.	
	H_SYSERR	4	Host System Error. The Host Controller sets this bit to 1 when a serious error occurred during a host system access involving the Host Controller module.	
	FRL_ROL	3	Frame List Rollover. The Host Controller sets this bit to 1 when the Frame List Index rolls over from its maximum value to zero.	
	PO_CHG_DET	2	Port Change Detect.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			The Host Controller sets this bit to '1' when any port has a change bit transition from '0' to '1'. In addition, this bit is loaded with the OR of all of the PORTSC change bits.	
	USBERR_INT	1	USB Error Interrupt. The Host Controller sets this bit to '1' when the completion of a USB transaction results in an error condition.	
	USB_INT	0	USB Interrupt. The Host Controller sets this bit to '1' upon the completion of a USB transaction.	
0Ah (100D15h)	**USBSTS**	**7:0**	**Default : 0x10**	**Access : RO**
	ASCH_STS	7	Asynchronous Schedule Status. This bit reports the actual status of Asynchronous Schedule.	
	PSCH_STS	6	Periodic Schedule Status. This bit reports the actual status of Periodic Schedule.	
	RECLAMATION	5	Reclamation. This is a read-only status bit, and is used to detect an empty of Asynchronous Schedule.	
	HCHALTED	4	Host Controller Halted. This bit is a zero whenever the Run/Stop bit is set to '1'. The Host Controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to '0'.	
	-	3:0	Reserved.	
0Ch (100D18h)	**USBINTR**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_OAA_EN	5	Interrupt on Async Advance Enable. When this bit is set to '1', and the Interrupt on Async Advance bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	H_SYSERR_EN	4	Host System Error Enable. When this bit is set to '1', and the Host System Error Status bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FRL_ROL_EN	3	Frame List Rollover Enable. When this bit is set to '1', and the Frame List Rollover bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	PO_CHG_INT_EN	2	Port Change Interrupt Enable. When this bit is set to '1', and the Port Change Detect bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	USBERR_INT_EN	1	USB Error Interrupt Enable. When this bit is set to '1', and the USBERRINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	USB_INT_EN	0	USB Interrupt Enable. When this bit is set to '1', and the USBINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
0Eh (100D1Ch)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRINDEX[7:0]	7:0	Frame Index. This register is used by the Host Controller to index the frame into the Periodic Frame List. It updates every 125 microseconds. This register cannot be written unless the Host Controller is in the Halted state.	
0Eh (100D1Dh)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRINDEX[13:8]	5:0	See description of '1Ch'.	
12h (100D25h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[15:12]	7:4	Periodic Frame List Base Address. This register contains the beginning address of the Periodic Frame List in the system memory. These bits correspond to memory address signals [31:12].	
	-	3:0	Reserved.	
13h (100D26h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[23:16]	7:0	See description of '25h'.	
13h (100D27h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[31:24]	7:0	See description of '25h'.	
14h	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100D28h)	ASYNC_LADR[7:5]	7:5	Current Asynchronous List Address. This register contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5].	
	-	4:0	Reserved.	
14h (100D29h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[15:8]	7:0	Please see description of '28h'.	
15h (100D2Ah)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[23:16]	7:0	Please see description of '28h'.	
15h (100D2Bh)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[31:24]	7:0	Please see description of '28h'.	
18h (100D30h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, R/WC, RO**
	PO_SUSP	7	Port Suspend (R/W). 1: Port is in suspend state. 0: Port is not in suspend state. The Port Enable bit and Suspend bit of this register define the port state as follows: Bits [Port Enable, Suspend] — Port State 0X — Disable Enable Suspend During the suspend state, downstream propagation of data is blocked on this port, except for port reset. While in the suspend state, the port is sensitive to resume detection. Writing a zero to this bit is ignored by the Host Controller. The Host Controller will unconditionally set this bit to a zero when: The software sets Force Port Resume bit to a zero (from a one) The software sets Port Reset bit to a one (from a zero) Note: Before setting this bit, RUN/STOP bit should be set to 0.	
	F_PO_RESM	6	Force Port Resume (R/W). 1: Resume detected/driven on port. 0: No resume detected/driven on port. Software sets this bit to a one to resume signaling.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			The Host Controller sets this bit to a one if a J-to-K transition is detected while the port is in the suspend state. When this bit transits to a one for the detection of a J-to-K transition, the Port Change Detect bit in USBSTS register is also set to a one.	
	POR_RESET_STS	5	USB port reset status. The bit is a read only status.	
		4	Reserved.	
	PO_EN_CHG	3	Port Enable/Disable Change (R/WC). 1: Port enable/disable status has changed. 0: No change.	
	PO_EN	2	Port Enable/Disable (R/W). 1: Enable. 0: Disable. Ports can only be enabled by the Host Controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field.	
	CONN_CHG	1	Connect Status Change (R/WC). 1: Change current connect status. 0: No change. This bit indicates a change has occurred in the port's current connect status.	
	CONN_STS	0	Current Connect Status (RO). 1: Device is present on the port. 0: No device is present. This value reflects the current state of the port, and may not correspond directly to cause the Connect Status Change bit to be set. When TST_FORCEEN is set to '1', this signal is the output of U_HDISCON.	
18h (100D31h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	-	7:4	Reserved.	
	LINE_STS	3:2	Line Status (RO). These bits reflect the current logical levels of the D+ and D- signal lines.	
	-	1	Reserved.	
	PO_RESET	0	Port Reset. 1: Port is in reset. 0: Port is not in reset. When the software writes a one to this bit, the bus	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			reset sequence as defined in the USB spec. is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence. Note: Before setting this bit, RUN/STOP bit should be set to 0.	
1Ah (100D34h)	**HCMISC**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	U_SUSP_N	6	Transceiver Suspend Mode. Active LOW places the transceiver in suspend mode that draws minimal power from power supplies. This is part of the power management.	
	EOF2_TIME	5:4	EOF 2 Timing Points, controlling EOF 2 timing point before next SOF. High-Speed EOF2 Time: 00: 2 clocks (30 MHz) = 66ns. 01: 4 clocks (30 MHz) = 133ns. 10: 8 clocks (30 MHz) = 266ns. 11: 16 clocks (30 MHz) = 533ns. Full-Speed EOF2 Time: 00: 20 clocks (30 MHz) = 666ns. 01: 40 clocks (30 MHz) = 1.333us. 10: 80 clocks (30 MHz) = 2.66us. 11: 160 clocks (30 MHz) = 5.3us. Low-Speed EOF2 Time: 00: 40 clocks (30 MHz) = 1.33us. 01: 80 clocks (30 MHz) = 2.66us. 10: 160 clocks (30 MHz) = 5.33us. 11: 320 clocks (30 MHz) = 10.66us.	
	EOF1_TIME	3:2	EOF 1 Timing Points, controlling EOF 1 timing point before next SOF. This value should be adjusted according to the maximum packet size. High-Speed EOF1 Time: 00: 6us. 01: 12us. 10: 24us. 11: 36us. Full-Speed EOF1 Time: 00: 53.3us.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			01: 70.0us. 10: 86.0us. 11: 700us. Low-Speed EOF1 Time: 00: 3750 clocks (30 MHz) = 125us. 01: 3500 clocks (30 MHz) = 116us. 10: 3250 clocks (30 MHz) = 108us. 11: 4000 clocks (30 MHz) = 133us.	
	ASYN_SCH_SLPT	1:0	Asynchronous Schedule Sleep Timer, controlling the Asynchronous Schedule sleep timer. 00: 5us. 01: 10us. 10: 15us. 11: 20us.	
20h (100D40h)	**BMCS**	**7:0**	**Default : 0x10**	**Access : R/W**
	FORCE_NO_CHIRP	7	Force Full/Low speed mode	
	-	6:5	Reserved (must be set to '0' at all times).	
	VBUS_OFF	4	VBUS Off. This bit controls the voltage on VBUS ON/OFF (Default is OFF) or in other words, the signal U_DRVBUS. 0: VBUS On. 1: VBUS Off.	
	INT_POLARITY	3	Control the polarity of system interrupt signal SYS_INT_N. 0: Active LOW (default). 1: Active HIGH.	
	HALF_SPEED	2	Half Speed Enable. 1: FIFO controller asserts ACK to DMA once every two clock cycles. 0: FIFO controller asserts ACK to DMA continuously. This bit is set to '1' while implementing FPGA.	
	HDISCON_FLT_SEL	1	Select a timer to filter out noise of HDISCON from UTMI+. 0: Approximated to 135 us. 1: Approximated to 270 us.	
	VBUS_FLT_SEL	0	Select a timer to filter out noise of VBUS_VLD from UTMI+. This signal is valid when signal U_VBUSVLD is connected.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Approximated to 135 us. 1: Approximated to 472 us.	
20h (100D41h)	**BMCS**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	HOST_SPD_TYP	2:1	Host Speed Type, indicating speed type of the attached device. 10: HS. 00: FS. 01: LS. 11: Reserved.	
	VBUS_VLD	0	VBUS Valid. When the voltage on VBUS is above the valid VBUS threshold, this signal is valid when U_VBUSVLD is connected.	
22h (100D44h)	**BUSMONINTSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:5	Reserved.	
	DMA_ERROR	4	DMA Error Interrupt. DMA operation cannot be finished normally, and an error signal is received. When CPU initiates DMA to fill up or read out device's FIFO, and DMA controller gets error response from system bus, this bit will be set. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DMA_CMPLT	3	DMA Completion Interrupt. DMA operation is finished normally. When CPU initiates DMA to fill up or read out device's FIFO, this bit will be set after mission completion. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DPLGRMV	2	Device Plug Remove. This register is set to '1' once the device plug is removed. Writing '1' clears this register and writing '0' takes no effect.	
	OVC	1	Over Current Detection. This register is set to '1' when the VBUS does not reach VBUS_VLD within the expected time. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VBUS_ERR	0	VBUS Error. This register is set to '1' when the Bus Monitor state machine moves to "VBUS_ERROR" state. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
24h (100D48h)	**BUSMONINTEN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMA_ERROR_EN	4	DMA_ERROR interrupt enable.	
	DMA_CMPLT_EN	3	DMA_CMPLT interrupt enable.	
	BPLGRMV_EN	2	BPLGRMV interrupt enable.	
	OVC_EN	1	OVC interrupt enable.	
	A_VBUS_ERR_EN	0	A_VBUS_ERR interrupt enable.	
28h (100D50h)	**TST**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_LOOPBK	4	FIFO Loop Back Mode. A '1' turns on the loop-back mode. When this bit is set to '1', the Host Controller will enter the loop-back mode. During the loop-back mode, the Host Controller will use manual setting of DMA control to trigger DMA master.	
	TST_MOD	3	Test Mode. A '1' turns on the test mode. When this bit is set to '1', the Host Controller will enter the test mode. This test mode can save simulation time. In normal mode, the Host Controller uses a counter for 10 ms detection of USB reset. The count is a large number. In test mode, the Host Controller will use a smaller number counter for USB reset detection to save the test cycle on test machine.	
	TST_PKT	2	Test Mode for Packet. Upon writing a '1' to this bit, the Host Controller repetitively sends the packet defined in UTMI spec. to transceiver. Run/Stop bit should also be enabled to enable the function.	
	TST_KSTA	1	Upon writing a '1', the D+/D- is set to the high-speed K state.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TST_JSTA	0	Upon writing a '1', the D+/D- is set to the high-speed J state.	
38h (100D70h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DMA_IO	3	DMA IO to IO. Force DMA Controller not to toggle address. This bit is set when the DMA target is not a system memory but an IO device. If this register is set to '1', the 'DMA_LEN' must be an integer multiple of DWORD (4 byes), and the 'DMA_MADDR' must align to the boundary of DWORD (4 bytes).	
	-	2	Reserved.	
	DMA_TYPE	1	DMA Type, the transfer type of data moving. 0: FIFO to Memory. 1: Memory to FIFO.	
	DMA_START	0	DMA Start, informing DMA Controller to initiate DMA transfer. This bit is set to start the transfer and cleared when the DMA operation is completed. Note that this bit cannot be cleared by software; it can only be cleared by hardware in the case of either DMA completion or DMA error. Note that if DMA_LEN and DMA_START are set at the same time, the DMA_LEN will take effect immediately.	
38h (100D71h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[7:0]	7:0	DMA Length. The total bytes the DMA Controller will move. The unit is byte. The maximum length could be 1024B-1.	
39h (100D72h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[15:8]	7:0	See description of '71h'.	
39h (100D73h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DMA_LEN[16]	0	See description of '71h'.	
3Ah (100D74h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[7:0]	7:0	DMA Memory Address. The starting address of memory to request DMA transfer.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ah (100D75h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[15:8]	7:0	See description of '74h'.	
3Bh (100D76h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[23:16]	7:0	See description of '74h'.	
3Bh (100D77h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[31:24]	7:0	See description of '74h'.	
40h (100D80h)	**PROJ_SPEC_REG0**	7:0	**Default: 0x00**	**Access: R/W, WO**
	DBUS_SELECT	7:5	Selects debug bus banks.	
	SFT_CLK_RECOV	4	Clock recovery controlled by software. The register is R/W and the MIU clock will be always active if the bit is kept as 1.	
	OLD_XI2PV	3	Enables old version XIU access.	
	CLK_STOP	2	Triggers the clock stop mechanism. Set 1 to stop the all clock in UHC. The bit also represents the clock status of UHC. Reading the bit if it is 1, it represents the clock is stopped.	
	EN_RD_RD_SCRAMBLE	1	Enables memory inverted read.	
	EN_RD_WR_SCRAMBLE	0	Enables memory inverted write.	
40h (100D81h)	**PROJ_SPEC_REG1**	**7:0**	**Default: 0x00**	**Access: R/W**
	SPLIT_SHORT_PKT_CLR_ACT	7	If the transfer is a periodic split transaction, the active status will be cleared when a short packet is received.	
	NON_ALIGN_EN	6	Enables MIU address non-alignment mode. It also means enabling new PV2MI bridge.	
	INVALID_MIU_ACS_INTEN	5	Enables interrupt when MIU invalid write occurs.	
	MIU_WR_PROTECT_EN	4	Enables MIU write protect.	
	DAT_RD_PRI_EN	3	The enable option (MIU priority access) of the "data read".	
	DAT_WR_PRI_EN	2	The enable option (MIU priority access) of the "data write".	
	QT_RD_PRI_EN	1	The enable option (MIU priority access) of the "q-table read".	
	QT_WR_PRI_EN	0	The enable option (MIU priority access) of the "q-table write".	
41h (100D82h)	**PROJ_SPEC_REG2**	**7:0**	**Default: 0x00**	**Access: R/W**
	QT_RD_PRI_SEL	7:6	The select (delay time of MIU priority assert) of the	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			"q-table read". 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	QT_WR_PRI_SEL	5:4	The select (delay time of MIU priority assert) of the "q-table write". 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	DAT_RD_PRI_SEL	3:2	The select (delay time of MIU priority assert) of the "data read". 2'b00: 21.3us 2'b01: 16.0us 2'b10: 10.7us 2'b11: 5.3us	
	DAT_RD_PRI_SEL	1:0	The select (delay time of MIU priority assert) of the "data write". 2'b00: 21.3us 2'b01: 16.0us 2'b10: 10.7us 2'b11: 5.3us	
41h (100D83h)	**PROJ_SPEC_REG3**	**7:0**	**Default: -**	**Access: R/W**
	Miu1_sel	7:6	2'b00: uh2mi_miu1_sel = uh2mi_adr[25] 2'b01: uh2mi_miu1_sel = uh2mi_adr[24] 2'b10: uh2mi_miu1_sel = uh2mi_adr[23] 2'b11: uh2mi_miu1_sel = uh2mi_adr[22]	
	Reserved	5	Reserved	
	En_last_done	4	Enable the mechanism that UHC state machine will wait until the last write data is done (mi2uh_last_done_z) when in write memory cycle.	
	Periodic_pri_sel	3:2	The select (delay time of MIU priority assert) of the periodic (Isochronous an Interrupt) transfer. 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	periodic_high_pri_en	1	Enable option for MIU high priority when proceeding periodic (Isochronous and Interrupt) transfer.	
	eof1_high_pri_en	0	Enable MIU high priority mechanism when in EOF1 window.	
	fusbh200_dbus[7:0]	7:0	Internal bus for debugging.	
42h (100D84h)	**FDBUS_REG1**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[15:8]	7:0	Internal bus for debugging.	
42h (100D85h)	**FDBUS_REG2**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[23:16]	7:0	Internal bus for debugging.	
43h (100D86h)	**FDBUS_REG3**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[31:24]	7:0	Internal bus for debugging.	
43h (100D87h)	**FDBUS_REG4**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[39:32]	7:0	Internal bus for debugging.	
44h (100D88h)	**FDBUS_REG5**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[47:40]	7:0	Internal bus for debugging.	
44h (100D89h)	**STATUS_REG**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved	
	INVALID_MIU_ACS	0	Interrupt status of invalid MIU write.	
45h (100D8Ah)	**-**	**7:0**	**Default: -**	**Access: R/W1C**
	-	7:0	Reserved	
45h (100D8B)	**MIU_WRITE_RANGE0**	**7:0**	**Default: 0x00**	**Access: -**
	LOWER_BOUND[7:0]	7:0	MIU write protect lower boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
46h (100D8Ch)	**MIU_WRITE_RANGE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[15:8]	7:0	MIU write protect lower boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
46h (100D8Dh)	**MIU_WRITE_RANGE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[23:16]	7:0	MIU write protect lower boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	

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UHC1 Register (Bank = 100D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (100D8Eh)	**MIU_WRITE_RANGE3**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[7:0]	7:0	MIU write protect upper boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
47h (100D8Fh)	**MIU_WRITE_RANGE4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[15:8]	7:0	MIU write protect upper boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (100D90h)	**MIU_WRITE_RANGE5**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[23:16]	7:0	MIU write protect upper boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	

MCU32 Register (Bank = 100F)

MCU32 Register (Bank = 100F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (100F80h)	**REG100F80**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	WPROTEN	4	Write protection region enable. 0: Disable. 1: Enable.	
	-	3:2	Reserved.	
	IOWINORDER	1	IO/MIU write in-order. 0: No in-order. 1: In-order.	
	NCDRAMPOSTW	0	NC write DRAM space post write and merge. 0: Disable. 1: Enable.	
60h	**REG100FC0**	**7:0**	**Default : 0x00**	**Access : R/W**

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MCU32 Register (Bank = 100F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100FC0h)	DRAM1_BASE[7:0]	7:0	Data dram1 address base [15:0]. . usage: Assign DRAM_WRprot = reg_WprotEn &. !((dcu_address[31:16] & DRAM1_mask[15:0]) == DRAM1_BASE[15:0] |. (dcu_address[31:16] & DRAM2_mask[15:0]) == DRAM2_base[15:0]);	
60h (100FC1h)	**REG100FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM1_BASE[15:8]	7:0	See description of '100FC0h'.	
61h (100FC2h)	**REG100FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM1_MASK[7:0]	7:0	Data dram1 address mask [15:0].	
61h (100FC3h)	**REG100FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM1_MASK[15:8]	7:0	See description of '100FC2h'.	
62h (100FC4h)	**REG100FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM2_BASE[7:0]	7:0	Data dram2 address base [15:0].	
62h (100FC5h)	**REG100FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM2_BASE[15:8]	7:0	See description of '100FC4h'.	
63h (100FC6h)	**REG100FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM2_MASK[7:0]	7:0	Data dram2 address mask [15:0].	
63h (100FC7h)	**REG100FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM2_MASK[15:8]	7:0	See description of '100FC6h'.	
74h (100FE8h)	**REG100FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DMASK0[7:0]	7:0	Data qmem address mask [15:0].	
74h (100FE9h)	**REG100FE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DMASK0[15:8]	7:0	See description of '100FE8h'.	
75h (100FEAh)	**REG100FEA**	**7:0**	**Default : 0xF0**	**Access : R/W**
	QMEM_DMASK1[7:0]	7:0	Data qmem address mask [31:16].	
75h (100FEBh)	**REG100FEB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	QMEM_DMASK1[15:8]	7:0	See description of '100FEAh'.	
76h (100FECh)	**REG100FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADDR0[7:0]	7:0	Data qmem matching address [15:0].	
76h (100FEDh)	**REG100FED**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADDR0[15:8]	7:0	See description of '100FECh'.	

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MCU32 Register (Bank = 100F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
77h (100FEEh)	**REG100FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADD1[7:0]	7:0	Data qmem matching address [31:16]. . QMEM_DMASK and QMEM_DADDR usage : Only works for data memory accesses. Let CPU_DADDR[31:0] represents CPU's data access addresses. When. ({REG16_QM_DMASK1, REG16_QM_DMASK0} && CPU_DADDR[31:0]) is equal to. .	
77h (100FEFh)	**REG100FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_DADD1[15:8]	7:0	See description of '100FEEh'.	
78h (100FF0h)	**REG100FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDRAM_BOOT	7	SDRAM code access bit. This will force 32BMCU to access program SDAM when set.	
	SPI_BOOT	6	SPI FLASH code access bit. This will force 32BMCU to access program from SPI FLASH when set.	
	MHG2MI_WPRIORITY	5	32BMCU to miu write priority setting.	
	MHG2MI_RPRIORITY	4	32BMCU to miu read priority setting.	
	DWB_SWAP	3	Data bus bridge endian switch. Default is 1'b0, set 1'b1 to reverse the endian.	
	IWB_SWAP	2	Instruction bus bridge endian switch. Default is 1'b0, set 1'b1 to reverse the endian.	
	SW_RSTZ	1	32BMCU local software reset, default is 1, (i.e. Not in reset mode).	
	MHEG_ENABLE	0	Enable 32BMCU cpu, when MHEG is co-processor.	
79h (100FF2h)	**REG100FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_SEL[7:0]	7:0	Mheg debugger select register. When [15:8] == 0xdb, debugger mode will be on.	
79h (100FF3h)	**REG100FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_SEL[15:8]	7:0	See description of '100FF2h'.	
7Ah (100FF4h)	**REG100FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE0[7:0]	7:0	32BMCU SDR base address [15:0].	
7Ah	**REG100FF5**	**7:0**	**Default : 0x00**	**Access : R/W**

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MCU32 Register (Bank = 100F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(100FF5h)	SDR_BASE0[15:8]	7:0	See description of '100FF4h'.	
7Bh (100FF6h)	**REG100FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE1[7:0]	7:0	32BMCU SDR base address [23:16]. . {REG16_MHG_SDR_BASE1[7:0], REG16_MHG_SDR_BASE0} [23:0]. Mheg dram base address register. Let CPU's internal memory access address be CPU_ADDR_IN[31:0]. Let CPU's address to MIU be CPU_ADDR[31:0]. CPU_ADDR[31:0] will be. {CPU_A.	
7Ch (100FF8h)	**REG100FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	REG32_BASE[7:0]	7:0	Register base address, mapped into addr[31:16]. . REG16_MHG_REG32_BASE [15:0]. 32BMCU RIU register access base register. Must be 0xA000 to access RIU.	
7Ch (100FF9h)	**REG100FF9**	**7:0**	**Default : 0xA0**	**Access : R/W**
	REG32_BASE[15:8]	7:0	See description of '100FF8h'.	
7Dh (100FFAh)	**REG100FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP0[7:0]	7:0	32BMCU SDR address mapping mask [15:0].	
7Dh (100FFBh)	**REG100FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP0[15:8]	7:0	See description of '100FFAh'.	
7Eh (100FFCh)	**REG100FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP1[7:0]	7:0	32BMCU SDR address mapping mask [31:16]. . {REG16_MHG_SDR_MAP1, REG16_MHG_SDR_MAP0} [31:0]. Mheg sdram range mask address registers, when in BOOT_32BMCU mode. Only for Intruction access. Deault is 0xfff0_0000. [1Mbyte]. That is the addresses between 0 ~ 0x000F_FFFF.	
7Eh (100FFDh)	**REG100FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP1[15:8]	7:0	See description of '100FFCh'.	

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MCU32 Register (Bank = 100F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Fh (100FFEh)	**REG100FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_BASE[7:0]	7:0	32BMCU SPI base address. . REG16_MHG_SPI_BASE [15:0]. Mheg spi bank address register. {only data accesses will be constrained by this rule}. usage: When cpu's addr[31:15] == REG16_MHG_SPI_BASE[15:0], The memory access cycles will be directed to SPI Flash.	
7Fh (100FFFh)	**REG100FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_BASE[15:8]	7:0	See description of '100FFEh'.	

MIU Register (Bank = 1012)

MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101200h)	**REG101200**	**7:0**	**Default : 0x00**	**Access : R/W**
	DPD	7	Enter deep power down mode(mobile dram only).	
	-	6	Reserved.	
	AUTO_REF_OFF	5	Turn off auto refresh.	
	ODT	4	Turn on ODT(only for ddr2/ddr3).	
	RSTZ	3	Dram reset.	
	CS	2	Dram chip select.	
	CKE	1	Enable CKE.	
	INIT_MIU	0	Auto initial dram cycle.	
00h (101201h)	**REG101201**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_INIT_DONE	7	Auto initial dram cycle done flag.	
	R_SINGLE_CMD_DONE	6	Single cmd done flag.	
	SELF_REFRESH	5	Enter self refresh mode.	
	SINGLE_CMD[3:0]	4:1	Single cmd = {rasz,casz,wez}.	
	SINGLE_CMD_EN	0	Issue single cmd.	
01h (101202h)	**REG101202**	**7:0**	**Default : 0x00**	**Access : R/W**
	CA_SIZE[1:0]	7:6	00: 8col, 01 : 9col, 10 : 10col, 11 : reserved.	
	BA_SIZE[1:0]	5:4	00: 2ba, 01 : 4ba, 10 : 8ba, 11 : reserved.	
	DRAM_BUS[1:0]	3:2	00: 16bit, 01 : 32bit, 10 : 64bit, 11 : reserved.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DRAM_TYPE[1:0]	1:0	00: Sdr, 01 : ddr, 10 : ddr2, 11 : ddr3.	
01h (101203h)	**REG101203**	**7:0**	**Default : 0xF0**	**Access : R/W**
	CKO_OENZ	7	Ck output enable.	
	ADR_OENZ	6	Address ouput enable.	
	DQ_OENZ	5	Data output enable.	
	CKE_OENZ	4	Cke output enable.	
	DATA_SWAP[1:0]	3:2	01: [15:0], 10 : [31:16].	
	DATA_RATIO[1:0]	1:0	00: 1x, 01 : 2x, 10 : 4x, 11 : 8x.	
02h (101204h)	**REG101204**	**7:0**	**Default : 0x09**	**Access : R/W**
	I64_MODE	7	0: All 128 internal bus, 1 : support 64 internal bus(only 4x mode).	
	TDQSS[1:0]	6:5	Dram TDQSS timing.	
	RD_TIMING[4:0]	4:0	Read back data delay timing.	
02h (101205h)	**REG101205**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_02	7	Reserved.	
	TDQSCK[2:0]	6:4	Dram TDQSCK timing.	
	MCP_TYPE	3	Internal MCP sdram type select.	
	MCP_EN	2	Internal MCP sdram enable.	
	RD_MCK_SEL	1	Feedback mclk/internal mclk.	
	RD_IN_PHASE	0	Read timing phase.	
03h (101206h)	**REG101206**	**7:0**	**Default : 0x08**	**Access : R/W**
	TREFPERIOD[7:0]	7:0	Refresh cycle period, unit 16 mclk.	
03h (101207h)	**REG101207**	**7:0**	**Default : 0x04**	**Access : R/W**
	CSZ_ALWAYS_ON	7	Csz always on.	
	MOBILE_DRAM	6	Dram type is mobile dram.	
	ODT_ALWAYS_ON	5	Odt always on.	
	CKE_ALWAYS_ON	4	Cke always on.	
	-	3	Reserved.	
	TCKE[2:0]	2:0	Dram TCKE timing.	
04h (101208h)	**REG101208**	**7:0**	**Default : 0x33**	**Access : R/W**
	TRP[3:0]	7:4	Dram TRP timing counter bit3~0.	
	TRCD[3:0]	3:0	Dram TRCD tming counter bit3~0.	
04h	**REG101209**	**7:0**	**Default : 0x08**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101209h)	TRP_4	7	Dram tRP timing counter bit4.	
	TRCD_4	6	Dram tRCD tming counter bit4.	
	TRAS[5:0]	5:0	Dram TRAS timing.	
05h (10120Ah)	**REG10120A**	**7:0**	**Default : 0x12**	**Access : R/W**
	TRTP[3:0]	7:4	Dram TRTP timing.	
	TRRD[3:0]	3:0	Dram TRRD timing.	
05h (10120Bh)	**REG10120B**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	
	TRC[5:0]	5:0	Dram TRC timing.	
06h (10120Ch)	**REG10120C**	**7:0**	**Default : 0x61**	**Access : R/W**
	TWR[3:0]	7:4	Dram TWR timing counter bit3~0 : write recovery time.	
	TWL[3:0]	3:0	Dram TWL timing : write latency.	
06h (10120Dh)	**REG10120D**	**7:0**	**Default : 0x63**	**Access : R/W**
	TRTW[3:0]	7:4	Read to write delay.	
	TWTR[3:0]	3:0	Dram TWTR timing : write to read delay.	
07h (10120Eh)	**REG10120E**	**7:0**	**Default : 0x0E**	**Access : R/W**
	TRFC[7:0]	7:0	Dram TRFC timing.	
07h (10120Fh)	**REG10120F**	**7:0**	**Default : 0x11**	**Access : R/W**
	TWR_4	7	Dram tWR timing counter bit4 : write recovery time.	
	TCCD[2:0]	6:4	Dram TCCD timing.	
	TXP[11:8]	3:0	Dram TXP timing.	
08h (101210h)	**REG101210**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[7:0]	7:0	Mode register 0.	
08h (101211h)	**REG101211**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[15:8]	7:0	See description of '101210h'.	
09h (101212h)	**REG101212**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR1[7:0]	7:0	Mode register 1.	
09h (101213h)	**REG101213**	**7:0**	**Default : 0x40**	**Access : R/W**
	MR1[15:8]	7:0	See description of '101212h'.	
0Ah (101214h)	**REG101214**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR2[7:0]	7:0	Mode register 2.	
0Ah (101215h)	**REG101215**	**7:0**	**Default : 0x80**	**Access : R/W**
	MR2[15:8]	7:0	See description of '101214h'.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (101216h)	**REG101216**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR3[7:0]	7:0	Mode register 3.	
0Bh (101217h)	**REG101217**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MR3[15:8]	7:0	See description of '101216h'.	
0Ch (101218h)	**REG101218**	**7:0**	**Default : 0x00**	**Access : R/W**
	MRX[7:0]	7:0	Single command mode register.	
0Ch (101219h)	**REG101219**	**7:0**	**Default : 0x00**	**Access : R/W**
	MRX[15:8]	7:0	See description of '101218h'.	
0Dh (10121Ah)	**REG10121A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEB_SEL[7:0]	7:0	For internal test only, select debug result.	
0Dh (10121Bh)	**REG10121B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEB_SEL[15:8]	7:0	See description of '10121Ah'.	
0Eh (10121Ch)	**REG10121C**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DEB_BUS[7:0]	7:0	Debug port.	
0Eh (10121Dh)	**REG10121D**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DEB_BUS[15:8]	7:0	See description of '10121Ch'.	
0Fh (10121Eh)	**REG10121E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RST_G3	7	Miu arbiter group 3 software reset.	
	SW_RST_G2	6	Miu arbiter group 2 software reset.	
	SW_RST_G1	5	Miu arbiter group 1 software reset.	
	SW_RST_G0	4	Miu arbiter group 0 software reset.	
	SW_INIT_DONE	3	Sw initial done and turn on arbitor.	
	-	2	Reserved.	
	DFT_ADRMD	1	For internal test only.	
	SW_RST_MIU	0	Miu software reset.	
0Fh (10121Fh)	**REG10121F**	**7:0**	**Default : 0x1A**	**Access : R/W**
	NO_RQ_CTRL_EN	7	Turn on the function of when there is no any other request to MIU, let MIU keep servicing the client which is timeouted.	
	CMD_FIFO_4_STAGE	6	Control command fifo to 4 stage(default 8 stage).	
	RESERVED_0F	5	Reserved.	
	SYNC_OUT_THRESHOLD[4:0]	4:0	Sync out FIFO full threshold.	
14h	**REG101229**	**7:0**	**Default : 0x80**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101229h)	RESERVED_14_0	7	Reserved.	
	PACK_EN	6	Pack enable.	
	-	5:0	Reserved.	
15h (10122Bh)	**REG10122B**	**7:0**	**Default : 0x00**	**Access : R / W**
	RESERVED_15_1[1:0]	7:6	Reserved.	
	-	5:0	Reserved.	
17h (10122Eh)	**REG10122E**	**7:0**	**Default : 0x00**	**Access : R / W**
	GROUP_DATA_MASK[7:0]	7:0	For internal test.	
17h (10122Fh)	**REG10122F**	**7:0**	**Default : 0x00**	**Access : R / W**
	GROUP_DATA_MASK[15:8]	7:0	See description of '10122Eh'.	
18h (101230h)	**REG101230**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT2_START[7:0]	7:0	Protect start address unit 8kb.	
18h (101231h)	**REG101231**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT2_START[15:8]	7:0	See description of '101230h'.	
19h (101232h)	**REG101232**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT2_END[7:0]	7:0	Protect end address unit 8kb.	
19h (101233h)	**REG101233**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT2_END[15:8]	7:0	See description of '101232h'.	
1Ah (101234h)	**REG101234**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT3_START[7:0]	7:0	Protect start address unit 8kb.	
1Ah (101235h)	**REG101235**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT3_START[15:8]	7:0	See description of '101234h'.	
1Bh (101236h)	**REG101236**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT3_END[7:0]	7:0	Protect end address unit 8kb.	
1Bh (101237h)	**REG101237**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT3_END[15:8]	7:0	See description of '101236h'.	
1Ch (101238h)	**REG101238**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT0_ID_ENABLE[7:0]	7:0	Protect0 ID enable.	
1Ch (101239h)	**REG101239**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT0_ID_ENABLE[15:8]	7:0	See description of '101238h'.	
1Dh (10123Ah)	**REG10123A**	**7:0**	**Default : 0x00**	**Access : R / W**
	PROTECT1_ID_ENABLE[7:0]	7:0	Protect1 ID enable.	
1Dh	**REG10123B**	**7:0**	**Default : 0x00**	**Access : R / W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10123Bh)	PROTECT1_ID_ENABLE[15:8]	7:0	See description of '10123Ah'.	
1Eh (10123Ch)	**REG10123C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_ID_ENABLE[7:0]	7:0	Protect2 ID enable.	
1Eh (10123Dh)	**REG10123D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_ID_ENABLE[15:8]	7:0	See description of '10123Ch'.	
1Fh (10123Eh)	**REG10123E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_CONTROL[7:0]	7:0	For power saving gated control.	
1Fh (10123Fh)	**REG10123F**	**7:0**	**Default : 0x00**	**Access : R/W**
	LAST_DONE_Z_CLR	7	For clear last_done_z signal.	
	POST_ORDER_CTRL_EN	6	For post order control enable.	
	LAST_DONE_Z_ID[13:8]	5:0	For clear last_done_z id.	
20h (101240h)	**REG101240**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RQ0_CEASELESS_EN	6	Group 0 ceaseless enable.	
	-	5	Reserved.	
	RQ0_TIMEOUT_EN	4	Group 0 timeout enable.	
	RQ0_GROUP_LIMIT_EN	3	Group 0 group limit enable.	
	RQ0_MEMBER_LIMIT_EN	2	Group 0 member limit enable.	
	RQ0_SET_PRIORITY	1	Group 0 set priority pulse.	
	RQ0_ROUND_ROBIN	0	Group 0 round robin enable.	
20h (101241h)	**REG101241**	**7:0**	**Default : 0x84**	**Access : R/W**
	RQ0_ARBITER_SKIP_ON	7	Group 0 skip empty ready on.	
	RQ0_GROUP_CUT_IN_EN	6	Group 0 group cut in enable.	
	RQ0_MEMBER_CUT_IN_EN	5	Group 0 pre-arbiter cut in enable.	
	RQ0_LAST_DONE_Z_OFF	4	Group 0 last_done_z off.	
	RQ0_ORDER_CTRL_RATIO[1:0]	3:2	Group 0 order control ratio.	
	RQ0_CNT1_CTRL_EN	1	Group 0 flow control 1 enable.	
	RQ0_CNT0_CTRL_EN	0	Group 0 flow control 0 enable.	
21h (101242h)	**REG101242**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MEMBER_MAX[7:0]	7:0	Group 0 member max service number, unit 4.	
21h (101243h)	**REG101243**	**7:0**	**Default : 0x20**	**Access : R/W**
	RQ0_GROUP_MAX[7:0]	7:0	Group 0 group max service nember, unit 4.	
22h	**REG101244**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101244h)	RQ0_TIMEOUT[7:0]	7:0	Group 0 time out number.	
22h (101245h)	**REG101245**	**7:0**	**Default : 0x04**	**Access : R/W**
	RQ0_TIMEOUT[15:8]	7:0	See description of '101244h'.	
23h (101246h)	**REG101246**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MASK[7:0]	7:0	Group 0 request mask.	
23h (101247h)	**REG101247**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MASK[15:8]	7:0	See description of '101246h'.	
24h (101248h)	**REG101248**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ0_HPMASK[7:0]	7:0	Group 0 high priority mask.	
24h (101249h)	**REG101249**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ0_HPMASK[15:8]	7:0	See description of '101248h'.	
25h (10124Ah)	**REG10124A**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ01_PRIORITY[3:0]	7:4	Group0 2nd priority id.	
	RQ00_PRIORITY[3:0]	3:0	Group0 1st priority id.	
25h (10124Bh)	**REG10124B**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ03_PRIORITY[3:0]	7:4	Group0 4th priority id.	
	RQ02_PRIORITY[3:0]	3:0	Group0 3rd priority id.	
26h (10124Ch)	**REG10124C**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ05_PRIORITY[3:0]	7:4	Group0 6th priority id.	
	RQ04_PRIORITY[3:0]	3:0	Group0 5th priority id.	
26h (10124Dh)	**REG10124D**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ07_PRIORITY[3:0]	7:4	Group0 8th priority id.	
	RQ06_PRIORITY[3:0]	3:0	Group0 7th priority id.	
27h (10124Eh)	**REG10124E**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ09_PRIORITY[3:0]	7:4	Group0 10th priority id.	
	RQ08_PRIORITY[3:0]	3:0	Group0 9th priority id.	
27h (10124Fh)	**REG10124F**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ0B_PRIORITY[3:0]	7:4	Group0 12th priority id.	
	RQ0A_PRIORITY[3:0]	3:0	Group0 11th priority id.	
28h (101250h)	**REG101250**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ0D_PRIORITY[3:0]	7:4	Group0 14th priority id.	
	RQ0C_PRIORITY[3:0]	3:0	Group0 13th priority id.	
28h	**REG101251**	**7:0**	**Default : 0xFE**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101251h)	RQ0F_PRIORITY[3:0]	7:4	Group0 16th priority id.	
	RQ0E_PRIORITY[3:0]	3:0	Group0 15th priority id.	
29h	**REG101252**	**7:0**	**Default : 0x00**	**Access : R/W**
(101252h)	RQ0_LAST_DONE_Z_SEL[7:0]	7:0	Group 0 last done z check in select.	
29h	**REG101253**	**7:0**	**Default : 0x00**	**Access : R/W**
(101253h)	RQ0_LAST_DONE_Z_SEL[15:8]	7:0	See description of '101252h'.	
2Ah	**REG101254**	**7:0**	**Default : 0x00**	**Access : R/W**
(101254h)	RQ0_CNT0_ID1[3:0]	7:4	Group 0 flow control 0 id1.	
	RQ0_CNT0_ID0[3:0]	3:0	Group 0 flow control 0 id0.	
2Ah	**REG101255**	**7:0**	**Default : 0x00**	**Access : R/W**
(101255h)	RQ0_CNT0_PERIOD[7:0]	7:0	Group 0 flow control 0 period number.	
2Bh	**REG101256**	**7:0**	**Default : 0x00**	**Access : R/W**
(101256h)	RQ0_CNT1_ID1[3:0]	7:4	Group 0 flow control 1 id1.	
	RQ0_CNT1_ID0[3:0]	3:0	Group 0 flow control 1 id0.	
2Bh	**REG101257**	**7:0**	**Default : 0x00**	**Access : R/W**
(101257h)	RQ0_CNT1_PERIOD[7:0]	7:0	Group 0 flow control 1 period number.	
2Ch	**REG101258**	**7:0**	**Default : 0x00**	**Access : R/W**
(101258h)	RQ0_TYPE_PRIORITY_SEL[7:0]	7:0	Group 0 type priority select.	
2Ch	**REG101259**	**7:0**	**Default : 0x00**	**Access : R/W**
(101259h)	RQ0_TYPE_PRIORITY_SEL[15:8]	7:0	See description of '101258h'.	
2Dh	**REG10125A**	**7:0**	**Default : 0x00**	**Access : R/W**
(10125Ah)	RESERVED_2D[7:0]	7:0	Reserved.	
2Dh	**REG10125B**	**7:0**	**Default : 0x20**	**Access : R/W**
(10125Bh)	DELAY_CTRL_SEL[1:0]	7:6	Choose delay lateny of new modew.	
	MODE_SEL	5	Reduce latency of cmd (0 is new;1 is ori).	
	ANA_BIST_EN	4	For internal test only.	
	ADC_TEST_EN	3	For internal test only.	
	OUT_OF_AREA_OFF	2	Out of area detect off (1 is detect OFF; 0 is ON).	
	RESERVED_2D[9:8]	1:0	See description of '10125Ah'.	
2Eh	**REG10125C**	**7:0**	**Default : 0x00**	**Access : R/W**
(10125Ch)	RQ0_LIMIT_MASK[7:0]	7:0	Group 0 client limit mask.	
2Eh	**REG10125D**	**7:0**	**Default : 0x00**	**Access : R/W**
(10125Dh)	RQ0_LIMIT_MASK[15:8]	7:0	See description of '10125Ch'.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (10125Eh)	**REG10125E**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ0_LAST_DONE_Z[7:0]	7:0	Group 0 last done flag.	
2Fh (10125Fh)	**REG10125F**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ0_LAST_DONE_Z[15:8]	7:0	See description of '10125Eh'.	
30h (101260h)	**REG101260**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RQ1_CEASELESS_EN	6	Group 1 ceaseless enable.	
	-	5	Reserved.	
	RQ1_TIMEOUT_EN	4	Group 1 timeout enable.	
	RQ1_GROUP_LIMIT_EN	3	Group 1 group limit enable.	
	RQ1_MEMBER_LIMIT_EN	2	Group 1 member limit enable.	
	RQ1_SET_PRIORITY	1	Group 1 set priority pulse.	
	RQ1_ROUND_ROBIN	0	Group 1 round robin enable.	
30h (101261h)	**REG101261**	**7:0**	**Default : 0x84**	**Access : R/W**
	RQ1_ARBITER_SKIP_ON	7	Group 1 skip empty ready on.	
	RQ1_GROUP_CUT_IN_EN	6	Group 1 group cut in enable.	
	RQ1_MEMBER_CUT_IN_EN	5	Group 1 pre-arbiter cut in enable.	
	RQ1_LAST_DONE_Z_OFF	4	Group 1 last_done_z off.	
	RQ1_ORDER_CTRL_RATIO[1:0]	3:2	Group 1 order control ratio.	
	RQ1_CNT1_CTRL_EN	1	Group 1 flow control 1 enable.	
	RQ1_CNT0_CTRL_EN	0	Group 1 flow control 0 enable.	
31h (101262h)	**REG101262**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MEMBER_MAX[7:0]	7:0	Group 1 member max service number, unit 4.	
31h (101263h)	**REG101263**	**7:0**	**Default : 0x20**	**Access : R/W**
	RQ1_GROUP_MAX[7:0]	7:0	Group 1 group max service nember, unit 4.	
32h (101264h)	**REG101264**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_TIMEOUT[7:0]	7:0	Group 1 time out number.	
32h (101265h)	**REG101265**	**7:0**	**Default : 0x04**	**Access : R/W**
	RQ1_TIMEOUT[15:8]	7:0	See description of '101264h'.	
33h (101266h)	**REG101266**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MASK[7:0]	7:0	Group 1 request mask.	
33h (101267h)	**REG101267**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MASK[15:8]	7:0	See description of '101266h'.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
34h (101268h)	**REG101268**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ1_HPMASK[7:0]	7:0	Group 1 high priority mask.	
34h (101269h)	**REG101269**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ1_HPMASK[15:8]	7:0	See description of '101268h'.	
35h (10126Ah)	**REG10126A**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ11_PRIORITY[3:0]	7:4	Group1 2nd priority id.	
	RQ10_PRIORITY[3:0]	3:0	Group1 1st priority id.	
35h (10126Bh)	**REG10126B**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ13_PRIORITY[3:0]	7:4	Group1 4th priority id.	
	RQ12_PRIORITY[3:0]	3:0	Group1 3rd priority id.	
36h (10126Ch)	**REG10126C**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ15_PRIORITY[3:0]	7:4	Group1 6th priority id.	
	RQ14_PRIORITY[3:0]	3:0	Group1 5th priority id.	
36h (10126Dh)	**REG10126D**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ17_PRIORITY[3:0]	7:4	Group1 8th priority id.	
	RQ16_PRIORITY[3:0]	3:0	Group1 7th priority id.	
37h (10126Eh)	**REG10126E**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ19_PRIORITY[3:0]	7:4	Group1 10th priority id.	
	RQ18_PRIORITY[3:0]	3:0	Group1 9th priority id.	
37h (10126Fh)	**REG10126F**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ1B_PRIORITY[3:0]	7:4	Group1 12th priority id.	
	RQ1A_PRIORITY[3:0]	3:0	Group1 11th priority id.	
38h (101270h)	**REG101270**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ1D_PRIORITY[3:0]	7:4	Group1 14th priority id.	
	RQ1C_PRIORITY[3:0]	3:0	Group1 13th priority id.	
38h (101271h)	**REG101271**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RQ1F_PRIORITY[3:0]	7:4	Group1 16th priority id.	
	RQ1E_PRIORITY[3:0]	3:0	Group1 15th priority id.	
39h (101272h)	**REG101272**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_LAST_DONE_Z_SEL[7:0]	7:0	Group 1 last done z check in select.	
39h (101273h)	**REG101273**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_LAST_DONE_Z_SEL[15:8]	7:0	See description of '101272h'.	
3Ah	**REG101274**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101274h)	RQ1_CNT0_ID1[3:0]	7:4	Group 1 flow control 0 id1.	
	RQ1_CNT0_ID0[3:0]	3:0	Group 1 flow control 0 id0.	
3Ah	**REG101275**	**7:0**	**Default : 0x00**	**Access : R/W**
(101275h)	RQ1_CNT0_PERIOD[7:0]	7:0	Group 1 flow control 0 period number.	
3Bh	**REG101276**	**7:0**	**Default : 0x00**	**Access : R/W**
(101276h)	RQ1_CNT1_ID1[3:0]	7:4	Group 1 flow control 1 id1.	
	RQ1_CNT1_ID0[3:0]	3:0	Group 1 flow control 1 id0.	
3Bh	**REG101277**	**7:0**	**Default : 0x00**	**Access : R/W**
(101277h)	RQ1_CNT1_PERIOD[7:0]	7:0	Group 1 flow control 1 period number.	
3Ch	**REG101278**	**7:0**	**Default : 0x00**	**Access : R/W**
(101278h)	RQ1_TYPE_PRIORITY_SEL[7:0]	7:0	Group 1 type priority select.	
3Ch	**REG101279**	**7:0**	**Default : 0x00**	**Access : R/W**
(101279h)	RQ1_TYPE_PRIORITY_SEL[15:8]	7:0	See description of '101278h'.	
3Dh	**REG10127A**	**7:0**	**Default : 0x00**	**Access : R/W**
(10127Ah)	PROTECT3_ID_ENABLE[7:0]	7:0	Protect3 ID enable.	
3Dh	**REG10127B**	**7:0**	**Default : 0x00**	**Access : R/W**
(10127Bh)	PROTECT3_ID_ENABLE[15:8]	7:0	See description of '10127Ah'.	
3Eh	**REG10127C**	**7:0**	**Default : 0x00**	**Access : R/W**
(10127Ch)	RQ1_LIMIT_MASK[7:0]	7:0	Group 1 client limit mask.	
3Eh	**REG10127D**	**7:0**	**Default : 0x00**	**Access : R/W**
(10127Dh)	RQ1_LIMIT_MASK[15:8]	7:0	See description of '10127Ch'.	
3Fh	**REG10127E**	**7:0**	**Default : 0x00**	**Access : RO**
(10127Eh)	R_RQ1_LAST_DONE_Z[7:0]	7:0	Group 1 last done flag.	
3Fh	**REG10127F**	**7:0**	**Default : 0x00**	**Access : RO**
(10127Fh)	R_RQ1_LAST_DONE_Z[15:8]	7:0	See description of '10127Eh'.	
40h	**REG101280**	**7:0**	**Default : 0x00**	**Access : R/W**
(101280h)	-	7	Reserved.	
	RQ2_CEASELESS_EN	6	Group 2 ceaseless enable.	
	-	5	Reserved.	
	RQ2_TIMEOUT_EN	4	Group 2 timeout enable.	
	RQ2_GROUP_LIMIT_EN	3	Group 2 group limit enable.	
	RQ2_MEMBER_LIMIT_EN	2	Group 2 member limit enable.	
	RQ2_SET_PRIORITY	1	Group 2 set priority pulse.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RQ2_ROUND_ROBIN	0	Group 2 round robin enable.	
40h (101281h)	**REG101281**	**7:0**	**Default : 0x84**	**Access : R/W**
	RQ2_ARBITER_SKIP_ON	7	Group 2 skip empty ready on.	
	RQ2_GROUP_CUT_IN_EN	6	Group 2 group cut in enable.	
	RQ2_MEMBER_CUT_IN_EN	5	Group 2 pre-arbiter cut in enable.	
	RQ2_LAST_DONE_Z_OFF	4	Group 2 last_done_z off.	
	RQ2_ORDER_CTRL_RATIO[1:0]	3:2	Group 2 order control ratio.	
	RQ2_CNT1_CTRL_EN	1	Group 2 flow control 1 enable.	
	RQ2_CNT0_CTRL_EN	0	Group 2 flow control 0 enable.	
41h (101282h)	**REG101282**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_MEMBER_MAX[7:0]	7:0	Group 2 member max service number, unit 4.	
41h (101283h)	**REG101283**	**7:0**	**Default : 0x20**	**Access : R/W**
	RQ2_GROUP_MAX[7:0]	7:0	Group 2 group max service nember, unit 4.	
42h (101284h)	**REG101284**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_TIMEOUT[7:0]	7:0	Group 2 time out number.	
42h (101285h)	**REG101285**	**7:0**	**Default : 0x04**	**Access : R/W**
	RQ2_TIMEOUT[15:8]	7:0	See description of '101284h'.	
43h (101286h)	**REG101286**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_MASK[7:0]	7:0	Group 2 request mask.	
43h (101287h)	**REG101287**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_MASK[15:8]	7:0	See description of '101286h'.	
44h (101288h)	**REG101288**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ2_HPMASK[7:0]	7:0	Group 2 high priority mask.	
44h (101289h)	**REG101289**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ2_HPMASK[15:8]	7:0	See description of '101288h'.	
45h (10128Ah)	**REG10128A**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ21_PRIORITY[3:0]	7:4	Group2 2nd priority id.	
	RQ20_PRIORITY[3:0]	3:0	Group2 1st priority id.	
45h (10128Bh)	**REG10128B**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ23_PRIORITY[3:0]	7:4	Group2 4th priority id.	
	RQ22_PRIORITY[3:0]	3:0	Group2 3rd priority id.	
46h (10128Ch)	**REG10128C**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ25_PRIORITY[3:0]	7:4	Group2 6th priority id.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RQ24_PRIORITY[3:0]	3:0	Group2 5th priority id.	
46h (10128Dh)	**REG10128D**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ27_PRIORITY[3:0]	7:4	Group2 8th priority id.	
	RQ26_PRIORITY[3:0]	3:0	Group2 7th priority id.	
47h (10128Eh)	**REG10128E**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ29_PRIORITY[3:0]	7:4	Group2 10th priority id.	
	RQ28_PRIORITY[3:0]	3:0	Group2 9th priority id.	
47h (10128Fh)	**REG10128F**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ2B_PRIORITY[3:0]	7:4	Group2 12th priority id.	
	RQ2A_PRIORITY[3:0]	3:0	Group2 11th priority id.	
48h (101290h)	**REG101290**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ2D_PRIORITY[3:0]	7:4	Group2 14th priority id.	
	RQ2C_PRIORITY[3:0]	3:0	Group2 13th priority id.	
48h (101291h)	**REG101291**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RQ2F_PRIORITY[3:0]	7:4	Group2 16th priority id.	
	RQ2E_PRIORITY[3:0]	3:0	Group2 15th priority id.	
49h (101292h)	**REG101292**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_LAST_DONE_Z_SEL[7:0]	7:0	Group 2 last done z check in select.	
49h (101293h)	**REG101293**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_LAST_DONE_Z_SEL[15:8]	7:0	See description of '101292h'.	
4Ah (101294h)	**REG101294**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT0_ID1[3:0]	7:4	Group 2 flow control 0 id1.	
	RQ2_CNT0_ID0[3:0]	3:0	Group 2 flow control 0 id0.	
4Ah (101295h)	**REG101295**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT0_PERIOD[7:0]	7:0	Group 2 flow control 0 period number.	
4Bh (101296h)	**REG101296**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT1_ID1[3:0]	7:4	Group 2 flow control 1 id1.	
	RQ2_CNT1_ID0[3:0]	3:0	Group 2 flow control 1 id0.	
4Bh (101297h)	**REG101297**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT1_PERIOD[7:0]	7:0	Group 2 flow control 1 period number.	
4Ch (101298h)	**REG101298**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_TYPE_PRIORITY_SEL[7:0]	7:0	Group 2 type priority select.	
4Ch	**REG101299**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101299h)	RQ2_TYPE_PRIORITY_SEL[15:8]	7:0	See description of '101298h'.	
4Dh (10129Ah)	**REG10129A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_STOP_MODE_OFF	7	Disable clk_stop_mode.	
	TEST_MODE_CLK_EN	6	Enable test_mode_clk.	
	TRTS_DISABLE	5	2cs read to sel disable.	
	INST_PDN_PRA	4	INST_PDN_PRA.	
	INST_PDN_PRA_TRP_EN	3	INST_PDN_PRA_TRP_EN.	
	ARB_BUSY_EN	2	ARB_BUSY_EN.	
	2CKE_EN	1	2cke_sel.	
	2CS_EN	0	2cs enable.	
4Dh (10129Bh)	**REG10129B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_4D_1[1:0]	7:6	Reserved.	
	2CS_CKE_ADDR_SEL[1:0]	5:4	2cs addr sel.	
	RESERVED_4D_0	3	Reserved.	
	TRTS[2:0]	2:0	2cs read to sel.	
4Eh (10129Ch)	**REG10129C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_LIMIT_MASK[7:0]	7:0	Group 2 client limit mask.	
4Eh (10129Dh)	**REG10129D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_LIMIT_MASK[15:8]	7:0	See description of '10129Ch'.	
4Fh (10129Eh)	**REG10129E**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ2_LAST_DONE_Z[7:0]	7:0	Group 2 last done flag.	
4Fh (10129Fh)	**REG10129F**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ2_LAST_DONE_Z[15:8]	7:0	See description of '10129Eh'.	
50h (1012A0h)	**REG1012A0**	**7:0**	**Default : 0x41**	**Access : R/W**
	-	7	Reserved.	
	RQ3_CEASELESS_EN	6	Group 3 ceaseless enable.	
	-	5	Reserved.	
	RQ3_TIMEOUT_EN	4	Group 3 timeout enable.	
	RQ3_GROUP_LIMIT_EN	3	Group 3 group limit enable.	
	RQ3_MEMBER_LIMIT_EN	2	Group 3 member limit enable.	
	RQ3_SET_PRIORITY	1	Group 3 set priority pulse.	
	RQ3_ROUND_ROBIN	0	Group 3 round robin enable.	
50h	**REG1012A1**	**7:0**	**Default : 0x84**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1012A1h)	RQ3_ARBITER_SKIP_ON	7	Group 3 skip empty ready on.	
	RQ3_GROUP_CUT_IN_EN	6	Group 3 group cut in enable.	
	RQ3_MEMBER_CUT_IN_EN	5	Group 3 pre-arbiter cut in enable.	
	RQ3_LAST_DONE_Z_OFF	4	Group 3 last_done_z off.	
	RQ3_ORDER_CTRL_RATIO[1:0]	3:2	Group 3 order control ratio.	
	RQ3_CNT1_CTRL_EN	1	Group 3 flow control 1 enable.	
	RQ3_CNT0_CTRL_EN	0	Group 3 flow control 0 enable.	
51h (1012A2h)	**REG1012A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_MEMBER_MAX[7:0]	7:0	Group 3 member max service number, unit 4.	
51h (1012A3h)	**REG1012A3**	**7:0**	**Default : 0x20**	**Access : R/W**
	RQ3_GROUP_MAX[7:0]	7:0	Group 3 group max service nember, unit 4.	
52h (1012A4h)	**REG1012A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_TIMEOUT[7:0]	7:0	Group 3 time out number.	
52h (1012A5h)	**REG1012A5**	**7:0**	**Default : 0x04**	**Access : R/W**
	RQ3_TIMEOUT[15:8]	7:0	See description of '1012A4h'.	
53h (1012A6h)	**REG1012A6**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_MASK[7:0]	7:0	Group 3 request mask.	
53h (1012A7h)	**REG1012A7**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_MASK[15:8]	7:0	See description of '1012A6h'.	
54h (1012A8h)	**REG1012A8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ3_HPMASK[7:0]	7:0	Group 3 high priority mask.	
54h (1012A9h)	**REG1012A9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ3_HPMASK[15:8]	7:0	See description of '1012A8h'.	
55h (1012AAh)	**REG1012AA**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ31_PRIORITY[3:0]	7:4	Group3 2nd priority id.	
	RQ30_PRIORITY[3:0]	3:0	Group3 1st priority id.	
55h (1012ABh)	**REG1012AB**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ33_PRIORITY[3:0]	7:4	Group3 4th priority id.	
	RQ32_PRIORITY[3:0]	3:0	Group3 3rd priority id.	
56h (1012ACh)	**REG1012AC**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ35_PRIORITY[3:0]	7:4	Group3 6th priority id.	
	RQ34_PRIORITY[3:0]	3:0	Group3 5th priority id.	
56h	**REG1012AD**	**7:0**	**Default : 0x76**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1012ADh)	RQ37_PRIORITY[3:0]	7:4	Group3 8th priority id.	
	RQ36_PRIORITY[3:0]	3:0	Group3 7th priority id.	
57h	**REG1012AE**	**7:0**	**Default : 0x98**	**Access : R/W**
(1012AEh)	RQ39_PRIORITY[3:0]	7:4	Group3 10th priority id.	
	RQ38_PRIORITY[3:0]	3:0	Group3 9th priority id.	
57h	**REG1012AF**	**7:0**	**Default : 0xBA**	**Access : R/W**
(1012AFh)	RQ3B_PRIORITY[3:0]	7:4	Group3 12th priority id.	
	RQ3A_PRIORITY[3:0]	3:0	Group3 11th priority id.	
58h	**REG1012B0**	**7:0**	**Default : 0xDC**	**Access : R/W**
(1012B0h)	RQ3D_PRIORITY[3:0]	7:4	Group3 14th priority id.	
	RQ3C_PRIORITY[3:0]	3:0	Group3 13th priority id.	
58h	**REG1012B1**	**7:0**	**Default : 0xFE**	**Access : R/W**
(1012B1h)	RQ3F_PRIORITY[3:0]	7:4	Group3 16th priority id.	
	RQ3E_PRIORITY[3:0]	3:0	Group3 15th priority id.	
59h	**REG1012B2**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B2h)	RQ3_LAST_DONE_Z_SEL[7:0]	7:0	Group 3 last done z check in select.	
59h	**REG1012B3**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B3h)	RQ3_LAST_DONE_Z_SEL[15:8]	7:0	See description of '1012B2h'.	
5Ah	**REG1012B4**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B4h)	RQ3_CNT0_ID1[3:0]	7:4	Group 3 flow control 0 id1.	
	RQ3_CNT0_ID0[3:0]	3:0	Group 3 flow control 0 id0.	
5Ah	**REG1012B5**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B5h)	RQ3_CNT0_PERIOD[7:0]	7:0	Group 3 flow control 0 period number.	
5Bh	**REG1012B6**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B6h)	RQ3_CNT1_ID1[3:0]	7:4	Group 3 flow control 1 id1.	
	RQ3_CNT1_ID0[3:0]	3:0	Group 3 flow control 1 id0.	
5Bh	**REG1012B7**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B7h)	RQ3_CNT1_PERIOD[7:0]	7:0	Group 3 flow control 1 period number.	
5Ch	**REG1012B8**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B8h)	RQ3_TYPE_PRIORITY_SEL[7:0]	7:0	Group 3 type priority select.	
5Ch	**REG1012B9**	**7:0**	**Default : 0x00**	**Access : R/W**
(1012B9h)	RQ3_TYPE_PRIORITY_SEL[15:8]	7:0	See description of '1012B8h'.	
5Dh	**REG1012BA**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1012BAh)	RESERVED_5D[7:0]	7:0	Reserved.	
5Dh (1012BBh)	**REG1012BB**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_5D[15:8]	7:0	See description of '1012BAh'.	
5Eh (1012BCh)	**REG1012BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_LIMIT_MASK[7:0]	7:0	Group 3 client limit mask.	
5Eh (1012BDh)	**REG1012BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_LIMIT_MASK[15:8]	7:0	See description of '1012BCh'.	
5Fh (1012BEh)	**REG1012BE**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ3_LAST_DONE_Z[7:0]	7:0	Group 3 last done flag.	
5Fh (1012BFh)	**REG1012BF**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ3_LAST_DONE_Z[15:8]	7:0	See description of '1012BEh'.	
60h (1012C0h)	**REG1012C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_R_EN	7	Protection 3 read enable.	
	PROTECT2_R_EN	6	Protection 2 read enable.	
	PROTECT1_R_EN	5	Protection 1 read enable.	
	PROTECT0_R_EN	4	Protection 0 read enable.	
	PROTECT3_W_EN	3	Protection 3 write enable.	
	PROTECT2_W_EN	2	Protection 2 write enable.	
	PROTECT1_W_EN	1	Protection 1 write enable.	
	PROTECT0_W_EN	0	Protection 0 write enable.	
60h (1012C1h)	**REG1012C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_SIZE[3:0]	7:4	0: For test, 1:4MB, 2:8MB, 3:16MB, 4:32MB, 5:64MB, 6:128MB, 7:256, 8:512MB.	
	PROTECT3_INV	3	Protection 3 function invert.	
	PROTECT2_INV	2	Protection 2 function invert.	
	PROTECT1_INV	1	Protection 1 function invert.	
	PROTECT0_INV	0	Protection 0 function invert.	
61h (1012C2h)	**REG1012C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_START_17_16[1:0]	7:6	Protect start address unit 8kb(Bit17~16).	
	PROTECT_ID0[5:0]	5:0	Protection client ID.	
61h (1012C3h)	**REG1012C3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_END_17_16[1:0]	7:6	Protect end address unit 8kb(Bit17~16).	
	PROTECT_ID1[5:0]	5:0	Protection client ID.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (1012C4h)	**REG1012C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_START_17_16[1:0]	7:6	Protect start address unit 8kb(Bit17~16).	
	PROTECT_ID2[5:0]	5:0	Protection client ID.	
62h (1012C5h)	**REG1012C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_END_17_16[1:0]	7:6	Protect end address unit 8kb(Bit17~16).	
	PROTECT_ID3[5:0]	5:0	Protection client ID.	
63h (1012C6h)	**REG1012C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_START_17_16[1:0]	7:6	Protect start address unit 8kb(Bit17~16).	
	PROTECT_ID4[5:0]	5:0	Protection client ID.	
63h (1012C7h)	**REG1012C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_END_17_16[1:0]	7:6	Protect end address unit 8kb(Bit17~16).	
	PROTECT_ID5[5:0]	5:0	Protection client ID.	
64h (1012C8h)	**REG1012C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_START_17_16[1:0]	7:6	Protect start address unit 8kb(Bit17~16).	
	PROTECT_ID6[5:0]	5:0	Protection client ID.	
64h (1012C9h)	**REG1012C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_END_17_16[1:0]	7:6	Protect end address unit 8kb(Bit17~16).	
	PROTECT_ID7[5:0]	5:0	Protection client ID.	
65h (1012CAh)	**REG1012CA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT_ID8[5:0]	5:0	Protection client ID.	
65h (1012CBh)	**REG1012CB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT_ID9[5:0]	5:0	Protection client ID.	
66h (1012CCh)	**REG1012CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT_IDA[5:0]	5:0	Protection client ID.	
66h (1012CDh)	**REG1012CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT_IDB[5:0]	5:0	Protection client ID.	
67h (1012CEh)	**REG1012CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT_IDC[5:0]	5:0	Protection client ID.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
67h (1012CFh)	**REG1012CF**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_67[1:0]	7:6	Reserved.	
	PROTECT_IDD[5:0]	5:0	Protection client ID.	
68h (1012D0h)	**REG1012D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT_IDE[5:0]	5:0	Protection client ID.	
68h (1012D1h)	**REG1012D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_68[1:0]	7:6	Reserved.	
	PROTECT_IDF[5:0]	5:0	Protection client ID.	
69h (1012D2h)	**REG1012D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_START[7:0]	7:0	Protect start address unit 8kb.	
69h (1012D3h)	**REG1012D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_START[15:8]	7:0	See description of '1012D2h'.	
6Ah (1012D4h)	**REG1012D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_END[7:0]	7:0	Protect end address unit 8kb.	
6Ah (1012D5h)	**REG1012D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_END[15:8]	7:0	See description of '1012D4h'.	
6Bh (1012D6h)	**REG1012D6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_START[7:0]	7:0	Protect start address unit 8kb.	
6Bh (1012D7h)	**REG1012D7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_START[15:8]	7:0	See description of '1012D6h'.	
6Ch (1012D8h)	**REG1012D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_END[7:0]	7:0	Protect end address unit 8kb.	
6Ch (1012D9h)	**REG1012D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_END[15:8]	7:0	See description of '1012D8h'.	
6Dh (1012DAh)	**REG1012DA**	**7:0**	**Default : 0x00**	**Access : RO**
	R_HIT_PROTECT_ADDR[7:0]	7:0	Recorde protection hit address.	
6Dh (1012DBh)	**REG1012DB**	**7:0**	**Default : 0x00**	**Access : RO**
	R_HIT_PROTECT_ADDR[15:8]	7:0	See description of '1012DAh'.	
6Eh (1012DCh)	**REG1012DC**	**7:0**	**Default : 0x00**	**Access : RO**
	R_HIT_PROTECT_ADDR[23:16]	7:0	See description of '1012DAh'.	
6Eh (1012DDh)	**REG1012DD**	**7:0**	**Default : 0x00**	**Access : RO**
	R_HIT_PROTECT_ADDR[31:24]	7:0	See description of '1012DAh'.	

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Fh (1012DEh)	**REG1012DE**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_HIT_PROTECT_NO[2:0]	7:5	Record times of hitting protection area.	
	R_HIT_PROTECT_FLAG	4	Indicate protection area been accessed.	
	TEST_BASE_17_16[1:0]	3:2	Test base address(Bit17~16).	
	PROTECT_IRQ_MASK	1	1: Turn on the log of protection function.	
	PROTECT_LOG_CLR	0	1: Turn on the log of protection function.	
6Fh (1012DFh)	**REG1012DF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	R_HIT_PROTECT_ID[5:0]	5:0	Record id which attemp to write protection area.	
70h (1012E0h)	**REG1012E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDR_TOGGLE_MODE	7	For internal test only.	
	FORCE_IN	6	Force read data.	
	FORCE_OUT	5	Force write data.	
	TEST_LOOP	4	Test loop mode.	
	INV_DATA	3	Inver data for test.	
	TEST_MODE[1:0]	2:1	Test mode.	
	TEST_EN	0	Test enable.	
70h (1012E1h)	**REG1012E1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_TEST_FINISH	7	Test finish report.	
	R_TEST_FAIL	6	Test fail report.	
	R_TEST_FLAG	5	Test fail flag.	
	TEST_BYTE[2:0]	4:2	Test data byte select.	
	WRITE_ONLY	1	Only write command is accepted.	
	READ_ONLY	0	Only read command is accepted.	
71h (1012E2h)	**REG1012E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[7:0]	7:0	Test base address.	
71h (1012E3h)	**REG1012E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[15:8]	7:0	See description of '1012E2h'.	
72h (1012E4h)	**REG1012E4**	**7:0**	**Default : 0x08**	**Access : R/W**
	TEST_LENGTH_L[7:0]	7:0	Test length[15:0].	
72h (1012E5h)	**REG1012E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_L[15:8]	7:0	See description of '1012E4h'.	
73h	**REG1012E6**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1012E6h)	TEST_LENGTH_H[7:0]	7:0	Test length[27:16].	
73h (1012E7h)	**REG1012E7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MASK[3:0]	7:4	For internal test only.	
	TEST_LENGTH_H[11:8]	3:0	See description of '1012E6h'.	
74h (1012E8h)	**REG1012E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[7:0]	7:0	Test data.	
74h (1012E9h)	**REG1012E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[15:8]	7:0	See description of '1012E8h'.	
75h (1012EAh)	**REG1012EA**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_STATUS[7:0]	7:0	For internal test only.	
75h (1012EBh)	**REG1012EB**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_STATUS[15:8]	7:0	See description of '1012EAh'.	
76h (1012ECh)	**REG1012EC**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BYTE_FAIL[7:0]	7:0	For internal test only.	
76h (1012EDh)	**REG1012ED**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BYTE_FAIL[15:8]	7:0	See description of '1012ECh'.	
77h (1012EEh)	**REG1012EE**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BIT_FAIL[7:0]	7:0	For internal test only.	
77h (1012EFh)	**REG1012EF**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BIT_FAIL[15:8]	7:0	See description of '1012EEh'.	
78h (1012F0h)	**REG1012F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL0[7:0]	7:0	For internal test only.	
78h (1012F1h)	**REG1012F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL0[15:8]	7:0	See description of '1012F0h'.	
79h (1012F2h)	**REG1012F2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL1[7:0]	7:0	For internal test only.	
79h (1012F3h)	**REG1012F3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL1[15:8]	7:0	See description of '1012F2h'.	
7Ah (1012F4h)	**REG1012F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL2[7:0]	7:0	For internal test only.	
7Ah (1012F5h)	**REG1012F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL2[15:8]	7:0	See description of '1012F4h'.	
7Bh	**REG1012F6**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1012F6h)	MIU_SEL3[7:0]	7:0	For internal test only.	
7Bh (1012F7h)	**REG1012F7**	**7:0**	**Default : 0x00**	**Access : R / W**
	MIU_SEL3[15:8]	7:0	See description of '1012F6h'.	
7Ch (1012F8h)	**REG1012F8**	**7:0**	**Default : 0x00**	**Access : R / W**
	RESERVED_7C[7:0]	7:0	Reserved.	
7Ch (1012F9h)	**REG1012F9**	**7:0**	**Default : 0x00**	**Access : R / W**
	RESERVED_7C[15:8]	7:0	See description of '1012F8h'.	
7Dh (1012FAh)	**REG1012FA**	**7:0**	**Default : 0x00**	**Access : R / W**
	RESERVED_7D[7:0]	7:0	Reserved.	
7Dh (1012FBh)	**REG1012FB**	**7:0**	**Default : 0x00**	**Access : R / W**
	RESERVED_7D[15:8]	7:0	See description of '1012FAh'.	
7Eh (1012FCh)	**REG1012FC**	**7:0**	**Default : 0x00**	**Access : R / W**
	RESERVED_7E[7:0]	7:0	Reseved.	
7Eh (1012FDh)	**REG1012FD**	**7:0**	**Default : 0x00**	**Access : R / W**
	SYNC_IN_STAGE[1:0]	7:6	Stage for others fifo, 00:8, 01:16, 10:32.	
	-	5:4	Reserved.	
	RESERVED_7E[11:8]	3:0	See description of '1012FCh'.	
7Fh (1012FEh)	**REG1012FE**	**7:0**	**Default : 0x87**	**Access : R / W**
	GROUP_PRIORITY3_ID[1:0]	7:6	4th priority group id.	
	GROUP_PRIORITY2_ID[1:0]	5:4	3rd priority group id.	
	GROUP_PRIORITY1_ID[1:0]	3:2	2nd priority group id.	
	GROUP_PRIORITY0_ID[1:0]	1:0	1st priority group id.	
7Fh (1012FFh)	**REG1012FF**	**7:0**	**Default : 0x00**	**Access : RO, R / W**
	R_MIU_SYNCO_BIST_FAIL[1:0]	7:6	Sync out bist fail.	
	R_MIU_SYNCI_BIST_FAIL[1:0]	5:4	Sync in bist fail.	
	-	3	Reserved.	
	RESERVED_6E[1:0]	2:1	Reserved.	
	SET_GROUP_PRIORITY	0	Set group fix priority.	

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MVOP Register (Bank = 1014)

MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101400h)	**REG101400**	**7:0**	**Default : 0x75**	**Access : R/W**
	FRAME_V[7:0]	7:0	Frame vertical total line. (Count from 1, unit: 1 line; include blanking, top and bottom fields).	
00h (101401h)	**REG101401**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	FRAME_V[12:8]	4:0	See description of '101400h'.	
01h (101402h)	**REG101402**	**7:0**	**Default : 0x21**	**Access : R/W**
	FRAME_H[7:0]	7:0	Line pixel total count. (Count from 1, unit: 1 pixel; include H blanking).	
01h (101403h)	**REG101403**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	FRAME_H[12:8]	4:0	See description of '101402h'.	
02h (101404h)	**REG101404**	**7:0**	**Default : 0x6D**	**Access : R/W**
	VB_STR0[7:0]	7:0	Vertical blanking interval 0 start line number (inclusive).	
02h (101405h)	**REG101405**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	VB_STR0[12:8]	4:0	See description of '101404h'.	
03h (101406h)	**REG101406**	**7:0**	**Default : 0x15**	**Access : R/W**
	VB_END0[7:0]	7:0	Vertical blanking interval 0 end line number (exclusive).	
03h (101407h)	**REG101407**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VB_END0[12:8]	4:0	See description of '101406h'.	
04h (101408h)	**REG101408**	**7:0**	**Default : 0x6D**	**Access : R/W**
	VB_STR1[7:0]	7:0	Vertical blanking interval 1 start line number (inclusive).	
04h (101409h)	**REG101409**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	VB_STR1[12:8]	4:0	See description of '101408h'.	
05h (10140Ah)	**REG10140A**	**7:0**	**Default : 0x15**	**Access : R/W**
	VB_END1[7:0]	7:0	Vertical blanking interval 1 end line number (exclusive).	
05h (10140Bh)	**REG10140B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VB_END1[12:8]	4:0	See description of '10140Ah'.	
06h (10140Ch)	**REG10140C**	**7:0**	**Default : 0x6D**	**Access : R/W**
	TF_STR[7:0]	7:0	TOP field toggle start line number (unit: 1 line).	
06h (10140Dh)	**REG10140D**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	TF_STR[12:8]	4:0	See description of '10140Ch'.	
07h (10140Eh)	**REG10140E**	**7:0**	**Default : 0x6D**	**Access : R/W**
	BF_STR[7:0]	7:0	Bottom field toggle start line number (unit: 1 line).	
07h (10140Fh)	**REG10140F**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	BF_STR[12:8]	4:0	See description of '10140Eh'.	
08h (101410h)	**REG101410**	**7:0**	**Default : 0x01**	**Access : R/W**
	HACT_STR[7:0]	7:0	Horizontal active start pixel number (unit: 1 pixel).	
08h (101411h)	**REG101411**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	HACT_STR[12:8]	4:0	See description of '101410h'.	
09h (101412h)	**REG101412**	**7:0**	**Default : 0x01**	**Access : R/W**
	IMG_HSTR[7:0]	7:0	Image active start pixel number (unit: 1 pixel).	
09h (101413h)	**REG101413**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	IMG_HSTR[12:8]	4:0	See description of '101412h'.	
0Ah (101414h)	**REG101414**	**7:0**	**Default : 0x15**	**Access : R/W**
	IMG_VSTR0[7:0]	7:0	Image active start line number for TOP field (unit: 1 pixel).	
0Ah (101415h)	**REG101415**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IMG_VSTR0[12:8]	4:0	See description of '101414h'.	
0Bh (101416h)	**REG101416**	**7:0**	**Default : 0x15**	**Access : R/W**
	IMG_VSTR1[7:0]	7:0	Image active start line number for Bottom field (unit: 1 pixel).	
0Bh (101417h)	**REG101417**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IMG_VSTR1[12:8]	4:0	See description of '101416h'.	
0Ch	**REG101418**	**7:0**	**Default : 0x0E**	**Access : R/W**

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101418h)	TF_VS[7:0]	7:0	TOP field Vsync start line number.	
0Ch (101419h)	**REG101419**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TF_VS[12:8]	4:0	See description of '101418h'.	
0Dh (10141Ah)	**REG10141A**	**7:0**	**Default : 0x0E**	**Access : R/W**
	BF_VS[7:0]	7:0	Bottom field Vsync start line number.	
0Dh (10141Bh)	**REG10141B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	BF_VS[12:8]	4:0	See description of '10141Ah'.	
0Eh (10141Ch)	**REG10141C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TF_VS_MVD[7:0]	7:0	TOP field Vsync start line number to MVD.	
0Eh (10141Dh)	**REG10141D**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	TF_VS_MVD[12:8]	4:0	See description of '10141Ch'.	
0Fh (10141Eh)	**REG10141E**	**7:0**	**Default : 0x00**	**Access : R/W**
	BF_VS_MVD[7:0]	7:0	Bottom field Vsync start line number to MVD.	
0Fh (10141Fh)	**REG10141F**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	BF_VS_MVD[12:8]	4:0	See description of '10141Eh'.	
11h (101422h)	**REG101422**	**7:0**	**Default : 0x00**	**Access : R/W**
	FLD_MD	7	Output mode. 0: Progressive (frame out). 1: Interlace (field out).	
	-	6:4	Reserved.	
	LINE_DUP	3	1: Vertical line duplicate. 0: No duplicate.	
	PIX_DUP	2	1: Horizontal pixel duplicate. 0: No duplicate.	
	-	1	Reserved.	
	DC_EN	0	DC (MVOP) enable. 0: Disable and soft reset. 1: Enable.	
11h	**REG101423**	**7:0**	**Default : 0x00**	**Access : R/W**

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101423h)	MVD_VS_SEL	7	MVOP2MVD_VS select. 1: MVOP2MVD_VS always go ahead 4 lines to MVOP2SC_VS. 0: MVOP2MVD_VS is directly connected to MVOP2SC_VS.	
	MVD_VS_MD	6	0: Original mode. 1: Use new vsync (tf_vs_mvd, bf_vs_mvd).	
	-	5	Reserved.	
	OFLD_INV	4	Invert the field to IP.	
	FLD_INV	3	Invert the field to MVD.	
	-	2	Reserved.	
	FLIP_YC	1	Flip YC order (for debugging). {FLIP_YC, REG_FLIP_UV}= 2'b00 -> Cb Y Cr Y. {FLIP_YC, REG_FLIP_UV}= 2'b01 -> Cr Y Cb Y. {FLIP_YC, REG_FLIP_UV}= 2'b10 -> Y Cb Y Cr. {FLIP_YC, REG_FLIP_UV}= 2'b11 -> Y Cr Y Cb.	
	FLIP_UV	0	Swap Cb, Cr order for 656out (for debugging).	
12h (101424h)	**REG101424**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TST_IMG[2:0]	2:0	000: Normal image from DRAM. 001: Color Bar. 010: Frame color {REG_Y, REG_U, REG_V}. 011: YCbCr Gray Level. 100: Y Gray Level. 101: Cb Gray Level. 110: Cr Gray Level.	
12h (101425h)	**REG101425**	**7:0**	**Default : 0x10**	**Access : R/W**
	Y[7:0]	7:0	Frame Color Y.	
13h (101426h)	**REG101426**	**7:0**	**Default : 0x80**	**Access : R/W**
	U[7:0]	7:0	Frame Color U (Cb).	
13h (101427h)	**REG101427**	**7:0**	**Default : 0x80**	**Access : R/W**
	V[7:0]	7:0	Frame Color V (Cr).	
14h (101428h)	**REG101428**	**7:0**	**Default : 0x08**	**Access : R/W**
	BURST_SEL	7	Timing to calculate burst length (only valid when reg_burst_ext = all). 0: At mi2dc_rdy. 1: At dc2mi_rdy.	

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:5	Reserved.	
	DMA_THD[4:0]	4:0	DMA FIFO threshold. = DMA_THD x 2 (reg_miu128b=1). = DMA_THD x 4 (reg_miu128b=0).	
14h (101429h)	**REG101429**	**7:0**	**Default : 0x22**	**Access : R/W**
	FORCE_HIGH	7	Force DMA High priority.	
	HI_TSH[3:0]	6:3	DMA High priority threshold (assert high priority if data count less then HI_TSH x 8).	
	BURST_EXT[2:0]	2:0	DMA burst length. 0: 4 (reg_miu128b=1), 8 (reg_miu128b=0). 1: 8 (reg_miu128b=1), 16 (reg_miu128b=0). 2: 16 (reg_miu128b=1), 32 (reg_miu128b=0). 3: 24 (reg_miu128b=1), 48 (reg_miu128b=0). 4: 32 (reg_miu128b=1), 64 (reg_miu128b=0). 5: 48 (reg_miu128b=1), 96 (reg_miu128b=0). 6: 64 (reg_miu128b=1),128 (reg_miu128b=0). 7: All.	
18h (101430h)	**REG101430**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DC_STRIP_H[2:0]	2:0	DC_STRIP_H[2:0] = reg_dc_strip[10:8].	
1Fh (10143Eh)	**REG10143E**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	FLD_INT_MASK	5	DC Field change interrupt mask. 1: Disable/clear. 0: Enable.	
	RDY_INT_MASK	4	DC RDY interrupt mask. 1: Disable/clear. 0: Enable.	
	HS_INT_MASK	3	DC2MA Hsync interrupt mask. 1: Disable/clear. 0: Enable.	
	VS_INT_MASK	2	DC2MA Vsync interrupt mask. 1: Disable/clear. 0: Enable.	
	OF_INT_MASK	1	DC buffer overflow interrupt mask. 1: Disable/clear. 0: Enable.	

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	UF_INT_MASK	0	DC buffer underflow interrupt mask. 1: Disable/clear. 0: Enable.	
1Fh (10143Fh)	**REG10143F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FLD_INT	5	DC Field change interrupt.	
	RDY_INT	4	DC RDY interrupt.	
	HS_INT	3	DC Hsync interrupt.	
	VS_INT	2	DC Vsync interrupt.	
	OF_INT	1	DC buffer overflow interrupt.	
	UF_INT	0	DC buffer underflow interrupt.	
20h (101440h)	**REG101440**	**7:0**	**Default : 0x00**	**Access : R/W**
	422PACK	7	YUV422 pack mode (*).	
	-	6	Reserved.	
	DRAM_RD_MD	5	DRAM data read out address mode(*). 0: Jump 32(PAGE_HEIGHT) after each access. 1: Continuous read out.	
	IMG422	4	0: YUV420. 1: YUV422 (*).	
	-	3	Reserved.	
	PRO_SEQ	2	1: Progressive frame. 0: Interlace frame. For DC_MD = 2 only(*).	
	DC_MD[1:0]	1:0	DC mode(*). 00: Hardwire mode (MVD). 01: Hardwire Clip mode (MVD). 10: MCU control mode (M4VD, JPG). 11: Reserved.	
20h (101441h)	**REG101441**	**7:0**	**Default : 0x5A**	**Access : R/W**
	DC_STRIP[7:0]	7:0	DC_STRIP valid at REG_DC_MD = 2 or 3. If (reg_dram_rd_md==0). DC_STRIP = DRAM H size (pixel) / 8; Else DC_STRIP = DRAM H size (pixel) / 4; (*).	
21h	**REG101442**	**7:0**	**Default : 0x00**	**Access : R/W**

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101442h)	Y_START[7:0]	7:0	REG_DC_MD=1: Y offset for the first Y address. REG_DC_MD=2: Y Start address. (*) (Unit: 1 word).	
21h (101443h)	**REG101443**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_START[15:8]	7:0	See description of '101442h'.	
22h (101444h)	**REG101444**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_START[23:16]	7:0	See description of '101442h'.	
22h (101445h)	**REG101445**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	Y_START[28:24]	4:0	See description of '101442h'.	
23h (101446h)	**REG101446**	**7:0**	**Default : 0x80**	**Access : R/W**
	UV_START[7:0]	7:0	REG_DC_MD=1: UV offset for the first UV address. REG_DC_MD=2: UV Start address. (*) (Unit: 1 word).	
23h (101447h)	**REG101447**	**7:0**	**Default : 0xCA**	**Access : R/W**
	UV_START[15:8]	7:0	See description of '101446h'.	
24h (101448h)	**REG101448**	**7:0**	**Default : 0x00**	**Access : R/W**
	UV_START[23:16]	7:0	See description of '101446h'.	
24h (101449h)	**REG101449**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	UV_START[28:24]	4:0	See description of '101446h'.	
25h (10144Ah)	**REG10144A**	**7:0**	**Default : 0x20**	**Access : R/W**
	HSIZE[7:0]	7:0	Display Image H size (unit: 1 pixel) when DC_MD =1, 2, 3 (*).	
25h (10144Bh)	**REG10144B**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:5	Reserved.	
	HSIZE[12:8]	4:0	See description of '10144Ah'.	
26h (10144Ch)	**REG10144C**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSIZE[7:0]	7:0	Display Image V size (unit: 1 pixel) when DC_MD =1, 2, 3 (*).	
26h (10144Dh)	**REG10144D**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	VSIZE[12:8]	4:0	See description of '10144Ch'.	
27h	**REG10144E**	**7:0**	**Default : 0x00**	**Access : R/W**

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10144Eh)	-	7:5	Reserved.	
	FWR	4	Force load registers in.	
	-	3:2	Reserved.	
	H264ORDER	1	DRAM H264 frame order read out.	
	DC_WR	0	Load new value into active registers 0x20-0x26.	
27h (10144Fh)	**REG10144F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OLD_IMG_HSTR	2	Old horizontal image start.	
	-	1:0	Reserved.	
28h (101451h)	**REG101451**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	HVD_EN	3	Switch MVD interface to H264 interface.	
	-	2	Reserved.	
	H264_PUREY	1	Mono mode (Chroma value is fixed).	
	MVD_EN	0	Switch MVD interface to MVD interface.	
29h (101452h)	**REG101452**	**7:0**	**Default : 0x08**	**Access : R/W**
	RAMAP_LUMA_EN	7	Enable Luma range mapping for VC1.	
	-	6:5	Reserved.	
	RAMAP_LUMA[4:0]	4:0	Luma range mapping for VC1 (value = 8~16).	
29h (101453h)	**REG101453**	**7:0**	**Default : 0x08**	**Access : R/W**
	RAMAP_CHROMA_EN	7	Enable Chroma range mapping for VC1.	
	-	6:5	Reserved.	
	RAMAP_CHROMA[4:0]	4:0	Chroma range mapping for VC1 (value = 8~16).	
30h (101460h)	**REG101460**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	UV_SHT_FLD1	1	0: Normal mode. 1: UV shift one line mode for field 1.	
	UV_SHT_FLD0	0	0: Normal mode. 1: UV shift one line mode for field 0.	
30h (101460h)	**REG101460**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_REQ_DISABLE	6	0: Normal mvop to miu access. 1: Disable mvop to miu access.	
	DC2MI_128B_I64	5	0: Use MIU group1 128bit bus. 1: Use MIU group1 64bit bus.	

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MIU128B	4	0: Use MIU group2 64bit bus. 1: Use MIU group1 128bit bus.	
	GCLK_VCLK_ON	3	0: Clk_dc0 use free-run clock. 1: Clk_dc0 use gated clock.	
	GCLK_MIU_ON	2	0: Clk_miu use free-run clock. 1: Clk_miu use gated clock.	
31h (101462h)	**REG101462**	**7:0**	**Default : 0x01**	**Access : R/W**
	Y_START1[7:0]	7:0	Bottom Field Y Start address when DC_MD=3 or dual_buffer mode (unit: 1 word)(*).	
31h (101463h)	**REG101463**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_START1[15:8]	7:0	See description of '101462h'.	
32h (101464h)	**REG101464**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_START1[23:16]	7:0	See description of '101462h'.	
32h (101465h)	**REG101465**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	Y_START1[28:24]	4:0	See description of '101462h'.	
33h (101466h)	**REG101466**	**7:0**	**Default : 0x80**	**Access : R/W**
	UV_START1[7:0]	7:0	Bottom Field UV Start address when DC_MD=3 or dual_buffer mode (unit: 1 word)(*).	
33h (101467h)	**REG101467**	**7:0**	**Default : 0xCA**	**Access : R/W**
	UV_START1[15:8]	7:0	See description of '101466h'.	
34h (101468h)	**REG101468**	**7:0**	**Default : 0x00**	**Access : R/W**
	UV_START1[23:16]	7:0	See description of '101466h'.	
34h (101469h)	**REG101469**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	UV_START1[28:24]	4:0	See description of '101466h'.	
35h (10146Ah)	**REG10146A**	**7:0**	**Default : 0x58**	**Access : R/W**
	SYNC_FRAME_V[7:0]	7:0	Frame vertical total line for frame sync function. (Count from 1, unit: 1 line; include blanking, top and bottom field).	
35h (10146Bh)	**REG10146B**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	SYNC_FRAME_V[12:8]	4:0	See description of '10146Ah'.	
36h	**REG10146C**	**7:0**	**Default : 0x20**	**Access : R/W**

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10146Ch)	SYNC_FRAME_H[7:0]	7:0	Line pixel total count for frame sync function. (Count from 1, unit:1 pixel; include H blanking).	
36h (10146Dh)	**REG10146D**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:5	Reserved.	
	SYNC_FRAME_H[12:8]	4:0	See description of '10146Ch'.	
37h (10146Fh)	**REG10146F**	**7:0**	**Default : 0x00**	**Access : R/W**
	INST_BLANK_VSIZE[7:0]	7:0	Insert vblank size after first View of 3D L/R mode.	
38h (101470h)	**REG101470**	**7:0**	**Default : 0xFF**	**Access : R/W**
	INFO_FROM_CODEC[7:0]	7:0	[0]: Base address. [1]: Pitch. [2]: Size. [3]: Progressive sequence. [4]: Field. [5]: Range map. [6]: Compression mode. [7]: 422 format. [8]: Dual buffer flag. [9]: Bpic reduction. [10]: Second buffer pitch. [11]: Second buffer size.	
38h (101471h)	**REG101471**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	INFO_FROM_CODEC[11:8]	3:0	See description of '101470h'.	
3Bh (101476h)	**REG101476**	**7:0**	**Default : 0x08**	**Access : R/W**
	MASK_BASE_LSB	7	Mask LSB of base address from Codec,(always get top field base address).	
	HW_422_BASE	6	Hardware calculate 422 2nd base address.	
	HW_FLD_BASE	5	Hardware calculate field jump base address.	
	HW_MIR_BASE	4	Hardware calculate mirror/flip base address.	
	FIELD_FROM_ADDR	3	Field info from mvd2dc base address LSB.	
	-	2	Reserved.	
	HMIR	1	Enable horizontall mirror.	
	VMIR	0	Enable vertical mirror.	
3Bh (101477h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Bh (101477h)	**REG101477**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	REF_SELF_FLD	1	Source field flag set by internal timing generator.	
	DC2MVD_FLD_SEL	0	Select dc2mvd field.	
3Ch (101478h)	**REG101478**	**7:0**	**Default : 0x00**	**Access : R/W**
	LR_DIFF_SIZE	7	3D L/R dual buffer with difference size.	
	EXTFLD_DIP	6	Use DIP field as external input field.	
	DIP_CLIP_MD	5	Clipping mode of DIP source (only work while reg_base_from_xc = 1).	
	BASE_FROM_DIP	4	Source buffer address is from DIP.	
	LR_LA2SBS	3	3D L/R dual buffer side by side output.	
	LR_LA_OUT	2	3D L/R dual buffer line alternative output.	
	P2I_MODE	1	Progressive source but interlace output mode.(to SC vsync is twice of to MVD vsync).	
	LR_BUF_MODE	0	3D L/R dual buffer mode.	
3Ch (101479h)	**REG101479**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RGB_FMT[1:0]	1:0	Source is RGB format : [0]=1 : RGB 565. [1]=1 : RGB 888.	
3Dh (10147Ah)	**REG10147A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_3D[7:0]	7:0	Dummy register.	
3Dh (10147Bh)	REG10147B	7:0	Default : 0x00	Access : R/W
	DUMMY_3D[15:8]	7:0	See description of '10147Ah'.	
3Eh (10147Ch)	**REG10147C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	VSYNC_FROM_SC	2	Vsync from Scaler.	
	TRIG_FROM_SC	1	Trigger start from Scaler.	
	HANDSHAKE_MD	0	Handshake output interface.	
3Eh (10147Dh)	**REG10147D**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	BLANK_CNT[3:0]	3:0	Horizontal blanking cycle of handshaking mode (x16).	
3Fh (10147Eh)	**REG10147E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_EN	7	Yuv to rgb CSC enable.	

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MVOP Register (Bank = 1014)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:3	Reserved.	
	WEIGHT_MD	2	Chroma weighting mode: (*). 0: U0, (3u0+u2)/4, (u0+3u2)/4, (3u2+u4)/4. 1: U0, (u0+u2)/2, u2, (u2+u4)/2.	
	WEIGHT_OFF	1	Chroma weighting off (*).	
	STRIP_ALIGN	0	Strip length alignment (*). 0: X1. 1: X2.	
3Fh (10147Fh)	**REG10147F**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FRAME_RST	7	Use frame sync (CLK_DC1 domain) to reset CLK_DC0 and CLK_MIU domain every frame.	
	-	6:0	Reserved.	
3Fh (10147Fh)	**REG10147F**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FIX_8PIX_ALIGN	6	1: Fix Horizontal 8-pixel alignment bug. 0: Use original design.	

SEMAPH Register (Bank = 1018)

SEMAPH Register (Bank = 1018)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101800h)	**REG101800**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_0[7:0]	7:0	SEMA_0[15:2]. Reserve. SEMA_0[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	
00h (101801h)	**REG101801**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_0[15:8]	7:0	See description of '101800h'.	
01h	**REG101802**	**7:0**	**Default : 0x00**	**Access : R/W**

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SEMAPH Register (Bank = 1018)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101802h)	SEMA_1[7:0]	7:0	SEMA_1[15:2]. Reserve. SEMA_1[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	
01h (101803h)	**REG101803**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_1[15:8]	7:0	See description of '101802h'.	
02h (101804h)	**REG101804**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_2[7:0]	7:0	SEMA_2[15:2]. Reserve. SEMA_2[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	
02h (101805h)	**REG101805**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_2[15:8]	7:0	See description of '101804h'.	
03h (101806h)	**REG101806**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_3[7:0]	7:0	SEMA_3[15:2]. Reserve. SEMA_3[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	
03h (101807h)	**REG101807**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_3[15:8]	7:0	See description of '101806h'.	
04h (101808h)	**REG101808**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_4[7:0]	7:0	SEMA_4[15:2]. Reserve. SEMA_4[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	

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SEMAPH Register (Bank = 1018)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (101809h)	**REG101809**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_4[15:8]	7:0	See description of '101808h'.	
05h (10180Ah)	**REG10180A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_5[7:0]	7:0	SEMA_5[15:2]. Reserve. SEMA_5[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	
05h (10180Bh)	**REG10180B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_5[15:8]	7:0	See description of '10180Ah'.	
06h (10180Ch)	**REG10180C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_6[7:0]	7:0	SEMA_6[15:2]. Reserve. SEMA_6[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	
06h (10180Dh)	**REG10180D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_6[15:8]	7:0	See description of '10180Ch'.	
07h (10180Eh)	**REG10180E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_7[7:0]	7:0	SEMA_7[15:2]. Reserve. SEMA_7[1:0]. 2'b00 :clear. 2'b01 :ID1. 2'b10 :ID2. 2'b11 :ID3.	
07h (10180Fh)	**REG10180F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_7[15:8]	7:0	See description of '10180Eh'.	

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MAU0 Register (Bank = 1018)

MAU0 Register (Bank = 1018)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (101840h)	**REG101840**	**7:0**	**Default : 0x10**	**Access : R/W**
	BURST_EN	7	Enable of burst-cascade function. 0: Disable. 1: Enable.	
	-	6:5	Reserved.	
	BURST_LENGTH[4:0]	4:0	Burst length of burst-cascade function.	
20h (101841h)	**REG101841**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	RQ_LENGTH[4:0]	4:0	The maximal length of continuous request. For single master.	
21h (101842h)	**REG101842**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MST3_RD_BLOCK_WR_EN	3	MST3 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST2_RD_BLOCK_WR_EN	2	MST2 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST1_RD_BLOCK_WR_EN	1	MST1 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST0_RD_BLOCK_WR_EN	0	MST0 enable of RD block WR function. 0: Disable. 1: Enable.	
21h (101843h)	**REG101843**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MIU0_SIZE	0	MIU0 size. It's for continuous address mapping when miu0 size is smaller than the maximum of one miu entry. 0: 64MB. 1: 128MB.	
22h (101844h)	**REG101844**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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MAU0 Register (Bank = 1018)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SW_RST	0	S/W reset of all MAU. 0: Not reset. 1: Reset.	
2Ch (101858h)	**REG101858**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV0[7:0]	7:0	Reserved register 0.	
2Ch (101859h)	**REG101859**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV0[15:8]	7:0	See description of '101858h'.	
2Dh (10185Ah)	**REG10185A**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV1[7:0]	7:0	Reserved register 1.	
2Dh (10185Bh)	**REG10185B**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV1[15:8]	7:0	See description of '10185Ah'.	
2Eh (10185Ch)	**REG10185C**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV2[7:0]	7:0	Reserved register 2.	
2Eh (10185Dh)	**REG10185D**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV2[15:8]	7:0	See description of '10185Ch'.	
2Fh (10185Eh)	**REG10185E**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV3[7:0]	7:0	Reserved register 3.	
2Fh (10185Fh)	**REG10185F**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV3[15:8]	7:0	See description of '10185Eh'.	

INTR_CTRL Register (Bank = 1019)

INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101900h)	**REG101900**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst0; 0/1 : not force/force.	
00h (101901h)	**REG101901**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_15_0_[15:8]	7:0	See description of '101900h'.	
01h (101902h)	**REG101902**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst0; 0/1 : not force/force.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (101903h)	**REG101903**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_31_16_[15:8]	7:0	See description of '101902h'.	
02h (101904h)	**REG101904**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst0; 0/1 : not force/force.	
02h (101905h)	**REG101905**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_47_32_[15:8]	7:0	See description of '101904h'.	
03h (101906h)	**REG101906**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst0; 0/1 : not force/force.	
03h (101907h)	**REG101907**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_FORCE_63_48_[15:8]	7:0	See description of '101906h'.	
04h (101908h)	**REG101908**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst0; 0/1: not mask/mask.	
04h (101909h)	**REG101909**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_15_0_[15:8]	7:0	See description of '101908h'.	
05h (10190Ah)	**REG10190A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst0; 0/1: not mask/mask.	
05h (10190Bh)	**REG10190B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_31_16_[15:8]	7:0	See description of '10190Ah'.	
06h (10190Ch)	**REG10190C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst0; 0/1: not mask/mask.	
06h (10190Dh)	**REG10190D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_47_32_[15:8]	7:0	See description of '10190Ch'.	
07h (10190Eh)	**REG10190E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst0; 0/1: not mask/mask.	
07h (10190Fh)	**REG10190F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_63_48_[15:8]	7:0	See description of '10190Eh'.	
08h	**REG101910**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101910h)	HST0_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
08h (101911h)	**REG101911**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '101910h'.	
09h (101912h)	**REG101912**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst0; 0/1: not reverse/reverse.	
09h (101913h)	**REG101913**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '101912h'.	
0Ah (101914h)	**REG101914**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst0; 0/1: not reverse/reverse.	
0Ah (101915h)	**REG101915**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '101914h'.	
0Bh (101916h)	**REG101916**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst0; 0/1: not reverse/reverse.	
0Bh (101917h)	**REG101917**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '101916h'.	
0Ch (101918h)	**REG101918**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst0; Write 1 to clear fiq interrupt[15:0] of hst0.	
0Ch (101919h)	**REG101919**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_15_0_[15:8]	7:0	See description of '101918h'.	
0Dh (10191Ah)	**REG10191A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst0; Write 1 to clear fiq interrupt[31:16] of hst0.	
0Dh (10191Bh)	**REG10191B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_31_16_[15:8]	7:0	See description of '10191Ah'.	
0Eh (10191Ch)	**REG10191C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst0; Write 1 to clear fiq interrupt[47:32] of hst0.	
0Eh (10191Dh)	**REG10191D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_47_32_[15:8]	7:0	See description of '10191Ch'.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (10191Eh)	**REG10191E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst0; Write 1 to clear fiq interrupt[63:48] of hst0.	
0Fh (10191Fh)	**REG10191F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_63_48_[15:8]	7:0	See description of '10191Eh'.	
10h (101920h)	**REG101920**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst0; 0/1 : not force/force.	
10h (101921h)	**REG101921**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_15_0_[15:8]	7:0	See description of '101920h'.	
11h (101922h)	**REG101922**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst0; 0/1 : not force/force.	
11h (101923h)	**REG101923**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_31_16_[15:8]	7:0	See description of '101922h'.	
12h (101924h)	**REG101924**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst0; 0/1 : not force/force.	
12h (101925h)	**REG101925**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_47_32_[15:8]	7:0	See description of '101924h'.	
13h (101926h)	**REG101926**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst0; 0/1 : not force/force.	
13h (101927h)	**REG101927**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_FORCE_63_48_[15:8]	7:0	See description of '101926h'.	
14h (101928h)	**REG101928**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst0; 0/1: not mask/mask.	
14h (101929h)	**REG101929**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_15_0_[15:8]	7:0	See description of '101928h'.	
15h (10192Ah)	**REG10192A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst0; 0/1: not mask/mask.	
15h	**REG10192B**	**7:0**	**Default : 0xFF**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10192Bh)	HST0_IRQ_MASK_31_16_[15:8]	7:0	See description of '10192Ah'.	
16h (10192Ch)	**REG10192C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst0; 0/1: not mask/mask.	
16h (10192Dh)	**REG10192D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_47_32_[15:8]	7:0	See description of '10192Ch'.	
17h (10192Eh)	**REG10192E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst0; 0/1: not mask/mask.	
17h (10192Fh)	**REG10192F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_63_48_[15:8]	7:0	See description of '10192Eh'.	
18h (101930h)	**REG101930**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
18h (101931h)	**REG101931**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '101930h'.	
19h (101932h)	**REG101932**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst0; 0/1: not reverse/reverse.	
19h (101933h)	**REG101933**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '101932h'.	
1Ah (101934h)	**REG101934**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst0; 0/1: not reverse/reverse.	
1Ah (101935h)	**REG101935**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '101934h'.	
1Bh (101936h)	**REG101936**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst0; 0/1: not reverse/reverse.	
1Bh (101937h)	**REG101937**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '101936h'.	
1Ch (101938h)	**REG101938**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst0;	
1Ch	**REG101939**	**7:0**	**Default : 0x00**	**Access : RO**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101939h)	HST0_IRQ_STATUS_15_0_[15:8]	7:0	See description of '101938h'.	
1Dh (10193Ah)	**REG10193A**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst0;	
1Dh (10193Bh)	**REG10193B**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_31_16_[15:8]	7:0	See description of '10193Ah'.	
1Eh (10193Ch)	**REG10193C**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst0;	
1Eh (10193Dh)	**REG10193D**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_47_32_[15:8]	7:0	See description of '10193Ch'.	
1Fh (10193Eh)	**REG10193E**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst0;	
1Fh (10193Fh)	**REG10193F**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_63_48_[15:8]	7:0	See description of '10193Eh'.	
20h (101940h)	**REG101940**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst1; 0/1 : not force/force.	
20h (101941h)	**REG101941**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_15_0_[15:8]	7:0	See description of '101940h'.	
21h (101942h)	**REG101942**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst1; 0/1 : not force/force.	
21h (101943h)	**REG101943**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_31_16_[15:8]	7:0	See description of '101942h'.	
22h (101944h)	**REG101944**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst1; 0/1 : not force/force.	
22h (101945h)	**REG101945**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_47_32_[15:8]	7:0	See description of '101944h'.	
23h (101946h)	**REG101946**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst1; 0/1 : not force/force.	
23h (101947h)	**REG101947**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_FORCE_63_48_[15:8]	7:0	See description of '101946h'.	
24h	**REG101948**	**7:0**	**Default : 0xFF**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101948h)	HST1_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst1; 0/1: not mask/mask.	
24h (101949h)	**REG101949**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_15_0_[15:8]	7:0	See description of '101948h'.	
25h (10194Ah)	**REG10194A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst1; 0/1: not mask/mask.	
25h (10194Bh)	**REG10194B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_31_16_[15:8]	7:0	See description of '10194Ah'.	
26h (10194Ch)	**REG10194C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst1; 0/1: not mask/mask.	
26h (10194Dh)	**REG10194D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_47_32_[15:8]	7:0	See description of '10194Ch'.	
27h (10194Eh)	**REG10194E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst1; 0/1: not mask/mask.	
27h (10194Fh)	**REG10194F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_63_48_[15:8]	7:0	See description of '10194Eh'.	
28h (101950h)	**REG101950**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst1; 0/1: not reverse/reverse.	
28h (101951h)	**REG101951**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '101950h'.	
29h (101952h)	**REG101952**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst1; 0/1: not reverse/reverse.	
29h (101953h)	**REG101953**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '101952h'.	
2Ah (101954h)	**REG101954**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst1; 0/1: not reverse/reverse.	
2Ah (101955h)	**REG101955**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '101954h'.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Bh (101956h)	**REG101956**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst1; 0/1: not reverse/reverse.	
2Bh (101957h)	**REG101957**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '101956h'.	
2Ch (101958h)	**REG101958**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst1; Write 1 to clear fiq interrupt[15:0] of hst1.	
2Ch (101959h)	**REG101959**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_15_0_[15:8]	7:0	See description of '101958h'.	
2Dh (10195Ah)	**REG10195A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst1; Write 1 to clear fiq interrupt[31:16] of hst1.	
2Dh (10195Bh)	**REG10195B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_31_16_[15:8]	7:0	See description of '10195Ah'.	
2Eh (10195Ch)	**REG10195C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst1; Write 1 to clear fiq interrupt[47:32] of hst1.	
2Eh (10195Dh)	**REG10195D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_47_32_[15:8]	7:0	See description of '10195Ch'.	
2Fh (10195Eh)	**REG10195E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst1; Write 1 to clear fiq interrupt[63:48] of hst1.	
2Fh (10195Fh)	**REG10195F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_63_48_[15:8]	7:0	See description of '10195Eh'.	
30h (101960h)	**REG101960**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst1; 0/1 : not force/force.	
30h (101961h)	**REG101961**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_15_0_[15:8]	7:0	See description of '101960h'.	
31h (101962h)	**REG101962**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst1; 0/1 : not force/force.	
31h	**REG101963**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101963h)	HST1_IRQ_FORCE_31_16_[15:8]	7:0	See description of '101962h'.	
32h (101964h)	**REG101964**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst1; 0/1 : not force/force.	
32h (101965h)	**REG101965**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_47_32_[15:8]	7:0	See description of '101964h'.	
33h (101966h)	**REG101966**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst1; 0/1 : not force/force.	
33h (101967h)	**REG101967**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_FORCE_63_48_[15:8]	7:0	See description of '101966h'.	
34h (101968h)	**REG101968**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst1; 0/1: not mask/mask.	
34h (101969h)	**REG101969**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_15_0_[15:8]	7:0	See description of '101968h'.	
35h (10196Ah)	**REG10196A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst1; 0/1: not mask/mask.	
35h (10196Bh)	**REG10196B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_31_16_[15:8]	7:0	See description of '10196Ah'.	
36h (10196Ch)	**REG10196C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst1; 0/1: not mask/mask.	
36h (10196Dh)	**REG10196D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_47_32_[15:8]	7:0	See description of '10196Ch'.	
37h (10196Eh)	**REG10196E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst1; 0/1: not mask/mask.	
37h (10196Fh)	**REG10196F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_63_48_[15:8]	7:0	See description of '10196Eh'.	
38h (101970h)	**REG101970**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst1; 0/1: not reverse/reverse.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (101971h)	**REG101971**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '101970h'.	
39h (101972h)	**REG101972**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst1; 0/1: not reverse/reverse.	
39h (101973h)	**REG101973**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '101972h'.	
3Ah (101974h)	**REG101974**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst1; 0/1: not reverse/reverse.	
3Ah (101975h)	**REG101975**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '101974h'.	
3Bh (101976h)	**REG101976**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst1; 0/1: not reverse/reverse.	
3Bh (101977h)	**REG101977**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '101976h'.	
3Ch (101978h)	**REG101978**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst1;	
3Ch (101979h)	**REG101979**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_15_0_[15:8]	7:0	See description of '101978h'.	
3Dh (10197Ah)	**REG10197A**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst1;	
3Dh (10197Bh)	**REG10197B**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_31_16_[15:8]	7:0	See description of '10197Ah'.	
3Eh (10197Ch)	**REG10197C**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst1;	
3Eh (10197Dh)	**REG10197D**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_47_32_[15:8]	7:0	See description of '10197Ch'.	
3Fh (10197Eh)	**REG10197E**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst1;	
3Fh (10197Fh)	**REG10197F**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_63_48_[15:8]	7:0	See description of '10197Eh'.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (101980h)	**REG101980**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst2; 0/1 : not force/force.	
40h (101981h)	**REG101981**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_15_0_[15:8]	7:0	See description of '101980h'.	
41h (101982h)	**REG101982**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst2; 0/1 : not force/force.	
41h (101983h)	**REG101983**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_31_16_[15:8]	7:0	See description of '101982h'.	
42h (101984h)	**REG101984**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst2; 0/1 : not force/force.	
42h (101985h)	**REG101985**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_47_32_[15:8]	7:0	See description of '101984h'.	
43h (101986h)	**REG101986**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst2; 0/1 : not force/force.	
43h (101987h)	**REG101987**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_FORCE_63_48_[15:8]	7:0	See description of '101986h'.	
44h (101988h)	**REG101988**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst2; 0/1: not mask/mask.	
44h (101989h)	**REG101989**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_15_0_[15:8]	7:0	See description of '101988h'.	
45h (10198Ah)	**REG10198A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst2; 0/1: not mask/mask.	
45h (10198Bh)	**REG10198B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_31_16_[15:8]	7:0	See description of '10198Ah'.	
46h (10198Ch)	**REG10198C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst2; 0/1: not mask/mask.	
46h	**REG10198D**	**7:0**	**Default : 0xFF**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10198Dh)	HST2_FIQ_MASK_47_32_[15:8]	7:0	See description of '10198Ch'.	
47h (10198Eh)	**REG10198E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst2; 0/1: not mask/mask.	
47h (10198Fh)	**REG10198F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_63_48_[15:8]	7:0	See description of '10198Eh'.	
48h (101990h)	**REG101990**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst2; 0/1: not reverse/reverse.	
48h (101991h)	**REG101991**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '101990h'.	
49h (101992h)	**REG101992**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst2; 0/1: not reverse/reverse.	
49h (101993h)	**REG101993**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '101992h'.	
4Ah (101994h)	**REG101994**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst2; 0/1: not reverse/reverse.	
4Ah (101995h)	**REG101995**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '101994h'.	
4Bh (101996h)	**REG101996**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst2; 0/1: not reverse/reverse.	
4Bh (101997h)	**REG101997**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '101996h'.	
4Ch (101998h)	**REG101998**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst2; Write 1 to clear fiq interrupt[15:0] of hst2.	
4Ch (101999h)	**REG101999**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_15_0_[15:8]	7:0	See description of '101998h'.	
4Dh (10199Ah)	**REG10199A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst2; Write 1 to clear fiq interrupt[31:16] of hst2.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Dh (10199Bh)	**REG10199B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_31_16_[15:8]	7:0	See description of '10199Ah'.	
4Eh (10199Ch)	**REG10199C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst2; Write 1 to clear fiq interrupt[47:32] of hst2.	
4Eh (10199Dh)	**REG10199D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_47_32_[15:8]	7:0	See description of '10199Ch'.	
4Fh (10199Eh)	**REG10199E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst2; Write 1 to clear fiq interrupt[63:48] of hst2.	
4Fh (10199Fh)	**REG10199F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_63_48_[15:8]	7:0	See description of '10199Eh'.	
50h (1019A0h)	**REG1019A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst2; 0/1 : not force/force.	
50h (1019A1h)	**REG1019A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_15_0_[15:8]	7:0	See description of '1019A0h'.	
51h (1019A2h)	**REG1019A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst2; 0/1 : not force/force.	
51h (1019A3h)	**REG1019A3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_31_16_[15:8]	7:0	See description of '1019A2h'.	
52h (1019A4h)	**REG1019A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst2; 0/1 : not force/force.	
52h (1019A5h)	**REG1019A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_47_32_[15:8]	7:0	See description of '1019A4h'.	
53h (1019A6h)	**REG1019A6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst2; 0/1 : not force/force.	
53h (1019A7h)	**REG1019A7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_FORCE_63_48_[15:8]	7:0	See description of '1019A6h'.	
54h	**REG1019A8**	**7:0**	**Default : 0xFF**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1019A8h)	HST2_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst2; 0/1: not mask/mask.	
54h (1019A9h)	**REG1019A9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_15_0_[15:8]	7:0	See description of '1019A8h'.	
55h (1019AAh)	**REG1019AA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst2; 0/1: not mask/mask.	
55h (1019ABh)	**REG1019AB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_31_16_[15:8]	7:0	See description of '1019AAh'.	
56h (1019ACh)	**REG1019AC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst2; 0/1: not mask/mask.	
56h (1019ADh)	**REG1019AD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_47_32_[15:8]	7:0	See description of '1019ACh'.	
57h (1019AEh)	**REG1019AE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst2; 0/1: not mask/mask.	
57h (1019AFh)	**REG1019AF**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_63_48_[15:8]	7:0	See description of '1019AEh'.	
58h (1019B0h)	**REG1019B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst2; 0/1: not reverse/reverse.	
58h (1019B1h)	**REG1019B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '1019B0h'.	
59h (1019B2h)	**REG1019B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst2; 0/1: not reverse/reverse.	
59h (1019B3h)	**REG1019B3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '1019B2h'.	
5Ah (1019B4h)	**REG1019B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst2; 0/1: not reverse/reverse.	
5Ah (1019B5h)	**REG1019B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '1019B4h'.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Bh (1019B6h)	**REG1019B6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst2; 0/1: not reverse/reverse.	
5Bh (1019B7h)	**REG1019B7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '1019B6h'.	
5Ch (1019B8h)	**REG1019B8**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst2;	
5Ch (1019B9h)	**REG1019B9**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_15_0_[15:8]	7:0	See description of '1019B8h'.	
5Dh (1019BAh)	**REG1019BA**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst2;	
5Dh (1019BBh)	**REG1019BB**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_31_16_[15:8]	7:0	See description of '1019BAh'.	
5Eh (1019BCh)	**REG1019BC**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst2;	
5Eh (1019BDh)	**REG1019BD**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_47_32_[15:8]	7:0	See description of '1019BCh'.	
5Fh (1019BEh)	**REG1019BE**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst2;	
5Fh (1019BFh)	**REG1019BF**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_63_48_[15:8]	7:0	See description of '1019BEh'.	
60h (1019C0h)	**REG1019C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst3; 0/1 : not force/force.	
60h (1019C1h)	**REG1019C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_15_0_[15:8]	7:0	See description of '1019C0h'.	
61h (1019C2h)	**REG1019C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst3; 0/1 : not force/force.	
61h (1019C3h)	**REG1019C3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_31_16_[15:8]	7:0	See description of '1019C2h'.	
62h (1019C4h)	**REG1019C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst3; 0/1 : not force/force.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (1019C5h)	**REG1019C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_47_32_[15:8]	7:0	See description of '1019C4h'.	
63h (1019C6h)	**REG1019C6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst3; 0/1 : not force/force.	
63h (1019C7h)	**REG1019C7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_FORCE_63_48_[15:8]	7:0	See description of '1019C6h'.	
64h (1019C8h)	**REG1019C8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst3; 0/1: not mask/mask.	
64h (1019C9h)	**REG1019C9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_15_0_[15:8]	7:0	See description of '1019C8h'.	
65h (1019CAh)	**REG1019CA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst3; 0/1: not mask/mask.	
65h (1019CBh)	**REG1019CB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_31_16_[15:8]	7:0	See description of '1019CAh'.	
66h (1019CCh)	**REG1019CC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst3; 0/1: not mask/mask.	
66h (1019CDh)	**REG1019CD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_47_32_[15:8]	7:0	See description of '1019CCh'.	
67h (1019CEh)	**REG1019CE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst3; 0/1: not mask/mask.	
67h (1019CFh)	**REG1019CF**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_63_48_[15:8]	7:0	See description of '1019CEh'.	
68h (1019D0h)	**REG1019D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst3; 0/1: not reverse/reverse.	
68h (1019D1h)	**REG1019D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '1019D0h'.	
69h	**REG1019D2**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1019D2h)	HST3_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst3; 0/1: not reverse/reverse.	
69h **(1019D3h)**	**REG1019D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '1019D2h'.	
6Ah **(1019D4h)**	**REG1019D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst3; 0/1: not reverse/reverse.	
6Ah **(1019D5h)**	**REG1019D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '1019D4h'.	
6Bh **(1019D6h)**	**REG1019D6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst3; 0/1: not reverse/reverse.	
6Bh **(1019D7h)**	**REG1019D7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '1019D6h'.	
6Ch **(1019D8h)**	**REG1019D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst3; Write 1 to clear fiq interrupt[15:0] of hst3.	
6Ch **(1019D9h)**	**REG1019D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_15_0_[15:8]	7:0	See description of '1019D8h'.	
6Dh **(1019DAh)**	**REG1019DA**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst3; Write 1 to clear fiq interrupt[31:16] of hst3.	
6Dh **(1019DBh)**	**REG1019DB**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_31_16_[15:8]	7:0	See description of '1019DAh'.	
6Eh **(1019DCh)**	**REG1019DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst3; Write 1 to clear fiq interrupt[47:32] of hst3.	
6Eh **(1019DDh)**	**REG1019DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_47_32_[15:8]	7:0	See description of '1019DCh'.	
6Fh **(1019DEh)**	**REG1019DE**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst3; Write 1 to clear fiq interrupt[63:48] of hst3.	
6Fh **(1019DFh)**	**REG1019DF**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_63_48_[15:8]	7:0	See description of '1019DEh'.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (1019E0h)	**REG1019E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst3; 0/1 : not force/force.	
70h (1019E1h)	**REG1019E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_15_0_[15:8]	7:0	See description of '1019E0h'.	
71h (1019E2h)	**REG1019E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst3; 0/1 : not force/force.	
71h (1019E3h)	**REG1019E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_31_16_[15:8]	7:0	See description of '1019E2h'.	
72h (1019E4h)	**REG1019E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst3; 0/1 : not force/force.	
72h (1019E5h)	**REG1019E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_47_32_[15:8]	7:0	See description of '1019E4h'.	
73h (1019E6h)	**REG1019E6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst3; 0/1 : not force/force.	
73h (1019E7h)	**REG1019E7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_FORCE_63_48_[15:8]	7:0	See description of '1019E6h'.	
74h (1019E8h)	**REG1019E8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst3; 0/1: not mask/mask.	
74h (1019E9h)	**REG1019E9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_15_0_[15:8]	7:0	See description of '1019E8h'.	
75h (1019EAh)	**REG1019EA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst3; 0/1: not mask/mask.	
75h (1019EBh)	**REG1019EB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_31_16_[15:8]	7:0	See description of '1019EAh'.	
76h (1019ECh)	**REG1019EC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst3; 0/1: not mask/mask.	
76h	**REG1019ED**	**7:0**	**Default : 0xFF**	**Access : R/W**

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1019EDh)	HST3_IRQ_MASK_47_32_[15:8]	7:0	See description of '1019ECh'.	
77h (1019EEh)	**REG1019EE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst3; 0/1: not mask/mask.	
77h (1019EFh)	**REG1019EF**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_63_48_[15:8]	7:0	See description of '1019EEh'.	
78h (1019F0h)	**REG1019F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst3; 0/1: not reverse/reverse.	
78h (1019F1h)	**REG1019F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '1019F0h'.	
79h (1019F2h)	**REG1019F2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst3; 0/1: not reverse/reverse.	
79h (1019F3h)	**REG1019F3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '1019F2h'.	
7Ah (1019F4h)	**REG1019F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst3; 0/1: not reverse/reverse.	
7Ah (1019F5h)	**REG1019F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '1019F4h'.	
7Bh (1019F6h)	**REG1019F6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst3; 0/1: not reverse/reverse.	
7Bh (1019F7h)	**REG1019F7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '1019F6h'.	
7Ch (1019F8h)	**REG1019F8**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst3;	
7Ch (1019F9h)	**REG1019F9**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_15_0_[15:8]	7:0	See description of '1019F8h'.	
7Dh (1019FAh)	**REG1019FA**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst3;	
7Dh (1019FBh)	**REG1019FB**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_31_16_[15:8]	7:0	See description of '1019FAh'.	

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INTR_CTRL Register (Bank = 1019)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Eh (1019FCh)	**REG1019FC**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst3;	
7Eh (1019FDh)	**REG1019FD**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_47_32_[15:8]	7:0	See description of '1019FCh'.	
7Fh (1019FEh)	**REG1019FE**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst3;	
7Fh (1019FFh)	**REG1019FF**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_63_48_[15:8]	7:0	See description of '1019FEh'.	

CHIPGPIO1 Register (Bank = 101A)

CHIPGPIO1 Register (Bank = 101A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101A00h)	**REG101A00**	**7:0**	**Default : 0x01**	**Access : R/W**
	EJ_CONFIG[0]	7	EJ_CONFIG.	
	DIGMIC_MODE[1:0]	6:5	DIGMIC_MODE.	
	CCIRIN_MODE	4	CCIRIN_MODE.	
	BTI2S_MODE[1:0]	3:2	BTI2S_MODE.	
	BT_MODE	1	BT_MODE.	
	ALL_PAD_IN	0	ALL_PAD_IN.	
00h (101A01h)	**REG101A01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FUART2_MODE	6	FUART2_MODE.	
	FUART1_MODE	5	FUART1_MODE.	
	EXTI2S_MODE[1:0]	4:3	EXTI2S_MODE.	
	-	2:1	Reserved.	
	EJ_CONFIG[1]	0	See description of '101A00h'.	
01h (101A02h)	**REG101A02**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCE1_MODE	7	NFCE1_MODE.	
	NF_MODE	6	NF_MODE.	
	MPIF_MODE[1:0]	5:4	MPIF_MODE.	
	I2CM1_MODE	3	I2CM1_MODE.	

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CHIPGPIO1 Register (Bank = 101A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	I2CM0_MODE	2	I2CM0_MODE.	
	GPSPWM1_MODE	1	GPSPWM1_MODE.	
	GPSPWM0_MODE	0	GPSPWM0_MODE.	
01h (101A03h)	**REG101A03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MPIFCS1_MODE	0	MPIFCS1_MODE.	
02h (101A04h)	**REG101A04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO2_MODE	4	SDIO2_MODE.	
	SDIO1_MODE[1:0]	3:2	SDIO1_MODE.	
	-	1	Reserved.	
	SDIO0_MODE	0	SDIO0_MODE.	
02h (101A05h)	**REG101A05**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWSPI_MODE	7	DWSPI_MODE.	
	SPDIFOUT_MODE	6	SPDIFOUT_MODE.	
	-	5:2	Reserved.	
	SENSOR1_MODE	1	SENSOR1_MODE.	
	SENSOR0_MODE	0	SENSOR0_MODE.	
03h (101A06h)	**REG101A06**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_IN_MODE	7	TEST_IN_MODE.	
	UART5_MODE	6	UART5_MODE.	
	UART4_MODE	5	UART4_MODE.	
	UART3_MODE	4	UART3_MODE.	
	UART2_MODE	3	UART2_MODE.	
	UART1_MODE	2	UART1_MODE.	
	-	1:0	Reserved.	
03h (101A07h)	**REG101A07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TEST_OUT_MODE[1:0]	1:0	TEST_OUT_MODE.	
04h (101A08h)	**REG101A08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GCR_SQR_LPF_BW_CTRL	4	GCR_SQR_LPF_BW_CTRL.	
	PD_LV_CLKSQR	3	PD_LV_CLKSQR.	

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CHIPGPIO1 Register (Bank = 101A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PD_HV_CLKSQR	2	PD_HV_CLKSQR.	
	PD_CLKSQR	1	PD_CLKSQR.	
	GCR_SQR_BYPASS	0	GCR_SQR_BYPASS.	
07h (101A0Eh)	**REG101A0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_SQR_PD_PASSWORD[7:0]	7:0	GCR_SQR_PD_PASSWORD.	
07h (101A0Fh)	**REG101A0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_SQR_PD_PASSWORD[15:8]	7:0	See description of '101A0Eh'.	
08h (101A10h)	**REG101A10**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_SQR_BP_PASSWORD[7:0]	7:0	GCR_SQR_BP_PASSWORD.	
08h (101A11h)	**REG101A11**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_SQR_BP_PASSWORD[15:8]	7:0	See description of '101A10h'.	
09h (101A12h)	**REG101A12**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_SQR_BW_PASSWORD[7:0]	7:0	GCR_SQR_BW_PASSWORD.	
09h (101A13h)	**REG101A13**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_SQR_BW_PASSWORD[15:8]	7:0	See description of '101A12h'.	
0Ah (101A14h)	**REG101A14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD2_DRV[7:0]	7:0	SD2_DRV.	
0Ah (101A15h)	**REG101A15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SD2_DRV[11:8]	3:0	See description of '101A14h'.	
0Bh (101A16h)	**REG101A16**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD2_PE[7:0]	7:0	SD2_PE.	
0Bh (101A17h)	**REG101A17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SD2_PE[11:8]	3:0	See description of '101A16h'.	
0Ch (101A18h)	**REG101A18**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD2_PS[7:0]	7:0	SD2_PS.	
0Ch (101A19h)	**REG101A19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SD2_PS[11:8]	3:0	See description of '101A18h'.	
0Dh (101A1Ah)	**REG101A1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD3_DRV[7:0]	7:0	SD3_DRV.	
0Dh	**REG101A1B**	**7:0**	**Default : 0x00**	**Access : R/W**

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CHIPGPIO1 Register (Bank = 101A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101A1Bh)	-	7:4	Reserved.	
	SD3_DRV[11:8]	3:0	See description of '101A1Ah'.	
0Eh (101A1Ch)	**REG101A1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD3_PE[7:0]	7:0	SD3_PE.	
0Eh (101A1Dh)	**REG101A1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SD3_PE[11:8]	3:0	See description of '101A1Ch'.	
0Fh (101A1Eh)	**REG101A1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD3_PS[7:0]	7:0	SD3_PS.	
0Fh (101A1Fh)	**REG101A1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SD3_PS[11:8]	3:0	See description of '101A1Eh'.	
10h (101A20h)	**REG101A20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	AGPSEVENT_MODE	6	AGPSEVENT_MODE.	
	SRDATA10B_MODE	5	SRDATA10B_MODE.	
	ISPI2CM_MODE	4	ISPI2CM_MODE.	
	DBBI2S_MODE[1:0]	3:2	DBBI2S_MODE.	
	XTLOUT_MODE	1	XTLOUT_MODE.	
	SPDIF_DRV	0	SPDIF_DRV.	
10h (101A21h)	**REG101A21**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	EMMC_MODE	5	EMMC_MODE.	
	SD3_BPS_MODE	4	SD3_BPS_MODE.	
	CA9_ONLY	3	CA9_ONLY.	
	SRCLKOUT_MODE	2	SRCLKOUT_MODE.	
	MCUJTAG_MODE[1:0]	1:0	MCUJTAG_MODE.	
11h (101A22h)	**REG101A22**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCON7_MODE	7	TCON7_MODE.	
	TCON6_MODE	6	TCON6_MODE.	
	TCON5_MODE	5	TCON5_MODE.	
	TCON4_MODE	4	TCON4_MODE.	
	TCON3_MODE	3	TCON3_MODE.	

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CHIPGPIO1 Register (Bank = 101A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TCON2_MODE	2	TCON2_MODE.	
	TCON1_MODE	1	TCON1_MODE.	
	TCON0_MODE	0	TCON0_MODE.	
12h (101A25h)	**REG101A25**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTINT7_MODE	7	EXTINT7_MODE.	
	EXTINT6_MODE	6	EXTINT6_MODE.	
	EXTINT5_MODE	5	EXTINT5_MODE.	
	EXTINT4_MODE	4	EXTINT4_MODE.	
	EXTINT3_MODE	3	EXTINT3_MODE.	
	EXTINT2_MODE	2	EXTINT2_MODE.	
	EXTINT1_MODE	1	EXTINT1_MODE.	
	EXTINT0_MODE	0	EXTINT0_MODE.	
13h (101A26h)	**REG101A26**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_ENABLE_B7	7	P1_ENABLE_B7.	
	P1_ENABLE_B6	6	P1_ENABLE_B6.	
	P1_ENABLE_B5	5	P1_ENABLE_B5.	
	P1_ENABLE_B4	4	P1_ENABLE_B4.	
	P1_ENABLE_B3	3	P1_ENABLE_B3.	
	P1_ENABLE_B2	2	P1_ENABLE_B2.	
	P1_ENABLE_B1	1	P1_ENABLE_B1.	
	P1_ENABLE_B0	0	P1_ENABLE_B0.	
14h (101A28h)	**REG101A28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	NF_BPS_MODE[7:0]	7:0	NF_BPS_MODE.	
14h (101A29h)	**REG101A29**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	NF_BPS_MODE[9:8]	1:0	See description of '101A28h'.	
15h (101A2Ah)	**REG101A2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPS_MODE	7	GPS_MODE.	
	GNS_MODE	6	GNS_MODE.	
	PWM5_MODE	5	PWM5_MODE.	
	PWM4_MODE	4	PWM4_MODE.	
	PWM3_MODE	3	PWM3_MODE.	
	PWM2_MODE	2	PWM2_MODE.	

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CHIPGPIO1 Register (Bank = 101A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM1_MODE	1	PWM1_MODE.	
	PWM0_MODE	0	PWM0_MODE.	
16h (101A2Ch)	**REG101A2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CCIRIN2_MODE	6	CCIRIN2_MODE.	
	TTLBG_MODE	5	TTLBG_MODE.	
	DWSPICZ_MODE	4	DWSPICZ_MODE.	
	TCK_MODE	3	TCK_MODE.	
	TTLHV_MODE	2	TTLHV_MODE.	
	NFCE3_MODE	1	NFCE3_MODE.	
	NFCE2_MODE	0	NFCE2_MODE.	
17h (101A2Eh)	**REG101A2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_DRV[7:0]	7:0	PAD_DRV.	
17h (101A2Fh)	**REG101A2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_DRV[15:8]	7:0	See description of '101A2Eh'.	
18h (101A30h)	**REG101A30**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_DRV[23:16]	7:0	See description of '101A2Eh'.	
18h (101A31h)	**REG101A31**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_DRV[31:24]	7:0	See description of '101A2Eh'.	
19h (101A32h)	**REG101A32**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_DRV[39:32]	7:0	See description of '101A2Eh'.	
19h (101A33h)	**REG101A33**	**7:0**	**Default : 0x55**	**Access : R/W**
	PAD_DRV[47:40]	7:0	See description of '101A2Eh'.	
1Ah (101A34h)	**REG101A34**	**7:0**	**Default : 0x55**	**Access : R/W**
	PAD_DRV[55:48]	7:0	See description of '101A2Eh'.	
1Ah (101A35h)	**REG101A35**	**7:0**	**Default : 0x55**	**Access : R/W**
	PAD_DRV[63:56]	7:0	See description of '101A2Eh'.	
1Bh (101A36h)	**REG101A36**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAD_PE[7:0]	7:0	PAD_PE.	
1Bh (101A37h)	**REG101A37**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAD_PE[15:8]	7:0	See description of '101A36h'.	
1Ch (101A38h)	**REG101A38**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAD_PE[23:16]	7:0	See description of '101A36h'.	

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CHIPGPIO1 Register (Bank = 101A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (101A39h)	**REG101A39**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PAD_PE[27:24]	3:0	See description of '101A36h'.	
1Dh (101A3Ah)	**REG101A3A**	**7:0**	**Default : 0x03**	**Access : R/W**
	PAD_PS[7:0]	7:0	PAD_PS.	
1Dh (101A3Bh)	**REG101A3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_PS[15:8]	7:0	See description of '101A3Ah'.	
1Eh (101A3Ch)	**REG101A3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_PS[23:16]	7:0	See description of '101A3Ah'.	
1Eh (101A3Dh)	**REG101A3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PAD_PS[27:24]	3:0	See description of '101A3Ah'.	

CHIPTOP Register (Bank = 101E)

CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (101E02h)	**REG101E02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FORCE_MODPAD	0	Force all MOD pads controlled by pad_top, mainly for test mode.	
01h (101E03h)	**REG101E03**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBSETL	7	Serial bus pads set low.	
	SBSETH	6	Serial bus pads set high.	
	SETL	5	Digital pads set low.	
	SETH	4	Digital pads set high.	
	BOOT_FROM_SDRAM	3	Boot from SDRAM. 1: Enable boot from SDRAM. 0: Disable boot from SDRAM.	
	-	2:0	Reserved.	
03h (101E06h)	**REG101E06**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM_OEN[5:0]	5:0	Output ENABLE_BAR of PWM pads. Initial should be input for capturing CHIP_CONFIG while reset.	
04h (101E08h)	**REG101E08**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	DBOARD_CA9_MODE	3	No used.	
	FCIE_USE_BYPASS	2	1 for disable bypass mode.	
	SDIO_USE_BYPASS	1	1 for disable bypass mode.	
	FORCE_CA9_MIUGATE	0	Force CA9's miu2x_en to be zero.	
04h (101E09h)	**REG101E09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MIPSPLL_LOCK_CHECK_FOR_CA9	1	Reg control mode for mipspll_lock.	
	MPLL_LOCK_CHECK_FOR_CA9	0	Reg control mode for mpll_lock.	
06h (101E0Ch)	**REG101E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	PHASE_SEL[4:0]	4:0	Phase selection for nand_delay_line.	
06h (101E0Dh)	**REG101E0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DQS_DLINE_SEL	1	1 for select data from dqs deline.	
	DQS_TEST_EN	0	1 for enable dqs test.	
07h (101E0Eh)	**REG101E0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIQ_SOURCE0[7:0]	7:0	[0]&[8] for control fiq source 14&13.	
07h (101E0Fh)	**REG101E0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIQ_SOURCE0[15:8]	7:0	See description of '101E0Eh'.	
08h (101E10h)	**REG101E10**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIQ_SOURCE1[7:0]	7:0	[0]&[8] for control fiq source 12&11.	
08h (101E11h)	**REG101E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIQ_SOURCE1[15:8]	7:0	See description of '101E10h'.	
0Bh (101E16h)	**REG101E16**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	COMBO_REMAP[3:0]	3:0	No used.	
0Ch	**REG101E18**	**7:0**	**Default : 0x00**	**Access : R/W**

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101E18h)	COMBO_BOOT_ADR[7:0]	7:0	Base address after reset.	
0Ch (101E19h)	**REG101E19**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_BOOT_ADR[15:8]	7:0	See description of '101E18h'.	
0Dh (101E1Ah)	**REG101E1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_BOOT_ADR[23:16]	7:0	See description of '101E18h'.	
0Dh (101E1Bh)	**REG101E1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_BOOT_ADR[31:24]	7:0	See description of '101E18h'.	
0Eh (101E1Ch)	**REG101E1C**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	EMMC_SW_RSTZ	4	Emmc software reset.	
	-	3:2	Reserved.	
	CLK4X_DIV_EN_SDIO2	1	Sdio flash clock selection.	
	CLK4X_DIV_EN_FCIE	0	Fcie flash clock selection.	
0Fh (101E1Eh)	**REG101E1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	VSENSE_CHSEL[2:0]	2:0	PAD_VSENSE ch selection.	
10h (101E20h)	**REG101E20**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	BYP_MIPS_DFS	3	Clock selection for MIPS DFS.	
	-	2:0	Reserved.	
10h (101E21h)	**REG101E21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	TSO_IN_MUX[2:0]	6:4	Source Selections for TSP Channel 0. 3'b000: come from PAD_TS0. 3'b001: come from PAD_TS1. 3'b010: come from PAD_TS2. 3'b110: come from PAD_TS_CB. 3'b111: come from DeMOD_TOP. Others reserved.	
	-	3:0	Reserved.	
11h (101E22h)	**REG101E22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TS_CB_MUX[2:0]	6:4	Source Selections for TSP Channel 0. 3'b000: come from PAD_TS0. 3'b001: come from PAD_TS1. 3'b010: come from DeMOD_TOP. 3'b011: come from PAD_TS2. 3'b100: come from PAD_TS3. Others reserved.	
	-	3	Reserved.	
	TS0_MUX[2:0]	2:0	Source Selections for TSP Channel 0. 3'b000: come from PAD_TS0. 3'b001: come from PAD_TS1. 3'b010: come from PAD_TS2. 3'b110: come from PAD_TS_CB. 3'b111: come from DeMOD_TOP. Others reserved.	
11h (101E23h)	**REG101E23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	TS2_MUX[2:0]	6:4	Source Selections for TSP Channel 2. 3'b000: come from PAD_TS0. 3'b001: come from PAD_TS1. 3'b010: come from PAD_TS2. 3'b110: come from PAD_TS_CB. 3'b111: come from DeMOD_TOP. Others reserved.	
	-	3	Reserved.	
	TS1_MUX[2:0]	2:0	Source Selections for TSP Channel 1. 3'b000: come from PAD_TS0. 3'b001: come from PAD_TS1. 3'b010: come from DeMOD_TOP. 3'b011: come from PAD_TS2. 3'b100: come from PAD_TS3. Others reserved.	
12h (101E25h)	**REG101E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CVBS_DACB_SEL	1	CVBS DAC2 Source Selection. 0: Select VIF. 1: Select VD.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CVBS_DACA_SEL	0	CVBS DAC1 Source Selection. 0: Select VIF. 1: Select VD.	
1Ch ~ 23h (101E38h ~ 101E47h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (101E60h)	**REG101E60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DI2_CLK_INV	1	DI_CLK invert.	
	DI_CLK_INV	0	DI_CLK invert.	
30h (101E61h)	**REG101E61**	**7:0**	**Default : 0x00**	**Access : R/W**
	DI2_CLK_SEL[3:0]	7:4	DOUT_CLK delay level selection.	
	DI_CLK_SEL[3:0]	3:0	DOUT_CLK delay level selection.	
31h (101E62h)	**REG101E62**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CLK_CALC_EN	0	Clock calculate enable.	
32h (101E64h)	**REG101E64**	**7:0**	**Default : 0x00**	**Access : RO**
	CALC_CNT_REPORT[7:0]	7:0	Clock count number report.	
32h (101E65h)	**REG101E65**	**7:0**	**Default : 0x00**	**Access : RO**
	CALC_CNT_REPORT[15:8]	7:0	See description of '101E64h'.	
40h (101E80h)	**REG101E80**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MIU_DYN_DIS0[7:0]	7:0	MIU dynamic gated disable.	
40h (101E81h)	**REG101E81**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MIU_DYN_DIS0[15:8]	7:0	See description of '101E80h'.	
41h (101E82h)	**REG101E82**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MIU_DYN_DIS1[7:0]	7:0	MIU dynamic gated disable.	
41h (101E83h)	**REG101E83**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MIU_DYN_DIS1[15:8]	7:0	See description of '101E82h'.	
42h (101E84h)	**REG101E84**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MIU_DYN_DIS2[7:0]	7:0	MIU dynamic gated disable.	
42h (101E85h)	**REG101E85**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MIU_DYN_DIS2[15:8]	7:0	See description of '101E84h'.	
43h	**REG101E86**	**7:0**	**Default : 0xFF**	**Access : R/W**

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101E86h)	MIU_DYN_DIS3[7:0]	7:0	MIU dynamic gated disable.	
43h (101E87h)	**REG101E87**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MIU_DYN_DIS3[15:8]	7:0	See description of '101E86h'.	
44h (101E88h)	**REG101E88**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP0[7:0]	7:0	MIU ip gated.	
44h (101E89h)	**REG101E89**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP0[15:8]	7:0	See description of '101E88h'.	
45h (101E8Ah)	**REG101E8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP1[7:0]	7:0	MIU ip gated.	
45h (101E8Bh)	**REG101E8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP1[15:8]	7:0	See description of '101E8Ah'.	
46h (101E8Ch)	**REG101E8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP2[7:0]	7:0	MIU ip gated.	
46h (101E8Dh)	**REG101E8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP2[15:8]	7:0	See description of '101E8Ch'.	
47h (101E8Eh)	**REG101E8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP3[7:0]	7:0	MIU ip gated.	
47h (101E8Fh)	**REG101E8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_GATE_IP3[15:8]	7:0	See description of '101E8Eh'.	
4Fh (101E9Eh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
53h (101EA6h)	**REG101EA6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UART_SEL1[3:0]	7:4	Select UART1 source.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	UART_SEL0[3:0]	3:0	Select UART0 source for PAD_DDCA_DA and PAD_DDCA_CK. 0000: Fuart0. 0001: Fuart1. 0010: Uart0. 0011: Uart1. 0100: Uart2. 0101: Uart3. 0110: VD R2 Uart. 0111: TSP Uart. 1000: NONE. 1001: NONE. 1010: VD_MCU51 Uart0. 1011: VD_MCU51 Uart1. 1100: NONE. 1101: N.A. 1110: COMBO R2. 1111: N.A. Note: For PAD_DDCA_DA and PAD_DDCA_CK, please refer to the "reg_hk51_uart0_en" and "reg_uart_rx_enable" in reg_pm_sleep.xls. (a). "reg_hk51_uart0_en" == 0. (b). "reg_uart_rx_enable" == 1.	
53h (101EA7h)	**REG101EA7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UART_SEL3[3:0]	7:4	Select UART3 source.	
	UART_SEL2[3:0]	3:0	Select UART2 source.	
54h (101EA8h)	**REG101EA8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UART_SEL5[3:0]	7:4	Select UART5 source.	
	UART_SEL4[3:0]	3:0	Select UART4 source.	
55h (101EAAh)	**REG101EAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	JTAG_POL	7	JTAG oen polarity selection. 0: Normal. 1: Invert.	
	-	6:4	Reserved.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	JTAG_SEL[3:0]	3:0	JTAG selection. 000: Reserved. 001: HK MCU32. 010: VD MCU32. 011: Reserved. 100: AU MCU32.	
55h (101EABh)	**REG101EAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	UART_PAD_INVERSE[7:0]	7:0	Invert PAD UART TX/RX.	
56h (101EACh)	**REG101EAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	UART_INNER_LOOPBACK[7:0]	7:0	Enable of inner loopback test for 8 sets of UART controller. [0]: UART0 enable. [1]: UART1 enable. [2]: UART2 enable. [3]: UART3 enable. [4]: UART4 enable. [5]: UART5 enable. [6]: UART6 enable. [7]: UART7 enable.	
56h (101EADh)	**REG101EAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	UART_OUTER_LOOPBACK[7:0]	7:0	Enable of outer loopback test for 3 sets of UART pad. [0]: UART0 pad enable. [1]: UART1 pad enable. [2]: UART2 pad enable.	
5Bh	**REG101EB6**	**7:0**	**Default : 0x00**	**Access : R/W**

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101EB6h)	BOND_AUDIO_OV_EN[7:0]	7:0	Audio bonding overwrite enable. Bit 0: BOND_AUDIO_0. Bit 1: BOND_AUDIO_1. Bit 2: BOND_AUDIO_2. Bit 3: BOND_AUDIO_3. Bit 4: BOND_AUDIO_4. Bit 5: BOND_AUDIO_5. Bit 6: BOND_AUDIO_6. Bit 7: BOND_AUDIO_7. Bit 8: BOND_AUDIO_8. Bit 9: BOND_AUDIO_9. Bit 10: BOND_AUDIO_10. Bit 11: BOND_AUDIO_11. Bit 12: BOND_AUDIO_12. Bit 13: BOND_AUDIO_13. Bit 14: BOND_AUDIO_14. Bit 15: BOND_AUDIO_15.	
5Bh (101EB7h)	**REG101EB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_AUDIO_OV_EN[15:8]	7:0	See description of '101EB6h'.	
5Ch (101EB8h)	**REG101EB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_AUDIO_OV[7:0]	7:0	Audio bonding overwrite value.	
5Ch (101EB9h)	**REG101EB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_AUDIO_OV[15:8]	7:0	See description of '101EB8h'.	
5Dh (101EBAh)	**REG101EBA**	**7:0**	**Default : 0x00**	**Access : RO**
	STAT_BOND_AUDIO[7:0]	7:0	Audio bonding status.	
5Dh (101EBBh)	**REG101EBB**	**7:0**	**Default : 0x00**	**Access : RO**
	STAT_BOND_AUDIO[15:8]	7:0	See description of '101EBAh'.	
61h (101EC3h)	**REG101EC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV1[1:0]	7:6	Reserved.	
	BOND_OV_EN1[1:0]	5:4	Bonding overwrite enable. Bit0: Reserved. Bit1: Reserved.	
	-	3:0	Reserved.	
63h (101EC6h)	**REG101EC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV_KEY[7:0]	7:0	Set bonding overwrite key.	
63h	**REG101EC7**	**7:0**	**Default : 0x00**	**Access : R/W**

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101EC7h)	BOND_OV_KEY[15:8]	7:0	See description of '101EC6h'.	
65h (101ECAh)	**REG101ECA**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CHIP_CONFIG_STAT[4:0]	4:0	CHIP_CONFIG status.	
68h (101ED0h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
69h (101ED2h)	**REG101ED2**	**7:0**	**Default : 0x00**	**Access : RO**
	POWERGOOD_MPLL	7	POWERGOOD_MPLL status.	
	-	6:0	Reserved.	
6Ah (101ED4h)	**REG101ED4**	**7:0**	**Default : 0x00**	**Access : R/W**
	WARM_BOOTBASE[7:0]	7:0	The booting address of SDRAM.	
6Ah (101ED5h)	**REG101ED5**	**7:0**	**Default : 0x00**	**Access : R/W**
	WARM_BOOTBASE[15:8]	7:0	See description of '101ED4h'.	
6Ch (101ED8h)	**REG101ED8**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	AXI_CLK1X	1		
	COLD_BOOT	0	The booting selection.	
70h (101EE1h)	**REG101EE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ROSC_OUT_SEL[2:0]	2:0	Ring OSC output select. 000: Select delay chain 0. 001: Select delay chain 1. 010: Select delay chain 2. 011: Select delay chain 3. 100: Select delay chain 4. 101: Select delay chain 5. 110: Select delay chain 6. 111: Select delay chain 7.	
71h (101EE2h)	**REG101EE2**	**7:0**	**Default : 0xA0**	**Access : R/W**
	XHD_TC0	7	SRAM wrapper configuration.	
	XHD_TC1	6	SRAM wrapper configuration.	
	XRF_TC0	5	SRAM wrapper configuration.	
	XRF_TC1	4	SRAM wrapper configuration.	
	DELAY_AMT[3:0]	3:0	MIU dyanmical gated delay.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
71h (101EE3h)	**REG101EE3**	**7:0**	**Default : 0x2A**	**Access : R/W**
	SRAM_VSEL[1:0]	7:6	SRAM wrapper configuration.	
	SRAM2P_VW[1:0]	5:4	SRAM wrapper configuration.	
	SRAM2P_VR[1:0]	3:2	SRAM wrapper configuration.	
	AMG_TC0	1	SRAM wrapper configuration.	
	AMG_TC1	0	SRAM wrapper configuration.	
72h (101EE4h)	**REG101EE4**	**7:0**	**Default : 0x00**	**Access : RO**
	POWERGOOD_AVDD	7	POWERGOOD_AVDD status.	
	-	6:0	Reserved.	
72h (101EE5h)	**REG101EE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CKG_ALLDFT	0	MIU clock select DFT clock. MPLL_SYN clock select DFT clock. MIU_REC clock select DFT clock. GE clock select DFT clock.	
73h (101EE6h)	**REG101EE6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RESERVED[7:0]	7:0	RESERVED register.	
73h (101EE7h)	**REG101EE7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RESERVED[15:8]	7:0	See description of '101EE6h'.	
74h (101EE8h)	**REG101EE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED[23:16]	7:0	See description of '101EE6h'.	
74h (101EE9h)	**REG101EE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED[31:24]	7:0	See description of '101EE6h'.	
75h (101EEAh)	**REG101EEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_RB	7	Setting for the data arrangement on test bus.	
	TEST_GB	6	Setting for the data arrangement on test bus.	
	TEST_RG	5	Setting for the data arrangement on test bus.	
	TEST_ADC_CLK_SEL	4	Select CLK_TEST_OUT. [0] select TEST CLOCK from TEST_BUS. [1] select TEST CLOCK from ADCPLL.	
	SWAPTEST12BIT	3	Swap MSB 12bits with LSB 12bits of test bus.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CLK_OUT_SEL[2:0]	2:0	Select TEST_CLK_OUT source. 000: TEST_CLK_OUT= TEST_BUS_GB[0]. 001: TEST_CLK_OUT= TEST_BUS_GB[1]. 010: TEST_CLK_OUT= TEST_BUS_GB[2]. 011: TEST_CLK_OUT= TEST_BUS_GB[3]. 100: TEST_CLK_OUT= TEST_BUS_GB[4]. 101: TEST_CLK_OUT= TEST_BUS_GB[5]. 110: TEST_CLK_OUT= TEST_BUS_GB[6]. 111: TEST_CLK_OUT= TEST_BUS_GB[7].	
75h (101EEBh)	**REG101EEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROSC_IN_SEL	7	Select the input source of ring oscillator in CHIP_CONF. 1: Close-loop (enable ring oscillator). 0: Open-loop (input from external digital input).	
	TESTBUS_EN	6	Enable test bus output.	
	TESTCLK_MODE	5	TESTCLK_MODE used in TEST_CTRL.	
	-	4	Reserved.	
	SEL_CLK_TEST_OUT[3:0]	3:0	Select CLK_TEST_OUT. 2'b00: select CLK_TEST_OUT[47:0]. 2'b01: select CLK_TEST_OUT[95:48]. 2'b10: select CLK_TEST_OUT[143:96]. 2'b11: reserved.	
76h (101EECh)	**REG101EEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SINGLE_ADC_CLK_OUT_SEL[2:0]	6:4	Select test_adc_clk_in divider ratio. 001: Test_adc_clk_in_d2. 010: Test_adc_clk_in_d4. 011: Test_adc_clk_in_d8. 100: Test_adc_clk_in_d16. 101: Test_adc_clk_in_d32. 110: Test_adc_clk_in_d54. others: Select original test_adc_clk_in.	
	-	3	Reserved.	

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SINGLE_CLK_OUT_SEL[2:0]	2:0	Select single CLK_OUT. 001: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT. 010: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d4. 011: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d8. 100: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d16. Others: No TEST_CLK_OUT.	
77h (101EEEh)	**REG101EEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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CHIPTOP Register (Bank = 101E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	TEST_BUS24B_SEL[5:0]	5:0	Select TEST_BUS[23:0] source. 6'd1: TEST_BUS = LPLL_TEST_OUT. 6'd2: TEST_BUS = CLK_TEST_OUT[23:0] after selecting CLK_TEST_OUT. 6'd3: TEST_BUS = CLK_TEST_OUT[47:24] after selecting CLK_TEST_OUT. 6'd4: TEST_BUS = {ROSC_OUT, CLK_RTC, CLK_TEST_OUT[70:48]}. 6'd5: TEST_BUS = TSP_TEST_OUT. 6'd6: TEST_BUS = MVD_TEST_OUT. 6'd7: TEST_BUS = PM_TEST_OUT. 6'd8: TEST_BUS = VD_TEST_OUT. 6'd9: TEST_BUS = SAR_TEST_OUT. 6'd10: TEST_BUS = AUDIO_TEST_OUT. 6'd11: TEST_BUS = CCFL_TEST_OUT. 6'd12: TEST_BUS = ADCDVI_TEST_OUT. 6'd13: TEST_BUS = SC_TEST_OUT. 6'd14: TEST_BUS = MIU_TEST_OUT. 6'd15: TEST_BUS = MCU_TEST_OUT. 6'd16: TEST_BUS = DC_TEST_OUT. 6'd17: TEST_BUS = GOP_TEST_OUT. //6'd18: TEST_BUS = SDIO_TEST_OUT. 6'd19: TEST_BUS = UHC_TEST_OUT. 6'd20: TEST_BUS = UTMI_TEST_OUT. 6'd21: TEST_BUS = M4VE_TEST_OUT. 6'd22: TEST_BUS = GE_TEST_OUT. 6'd23: TEST_BUS = 32BMCU_TEST_OUT. 6'd24: TEST_BUS = PIU_TEST_OUT. 6'd25: TEST_BUS = STRLD_TEST_OUT. 6'd26: TEST_BUS = EMAC_TEST_OUT. 6'd27: TEST_BUS = JPD_TEST_OUT. 6'd28: TEST_BUS = VE_TEST_OUT. 6'd29: TEST_BUS = DHC_TEST_OUT. 6'd30: TEST_BUS = NFIE_TEST_OUT. 6'd31: TEST_BUS = MIPS_TEST_OUT. 6'd32: TEST_BUS = GPD_TEST_OUT. 6'd33: TEST_BUS = FRC_TEST_OUT. 6'd34: TEST_BUS = RVD_TEST_OUT. 6'd35: TEST_BUS = DSCRMB_TEST_OUT. 6'd36: TEST_BUS = UHC1_TEST_OUT. 6'd37: TEST_BUS = HVD_TEST_OUT. 6'd38: TEST_BUS = MPIF_TEST_OUT. 6'd39: TEST_BUS = LAN_TOP_TEST_OUT. 6'd40: TEST_BUS = DEMOD_TEST_OUT.

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CHIPTOP Register (Bank = 101E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
78h (101EF0h)	**REG101EF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TEST_BUS24B_SEL0[5:0]	5:0	Select TEST_BUS0.	
78h (101EF1h)	**REG101EF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TEST_BUS24B_SEL1[5:0]	5:0	Select TEST_BUS1.	
79h (101EF2h)	**REG101EF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TEST_BUS24B_SEL2[5:0]	5:0	Select TEST_BUS2.	
79h (101EF3h)	**REG101EF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TEST_BUS24B_SEL3[5:0]	5:0	Select TEST_BUS3.	
7Ah (101EF4h)	**REG101EF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TEST_BUS24B_SEL4[5:0]	5:0	Select TEST_BUS4.	
7Ah (101EF5h)	**REG101EF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TEST_BUS24B_SEL5[5:0]	5:0	Select TEST_BUS5.	

GOP Register (Bank = 101F)

GOP Register (Bank = 101F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101F00h)	**REG101F00**	**7:0**	**Default : 0x18**	**Access : R/W**
	DWIN_SHOT	7	DWIN capture mode. 0: Capture each DWIN frame. 1: Auto-stop capture after one frame has been successfully captured.	
	-	6	Reserved.	
	DWIN_FLD_INV	5	Inverse input field polarity.	
	DWIN_PROG	4	DWIN write to DRAM order. 0: Interlace. 1: Progressive.	

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GOP Register (Bank = 101F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3	Reserved.	
	DWIN_HS_INV	2	DWIN HSYNC source inverse.	
	DWIN_VS_INV	1	DWIN VSYNC source inverse.	
	DWIN_EN	0	GOP dump window data to DRAM enable. 1. Set DWIN_EN. 2. Wait (DWIN_EN==1). 1: Clear DWIN_EN. 3. Wait (DWIN_EN==0).	
00h (101F01h)	**REG101F01**	**7:0**	**Default : 0xC0**	**Access : R/W**
	DWIN_DTYPE[1:0]	7:6	Convert DATA type into DRAM. 0: UV7Y8. 1: UV8Y8. 2: ARGB8888. 3: RGB565.	
	-	5:4	Reserved.	
	UV_SWAP	3	SWAP UV into DRAM.	
	SRC_SEL[2:0]	2:0	DWIN source select. 0: OP. 1: IP main. 2: IP sub. 3: MVOP main. 4: MVOP sub.	
01h ~ 01h (101F02h ~ 101F03h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (101F04h)	**REG101F04**	**7:0**	**Default : 0xF8**	**Access : R/W**
	VS_INT_MASK	7	Vsync INT mask.	
	BF_INT_MASK	6	Bottom Field INT mask.	
	TF_INT_MASK	5	TOP Field INT mask.	
	PROG_INT_MASK	4	PROG INT mask.	
	WADR_INT_MASK	3	WADR violation INT mask.	
	-	2:0	Reserved.	

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GOP Register (Bank = 101F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (101F05h)	**REG101F05**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_INT	7	Vsync INT FLAG.	
	BF_INT	6	Bottom Field INT FLAG.	
	TF_INT	5	TOP Field INT FLAG.	
	PROG_INT	4	PROG INT FLAG.	
	WADR_INT	3	DMA WADR violation INT.	
	-	2:0	Reserved.	
03h (101F06h)	**REG101F06**	**7:0**	**Default : 0x00**	**Access : RO**
	SRAM_BIST_FAIL	7	SRAM BIST FLAG.	
	WDMA_STATE[2:0]	6:4	DWIN DMA state. 0: WAIT_VS. 1: VS_RISE. 2: START. 3: MIU_BURST. 4: CHK_FF. 5: IDLE. 6: WAIT_LAST_DONE_Z.	
	-	3	Reserved.	
	DWIN_BF_ACK	2	DWIN interlace mode Bottom Field. DOWN ACK.	
	DWIN_TF_ACK	1	DWIN interlace mode TOP Field. DOWN ACK.	
	DWIN_PROG_ACK	0	DWIN progressive mode DOWN ACK.	
03h (101F07h)	**REG101F07**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	GOPG_RD_FLAG	5	GOPG pinpon buffer flag.	
	GOPD_WR_FLAG	4	GOPD pinpon buffer flag.	
	PINPON	3	PINPON mode.	
	-	2	Reserved.	
	DWIN_BUF_UF	1	DWIN buffer underflow FLAG.	
	DWIN_BUF_OF	0	DWIN buffer overflow FLAG.	
04h (101F08h)	**REG101F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	ALPHA_INV	7	Alpha inverse.	
	R2Y_CSC	6	Enable R2Y CSC.	

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GOP Register (Bank = 101F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:0	Reserved.	
04h (101F09h)	**REG101F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	ALPHA[7:0]	7:0	Constant ALPHA value for ARGB8888 type.	
05h (101F0Ah)	**REG101F0A**	**7:0**	**Default : 0x83**	**Access : R/W**
	DW_HI_TSH[1:0]	7:6	MIU write High priority threshold.	
	-	5:3	Reserved.	
	DMA_EXT[2:0]	2:0	DMA burst access length. 0: 2. 1: 4. 2: 8. 3: 16. 4: 24. 5: 32. 6: 48. 7: 64.	
10h (101F20h)	**REG101F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_VSTR[7:0]	7:0	DWIN capture V start line.	
10h (101F21h)	**REG101F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DWIN_VSTR[10:8]	2:0	See description of '101F20h'.	
11h (101F22h)	**REG101F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_HSTR[7:0]	7:0	DWIN capture H start Pixel.	
11h (101F23h)	**REG101F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DWIN_HSTR[9:8]	1:0	See description of '101F22h'.	
12h (101F24h)	**REG101F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_VEND[7:0]	7:0	DWIN capture V end line (unit: line).	
12h (101F25h)	**REG101F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DWIN_VEND[10:8]	2:0	See description of '101F24h'.	
13h (101F26h)	**REG101F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_HEND[7:0]	7:0	DWIN capture H end Pixel (unit: 8byte).	
13h (101F27h)	**REG101F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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GOP Register (Bank = 101F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DWIN_HEND[9:8]	1:0	See description of '101F26h'.	
14h (101F28h)	**REG101F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_HSIZE[7:0]	7:0	DWIN capture H size (unit: 8byte). = REG_DWIN_HEND - REG_DWIN_HSTR.	
14h (101F29h)	**REG101F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DWIN_HSIZE[9:8]	1:0	See description of '101F28h'.	
15h (101F2Ah)	**REG101F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_JMPLEN[7:0]	7:0	Jump address length after each DWIN line end to next line start.	
15h (101F2Bh)	**REG101F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DWIN_JMPLEN[9:8]	1:0	See description of '101F2Ah'.	
16h (101F2Ch)	**REG101F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_DWIN_TF_STR0[7:0]	7:0	DWIN DRAM start address.	
16h (101F2Dh)	**REG101F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_DWIN_TF_STR0[15:8]	7:0	See description of '101F2Ch'.	
17h (101F2Eh)	**REG101F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_DWIN_TF_STR0[23:16]	7:0	See description of '101F2Ch'.	
17h (101F2Fh)	**REG101F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_DWIN_TF_STR0[27:24]	3:0	See description of '101F2Ch'.	
18h (101F30h)	**REG101F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_UPBOND_ADR0[7:0]	7:0	DWIN DRAM access address high bond.	
18h (101F31h)	**REG101F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_UPBOND_ADR0[15:8]	7:0	See description of '101F30h'.	
19h (101F32h)	**REG101F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_UPBOND_ADR0[23:16]	7:0	See description of '101F30h'.	
19h (101F33h)	**REG101F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DWIN_UPBOND_ADR0[27:24]	3:0	See description of '101F30h'.	
1Ah (101F34h)	**REG101F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_DWIN_TF_STR1[7:0]	7:0	DWIN DRAM start address.	

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GOP Register (Bank = 101F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ah (101F35h)	**REG101F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_DWIN_TF_STR1[15:8]	7:0	See description of '101F34h'.	
1Bh (101F36h)	**REG101F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_DWIN_TF_STR1[23:16]	7:0	See description of '101F34h'.	
1Bh (101F37h)	**REG101F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_DWIN_TF_STR1[27:24]	3:0	See description of '101F34h'.	
1Ch (101F38h)	**REG101F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_UPBOND_ADR1[7:0]	7:0	DWIN DRAM access address high bond.	
1Ch (101F39h)	**REG101F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_UPBOND_ADR1[15:8]	7:0	See description of '101F38h'.	
1Dh (101F3Ah)	**REG101F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DWIN_UPBOND_ADR1[23:16]	7:0	See description of '101F38h'.	
1Dh (101F3Bh)	**REG101F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DWIN_UPBOND_ADR1[27:24]	3:0	See description of '101F38h'.	
1Eh (101F3Ch)	**REG101F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAM_TST_MD[1:0]	7:6	0: Disable. 1: Sram test mode --gradient. 2: Sram test mode --grid. 3: Sram test mode --strip.	
	-	5:3	Reserved.	
	MIU_REQ_DISABLE	2	0: Normal gop to miu access. 1: Disable gop to miu access.	
	-	1:0	Reserved.	
1Fh ~ 1Fh (101F3Eh ~ 101F3Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h (101F40h)	**REG101F40**	**7:0**	**Default : 0x00**	**Access : RO**
	WADR_VIO[7:0]	7:0	DMA violation write address out of bond.	
20h (101F41h)	**REG101F41**	**7:0**	**Default : 0x00**	**Access : RO**
	WADR_VIO[15:8]	7:0	See description of '101F40h'.	
21h	**REG101F42**	**7:0**	**Default : 0x00**	**Access : RO**

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GOP Register (Bank = 101F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(101F42h)	WADR_VIO[23:16]	7:0	See description of '101F40h'.	
21h (101F43h)	**REG101F43**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	WADR_VIO[24]	0	See description of '101F40h'.	

UHC0 Register (Bank = 1024)

UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102400h)	**HCCAP**	**7:0**	**Default : 0x10**	**Access : RO**
	CAPLENGTH	7:0	Capability Register Length. This register is used as an offset to be added to register base to determine the beginning of the Operational Register Space.	
01h (102402h)	**HCCAP**	**7:0**	**Default : 0x00**	**Access : RO**
	HCIVERSION[7:0]	7:0	Host Controller Interface Version Number. This register is a two-byte register containing a BCD encoding of the EHCI revision number supported by the Host Controller.	
01h (102403h)	**HCCAP**	**7:0**	**Default : 0x01**	**Access : RO**
	HCIVERSION[15:8]	7:0	See description of '2402h'.	
02h (102404h)	**HCSPARAMS**	**7:0**	**Default : 0x01**	**Access : RO**
	-	7:4	Reserved.	
	N_PORTS	3:0	Number of Ports. This field specifies the number of physical downstream ports implemented on the Host Controller.	
04h (102408h)	**HCCPARAMS**	**7:0**	**Default : 0x06**	**Access : RO**
	-	7:3	Reserved.	
	ASYN_SCH_PARK_CAP	2	Asynchronous Schedule Park Capability. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via the Frame List Size field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PROG_FR_LIST_FLAG	1	Programmable Frame List Flag. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via Frame List Size Field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	-	0	Reserved.	
08h (102410h)	**USBCMD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INT_OAAD	6	Interrupt on Asynchronous Advance Doorbell. This bit is used as a doorbell by software to ring the Host Controller to issue an interrupt at the next advance of Asynchronous Schedule.	
	ASCH_EN	5	Asynchronous Schedule Enable. This bit controls whether the Host Controller skips the processing of Asynchronous Schedule. 0: Do not process Asynchronous Schedule. 1: Use the ASYNCLISTADDR register to access the Asynchronous Schedule.	
	PSCH_EN	4	Periodic Schedule Enable. This bit controls whether the Host Controller skips the processing of Periodic Schedule. 0: Do not process Periodic Schedule. 1: Use the PERIODICKISTBASE register to access the Periodic Schedule.	
	FRL_SIZE	3:2	Frame List Size. This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value). 01: 512 elements (2048 bytes). 10: 256 elements (1024 bytes). 11: Reserved.	
	HC_RESET	1	Host Controller Reset. This control bit is used by software to reset the Host Controller.	
	RS	0	Run/Stop. When this bit is set to '1', the Host Controller proceeds with the execution of schedule. 0: Stop.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Run.	
08h (102411h)	**USBCMD**	**7:0**	**Default : 0x0b**	**Access : R/W**
	-	7:4	Reserved.	
	ASYN_PK_EN	3	Asynchronous Schedule Park Mode Enable. Software uses this register to enable or disable the Park mode. When this register is set to 1, the Park mode is enabled.	
	-	2	Reserved.	
	ASYN_PK_CNT	1:0	Asynchronous Schedule Park Mode Count. This field contains a count for the number of successive transactions that the Host Controller is allowed to execute from a high-speed queue head on Asynchronous Schedule.	
09h (102412h)	**USBCMD**	**7:0**	**Default : 0x08**	**Access : R/W**
	INT_THRC	7:0	Interrupt Threshold Control. This field is used by system software to select the maximum rate at which the Host Controller will issue interrupts. The only valid values are described below: Value — Maximum Interrupt Interval for High Speed 00h — Reserved. 01h — 1 micro-frame. 02h — 2 micro-frames. 04h — 4 micro-frames. 08h — 8 micro-frames (default, equals to 1ms). 10h — 16 micro-frames (2 ms). 20h — 32 micro-frames (4 ms). 40h — 64 micro-frames (8 ms). Note: For Full Speed, these registers are reserved.	
0Ah (102414h)	**USBSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:6	Reserved.	
	INT_OAA	5	Interrupt on Async Advance. This status bit indicates the assertion of interrupt on Async Advance Doorbell.	
	H_SYSERR	4	Host System Error. The Host Controller sets this bit to 1 when a serious error occurred during a host system access involving the Host Controller module.	
	FRL_ROL	3	Frame List Rollover.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			The Host Controller sets this bit to 1 when the Frame List Index rolls over from its maximum value to zero.	
	PO_CHG_DET	2	Port Change Detect. The Host Controller sets this bit to '1' when any port has a change bit transition from '0' to '1'. In addition, this bit is loaded with the OR of all of the PORTSC change bits.	
	USBERR_INT	1	USB Error Interrupt. The Host Controller sets this bit to '1' when the completion of a USB transaction results in an error condition.	
	USB_INT	0	USB Interrupt. The Host Controller sets this bit to '1' upon the completion of a USB transaction.	
0Ah (102415h)	**USBSTS**	**7:0**	**Default : 0x10**	**Access : RO**
	ASCH_STS	7	Asynchronous Schedule Status. This bit reports the actual status of Asynchronous Schedule.	
	PSCH_STS	6	Periodic Schedule Status. This bit reports the actual status of Periodic Schedule.	
	RECLAMATION	5	Reclamation. This is a read-only status bit, and is used to detect an empty of Asynchronous Schedule.	
	HCHALTED	4	Host Controller Halted. This bit is a zero whenever the Run/Stop bit is set to '1'. The Host Controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to '0'.	
	-	3:0	Reserved.	
0Ch (102418h)	**USBINTR**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_OAA_EN	5	Interrupt on Async Advance Enable. When this bit is set to '1', and the Interrupt on Async Advance bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	H_SYSERR_EN	4	Host System Error Enable.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			When this bit is set to '1', and the Host System Error Status bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	FRL_ROL_EN	3	Frame List Rollover Enable. When this bit is set to '1', and the Frame List Rollover bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	PO_CHG_INT_EN	2	Port Change Interrupt Enable. When this bit is set to '1', and the Port Change Detect bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	USBERR_INT_EN	1	USB Error Interrupt Enable. When this bit is set to '1', and the USBERRINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	USB_INT_EN	0	USB Interrupt Enable. When this bit is set to '1', and the USBINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
0Eh (10241Ch)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRINDEX[7:0]	7:0	Frame Index. This register is used by the Host Controller to index the frame into the Periodic Frame List. It updates every 125 microseconds. This register cannot be written unless the Host Controller is in the Halted state.	
0Eh (10241Dh)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRINDEX[13:8]	5:0	See description of '1Ch'.	
0Fh ~ 12h (10241Eh ~ 2424h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
12h (102425h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[15:12]	7:4	Periodic Frame List Base Address. This register contains the beginning address of the Periodic Frame List in the system memory. These bits correspond to memory address signals [31:12].	

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UHC0 Register (Bank = 1024)

Index (Absolute)	Mnemonic	Bit	Description	
	-	3:0	Reserved.	
13h (102426h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[23:16]	7:0	See description of '25h'.	
13h (102427h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[31:24]	7:0	See description of '25h'.	
14h (102428h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[7:5]	7:5	Current Asynchronous List Address. This register contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5].	
	-	4:0	Reserved.	
14h (102429h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[15:8]	7:0	Please see description of '28h'.	
15h (10242Ah)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[23:16]	7:0	Please see description of '28h'.	
15h (10242Bh)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[31:24]	7:0	Please see description of '28h'.	
18h (102430h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, R/WC, RO**
	PO_SUSP	7	Port Suspend (R/W). 1: Port is in suspend state. 0: Port is not in suspend state. The Port Enable bit and Suspend bit of this register define the port state as follows: Bits [Port Enable, Suspend] — Port State 0X — Disable Enable Suspend During the suspend state, downstream propagation of data is blocked on this port, except for port reset. While in the suspend state, the port is sensitive to resume detection. Writing a zero to this bit is ignored by the Host Controller. The Host Controller will unconditionally set this bit to a zero when: The software sets Force Port Resume bit to a zero (from a one) The software sets Port Reset bit to a one (from a zero)	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Note: Before setting this bit, RUN/STOP bit should be set to 0.	
	F_PO_RESM	6	Force Port Resume (R/W). 1: Resume detected/driven on port. 0: No resume detected/driven on port. Software sets this bit to a one to resume signaling. The Host Controller sets this bit to a one if a J-to-K transition is detected while the port is in the suspend state. When this bit transits to a one for the detection of a J-to-K transition, the Port Change Detect bit in USBSTS register is also set to a one.	
	POR_RESET_STS	5	USB port reset status. The bit is a read only status.	
		4	Reserved.	
	PO_EN_CHG	3	Port Enable/Disable Change (R/WC). 1: Port enable/disable status has changed. 0: No change.	
	PO_EN	2	Port Enable/Disable (R/W). 1: Enable. 0: Disable. Ports can only be enabled by the Host Controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field.	
	CONN_CHG	1	Connect Status Change (R/WC). 1: Change current connect status. 0: No change. This bit indicates a change has occurred in the port's current connect status.	
	CONN_STS	0	Current Connect Status (RO). 1: Device is present on the port. 0: No device is present. This value reflects the current state of the port, and may not correspond directly to cause the Connect Status Change bit to be set. When TST_FORCEEN is set to '1', this signal is the output of U_HDISCON.	
18h (102431h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	-	7:4	Reserved.	
	LINE_STS	3:2	Line Status (RO). These bits reflect the current logical levels of the D+	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			and D- signal lines.	
	-	1	Reserved.	
	PO_RESET	0	Port Reset. 1: Port is in reset. 0: Port is not in reset. When the software writes a one to this bit, the bus reset sequence as defined in the USB spec. is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence. Note: Before setting this bit, RUN/STOP bit should be set to 0.	
19h 102432h	**-**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	**7:1**	Reserved.	
	FORCE_TST_ENABLE	**0**	Force UHC enter test mode to issue test packet. The bit must set before clearing VBUS_OFF. Or it cannot enter test mode successfully.	
1Ah (102434h)	**HCMISC**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	U_SUSP_N	6	Transceiver Suspend Mode. Active LOW places the transceiver in suspend mode that draws minimal power from power supplies. This is part of the power management.	
	EOF2_TIME	5:4	EOF 2 Timing Points, controlling EOF 2 timing point before next SOF. High-Speed EOF2 Time: 00: 2 clocks (30 MHz) = 66ns. 01: 4 clocks (30 MHz) = 133ns. 10: 8 clocks (30 MHz) = 266ns. 11: 16 clocks (30 MHz) = 533ns. Full-Speed EOF2 Time: 00: 20 clocks (30 MHz) = 666ns. 01: 40 clocks (30 MHz) = 1.333us. 10: 80 clocks (30 MHz) = 2.66us. 11: 160 clocks (30 MHz) = 5.3us. Low-Speed EOF2 Time: 00: 40 clocks (30 MHz) = 1.33us. 01: 80 clocks (30 MHz) = 2.66us.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: 160 clocks (30 MHz) = 5.33us. 11: 320 clocks (30 MHz) = 10.66us.	
	EOF1_TIME	3:2	EOF 1 Timing Points, controlling EOF 1 timing point before next SOF. This value should be adjusted according to the maximum packet size. High-Speed EOF1 Time: 00: 6us. 01: 12us. 10: 24us. 11: 36us. Full-Speed EOF1 Time: 00: 53.3us. 01: 70.0us. 10: 86.0us. 11: 700us. Low-Speed EOF1 Time: 00: 3750 clocks (30 MHz) = 125us. 01: 3500 clocks (30 MHz) = 116us. 10: 3250 clocks (30 MHz) = 108us. 11: 4000 clocks (30 MHz) = 133us.	
	ASYN_SCH_SLPT	1:0	Asynchronous Schedule Sleep Timer, controlling the Asynchronous Schedule sleep timer. 00: 5us. 01: 10us. 10: 15us. 11: 20us.	
20h (102440h)	**BMCS**	**7:0**	**Default : 0x10**	**Access : R/W**
	FORCE_NO_CHIRP	7	Force Full/Low speed mode	
	-	6:5	Reserved (must be set to '0' at all times).	
	VBUS_OFF	4	VBUS Off. This bit controls the voltage on VBUS ON/OFF (Default is OFF) or in other words, the signal U_DRVBUS. 0: VBUS On. 1: VBUS Off.	
	INT_POLARITY	3	Control the polarity of system interrupt signal SYS_INT_N. 0: Active LOW (default). 1: Active HIGH.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HALF_SPEED	2	Half Speed Enable. 1: FIFO controller asserts ACK to DMA once every two clock cycles. 0: FIFO controller asserts ACK to DMA continuously. This bit is set to '1' while implementing FPGA.	
	HDISCON_FLT_SEL	1	Select a timer to filter out noise of HDISCON from UTMI+. 0: Approximated to 135 us. 1: Approximated to 270 us.	
	VBUS_FLT_SEL	0	Select a timer to filter out noise of VBUS_VLD from UTMI+. This signal is valid when signal U_VBUSVLD is connected. 0: Approximated to 135 us. 1: Approximated to 472 us.	
20h (102441h)	**BMCS**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	HOST_SPD_TYP	2:1	Host Speed Type, indicating speed type of the attached device. 10: HS. 00: FS. 01: LS. 11: Reserved.	
	VBUS_VLD	0	VBUS Valid. When the voltage on VBUS is above the valid VBUS threshold, this signal is valid when U_VBUSVLD is connected.	
22h (102444h)	**BUSMONINTSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:5	Reserved.	
	DMA_ERROR	4	DMA Error Interrupt. DMA operation cannot be finished normally, and an error signal is received. When CPU initiates DMA to fill up or read out device's FIFO, and DMA controller gets error response from system bus, this bit will be set. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DMA_CMPLT	3	DMA Completion Interrupt. DMA operation is finished normally. When CPU initiates DMA to fill up or read out device's FIFO, this	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			bit will be set after mission completion. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DPLGRMV	2	Device Plug Remove. This register is set to '1' once the device plug is removed. Writing '1' clears this register and writing '0' takes no effect.	
	OVC	1	Over Current Detection. This register is set to '1' when the VBUS does not reach VBUS_VLD within the expected time. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
	VBUS_ERR	0	VBUS Error. This register is set to '1' when the Bus Monitor state machine moves to "VBUS_ERROR" state. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
24h (102448h)	**BUSMONINTEN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMA_ERROR_EN	4	DMA_ERROR interrupt enable.	
	DMA_CMPLT_EN	3	DMA_CMPLT interrupt enable.	
	BPLGRMV_EN	2	BPLGRMV interrupt enable.	
	OVC_EN	1	OVC interrupt enable.	
	A_VBUS_ERR_EN	0	A_VBUS_ERR interrupt enable.	
28h (102450h)	**TST**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_LOOPBK	4	FIFO Loop Back Mode. A '1' turns on the loop-back mode. When this bit is set to '1', the Host Controller will enter the loop-back mode. During the loop-back mode, the Host Controller will use manual setting of DMA control to trigger DMA master.	
	TST_MOD	3	Test Mode. A '1' turns on the test mode. When this bit is set to '1', the Host Controller will enter the test mode. This test mode can save simulation time. In normal mode, the Host Controller uses a counter	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			for 10 ms detection of USB reset. The count is a large number. In test mode, the Host Controller will use a smaller number counter for USB reset detection to save the test cycle on test machine.	
	TST_PKT	2	Test Mode for Packet. Upon writing a '1' to this bit, the Host Controller repetitively sends the packet defined in UTMI spec. to transceiver. Run/Stop bit should also be enabled to enable the function.	
	TST_KSTA	1	Upon writing a '1', the D+/D- is set to the high-speed K state.	
	TST_JSTA	0	Upon writing a '1', the D+/D- is set to the high-speed J state.	
38h (102470h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DMA_IO	3	DMA IO to IO. Force DMA Controller not to toggle address. This bit is set when the DMA target is not a system memory but an IO device. If this register is set to '1', the 'DMA_LEN' must be an integer multiple of DWORD (4 byes), and the 'DMA_MADDR' must align to the boundary of DWORD (4 bytes).	
	-	2	Reserved.	
	DMA_TYPE	1	DMA Type, the transfer type of data moving. 0: FIFO to Memory. 1: Memory to FIFO.	
	DMA_START	0	DMA Start, informing DMA Controller to initiate DMA transfer. This bit is set to start the transfer and cleared when the DMA operation is completed. Note that this bit cannot be cleared by software; it can only be cleared by hardware in the case of either DMA completion or DMA error. Note that if DMA_LEN and DMA_START are set at the same time, the DMA_LEN will take effect immediately.	
38h (102471h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[7:0]	7:0	DMA Length.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			The total bytes the DMA Controller will move. The unit is byte. The maximum length could be 1024B-1.	
39h (102472h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[15:8]	7:0	See description of '71h'.	
39h (102473h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DMA_LEN[16]	0	See description of '71h'.	
3Ah (102474h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[7:0]	7:0	DMA Memory Address. The starting address of memory to request DMA transfer.	
3Ah (102475h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[15:8]	7:0	See description of '74h'.	
3Bh (102476h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[23:16]	7:0	See description of '74h'.	
3Bh (102477h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[31:24]	7:0	See description of '74h'.	
40h (102480h)	**PROJ_SPEC_REG0**	7:0	**Default: 0x00**	**Access: R/W, WO**
	-	7:5	Reserved.	
	SFT_CLK_RECOV	4	Clock recovery controlled by software. The register is R/W and the MIU clock will be always active if the bit is kept as 1.	
	OLD_XI2PV	3	Enables old version XIU access.	
	CLK_STOP	2	Triggers the clock stop mechanism. Set 1 to stop the all clock in UHC. The bit also represents the clock status of UHC. Reading the bit if it is 1, it represents the clock is stopped.	
	EN_RD_RD_SCRAMBLE	1	Enables memory inverted read.	
	EN_RD_WR_SCRAMBLE	0	Enables memory inverted write.	
40h (102481h)	**PROJ_SPEC_REG1**	**7:0**	**Default: 0x00**	**Access: R/W**
	SPLIT_SHORT_PKT_CLR_ACT	7	If the transfer is a periodic split transaction, the active status will be cleared when a short packet is received.	
	NON_ALIGN_EN	6	Enables MIU address non-alignment mode. It also means enabling new PV2MI bridge.	
	INVALID_MIU_ACS_INTEN	5	Enables interrupt when MIU invalid write occurs.	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MIU_WR_PROTECT_EN	4	Enables MIU write protect.	
	DAT_RD_PRI_EN	3	The enable option (MIU priority access) of the "data read".	
	DAT_WR_PRI_EN	2	The enable option (MIU priority access) of the "data write".	
	QT_RD_PRI_EN	1	The enable option (MIU priority access) of the "q-table read".	
	QT_WR_PRI_EN	0	The enable option (MIU priority access) of the "q-table write".	
41h (102482h)	**PROJ_SPEC_REG2**	**7:0**	**Default: 0x00**	**Access: R/W**
	QT_RD_PRI_SEL	7:6	The select (delay time of MIU priority assert) of the "q-table read". 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	QT_WR_PRI_SEL	5:4	The select (delay time of MIU priority assert) of the "q-table write". 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	DAT_RD_PRI_SEL	3:2	The select (delay time of MIU priority assert) of the "data read". 2'b00: 21.3us 2'b01: 16.0us 2'b10: 10.7us 2'b11: 5.3us	
	DAT_RD_PRI_SEL	1:0	The select (delay time of MIU priority assert) of the "data write". 2'b00: 21.3us 2'b01: 16.0us 2'b10: 10.7us 2'b11: 5.3us	
41h (102483h)	**PROJ_SPEC_REG3**	**7:0**	**Default: -**	**Access: R/W**
	Miu1_sel	7:6	2'b00: uh2mi_miu1_sel = uh2mi_adr[25] 2'b01: uh2mi_miu1_sel = uh2mi_adr[24] 2'b10: uh2mi_miu1_sel = uh2mi_adr[23]	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2'b11: uh2mi_miu1_sel = uh2mi_adr[22]	
	Reserved	5	Reserved	
	En_last_done	4	Enable the mechanism that UHC state machine will wait until the last write data is done (mi2uh_last_done_z) when in write memory cycle.	
	Periodic_pri_sel	3:2	The select (delay time of MIU priority assert) of the periodic (Isochronous an Interrupt) transfer. 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	periodic_high_pri_en	1	Enable option for MIU high priority when proceeding periodic (Isochronous and Interrupt) transfer.	
	eof1_high_pri_en	0	Enable MIU high priority mechanism when in EOF1 window.	
	STATUS_REG	**7:0**	**Default: 0x00**	
45h (10248Ah)	-	7:1	Reserved	**Access: R/W1C**
	INVALID_MIU_ACS	0	Interrupt status of invalid MIU write.	
46h (10248Ch)	**MIU_WRITE_RANGE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[7:0]	7:0	MIU write protect lower boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
46h (10248Dh)	**MIU_WRITE_RANGE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[15:8]	7:0	MIU write protect lower boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
47h (10248Eh)	**MIU_WRITE_RANGE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[23:16]	7:0	MIU write protect lower boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
47h (10248Fh)	**MIU_WRITE_RANGE3**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[7:0]	7:0	MIU write protect upper boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower	

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UHC0 Register (Bank = 1024)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			boundary address.	
48h (102490h)	**MIU_WRITE_RANGE4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[15:8]	7:0	MIU write protect upper boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (102491h)	**MIU_WRITE_RANGE5**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[23:16]	7:0	MIU write protect upper boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	

ADC_TOP Register (Bank = 1025)

ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102500h)	**REG102500**	**7:0**	**Default : 0x95**	**Access : R/W**
	PLLDIV[7:0]	7:0	ADC PLL divider ratio (Htotal-3). (Write sequence LSB -> MSB).	
00h (102501h)	**REG102501**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	PLLDIV[12:8]	4:0	See description of '102500h'.	
01h (102502h)	**REG102502**	**7:0**	**Default : 0x82**	**Access : R/W**
	BWCOEF[7:0]	7:0	ADC PLL bandwidth coefficient.	
01h (102503h)	**REG102503**	**7:0**	**Default : 0x09**	**Access : R/W**
	FREQCOEF[7:0]	7:0	ADC PLL frequency coefficient.	
02h (102504h)	**REG102504**	**7:0**	**Default : 0x05**	**Access : R/W**
	DAMPCOEF[7:0]	7:0	ADC PLL damping coefficient.	
04h (102508h)	**REG102508**	**7:0**	**Default : 0x05**	**Access : R/W**
	PLL_STATUS_SEL[2:0]	7:5	Select PLL digital status.	
	PHD_CAL_DIS	4	Disable phase digitalizer calibration.	
	SETTLE_CNT[3:0]	3:0	Select phase digitalizer settling time.	
04h	**REG102509**	**7:0**	**Default : 0xC6**	**Access : R/W**

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102509h)	WDOG_TOL[1:0]	7:6	Select PLL watch dog reset tolerance.	
	IQCLR_TH[2:0]	5:3	PLL lock to unlock threshold.	
	IQSET_TH[2:0]	2:0	PLL unlock to lock threshold.	
05h (10250Ah)	**REG10250A**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_STATUS[7:0]	7:0	PLL digital status. 000: {LOCK, IQ, SLOW, FAST, FREERUN, 3'b000}.	
07h (10250Eh)	**REG10250E**	**7:0**	**Default : 0x8A**	**Access : R/W**
	HSYNC_POL	7	Input HSYNC polarity. 0: Low active. 1: High active.	
	SOG_EN	6	Select PLL locking source. 0: HSYNC. 1: SOG.	
	HSYNC_EDGE	5	Select PLL locking edge. 0: HSYNC leading edge. 1: HSYNC trailing edge.	
	CLAMP_EDGE	4	Select clamp reference edge. 0: HSYNC trailing edge. 1: HSYNC leading edge.	
	CCDIS	3	1: Disable clamp during coast region.	
	WDOG_DIS	2	1: Disable ADC PLL watch dog.	
	COAST_POL	1	Select coast polarity. 0: Low active. 1: High active.	
	-	0	Reserved.	
07h (10250Fh)	**REG10250F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSOUT_PW[7:0]	7:0	Select extended HSOUT pulse width.	
08h (102511h)	**REG102511**	**7:0**	**Default : 0x05**	**Access : R/W**
	CLAMP_DUR[7:0]	7:0	Select clamp pulse duration.	
09h (102512h)	**REG102512**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HSOUT_GEN	1	1: Enable HSOUT pulse extension.	
	-	0	Reserved.	
0Bh (102516h)	**REG102516**	**7:0**	**Default : 0x40**	**Access : R/W**
	TIMEOUT_H[7:0]	7:0	HSYNC activity timeout period (100us).	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (102517h)	**REG102517**	**7:0**	**Default : 0x64**	**Access : R/W**
	TIMEOUT_V[7:0]	7:0	VSYNC activity timeout period (ms).	
0Ch (102518h)	**REG102518**	**7:0**	**Default : 0x00**	**Access : RO**
	OVF_RGBY[7:0]	7:0	ADC overflow flags, {OVFY, UNFY, OVFB, UNFB, OVFG, UNFG, OVFR, UNFR}.	
0Ch (102519h)	**REG102519**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:4	Reserved.	
	SOG_TOG	3	1: Active channel SOG toggle status.	
	VSYNC_TOG	2	1: Active channel VSYNC toggle status.	
	HSYNC_TOG	1	1: Active channel HSYNC toggle status.	
	CLROVF_RGBY	0	Write a 1 to clear ADC_RGBY overflow flags.	
0Dh (10251Ah)	**REG10251A**	**7:0**	**Default : 0x05**	**Access : R/W**
	CLAMP_DLY[7:0]	7:0	Select clamp pulse start position relative to input HSYNC edge.	
0Dh (10251Bh)	**REG10251B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VCLAMP_EN_HACT	5	1: Enable HACT window.	
	VCLAMP_HSYNC_OR_HSOUT	4	0: Use HSYNC, 1: use HSOUT.	
	CLAMP_DLY[11:8]	3:0	See description of '10251Ah'.	
10h (102520h)	**REG102520**	**7:0**	**Default : 0x88**	**Access : R/W**
	RGBY_SWAP[7:0]	7:0	Select RGBY data to scalar. [2:0]: SEL R. [5:3]: SEL G. [8:6]: SEL B. [11:9]: SEL Y. 000: R. 001: G. 010: B. 011: Y. 1xx: Blank.	
10h (102521h)	**REG102521**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:4	Reserved.	
	RGBY_SWAP[11:8]	3:0	See description of '102520h'.	
12h	**REG102524**	**7:0**	**Default : 0x00**	**Access : R/W**

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102524h)	YMIDA[1:0]	7:6	0/1=select gnd-clamp/mid-clamp for ADC Y. 00: 10h000. 01: 10h040. 10: 10h200.	
	BMIDA[1:0]	5:4	0/1=select gnd-clamp/mid-clamp for ADC B. 00: 10h000. 01: 10h040. 10: 10h200.	
	GMIDA[1:0]	3:2	0/1=select gnd-clamp/mid-clamp for ADC G. 00: 10h000. 01: 10h040. 10: 10h200.	
	RMIDA[1:0]	1:0	0/1=select gnd-clamp/mid-clamp for ADC R. 00: 10h000. 01: 10h040. 10: 10h200.	
12h (102525h)	**REG102525**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	HSOUT2SC_PIPEDLY[3:0]	5:2	Hsout pipe delay 1~16=0~F.	
	SYNC_SEL_YUV	1	Yuv sync sel 1:VD 0:scalar.	
	SYNC_SEL_RGB	0	Rgb sync sel 1:VD 0:scalar.	
13h (102526h)	**REG102526**	**7:0**	**Default : 0x84**	**Access : R/W**
	-	7:3	Reserved.	
	DIT_DISP[2:0]	2:0	Select ADC RGB dither mode for display.	
14h (102528h)	**REG102528**	**7:0**	**Default : 0x28**	**Access : R/W**
	VSSEP_TH[7:0]	7:0	Select VSYNC separator threshold width (unit=XTAL period*2).	
14h (102529h)	**REG102529**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	CAL_BW	6	1: Enable max ADC bandwidth during CAL.	
	SYNC_SEL	5	Select sync source for ADC_DIG. 0: From scalar. 1: From ADC sync process block.	
	COAST_EN	4	Enable coast generator. 0: Disable coast. 1: Enable coast.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COAST_HS	3	Select HSYNC sources for coast line counter. 0: PLL locked HSOUT. 1: Input HSYNC.	
	VSYNC_POL	2	Input VSYNC polarity. 0: Low active. 1: High active.	
	VS_SEL	1	Select VSYNC input source. 0: VSYNC. 1: Separated VSYNC.	
	VSSEP_SEL	0	Select VSYNC separator input source. 0: HSYNC or SOG. 1: VSYNC.	
15h (10252Ah)	**REG10252A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRECOAST[7:0]	7:0	Select PRECOAST lines before VSYNC.	
15h (10252Bh)	**REG10252B**	**7:0**	**Default : 0x00**	**Access : R/W**
	POSTCOAST[7:0]	7:0	Select POSTCOAST lines after VSYNC.	
16h (10252Ch)	**REG10252C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIT_DISP_YUV[1:0]	7:6	Select ADC YUV dither mode for display.	
	-	5:3	Reserved.	
	LAT_SYNC_DLY_SEL[2:0]	2:0	Select postcoast lines after VSYNC.	
16h (10252Dh)	**REG10252D**	**7:0**	**Default : 0x55**	**Access : R/W**
	-	7:1	Reserved.	
	DIT_DISP_YUV[2]	0	See description of '10252Ch'.	
17h (10252Eh)	**REG10252E**	**7:0**	**Default : 0x14**	**Access : R/W**
	ICLAMP_CLPDLY[7:0]	7:0	Register setting for delay. (to start of analog clamp).	
17h (10252Fh)	**REG10252F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_CLPDLY[11:8]	3:0	See description of '10252Eh'.	
18h (102530h)	**REG102530**	**7:0**	**Default : 0x08**	**Access : R/W**
	ICLAMP_CALDUR[7:0]	7:0	Register setting for duration, only for 2^N. (of analog clamp).	
18h (102531h)	**REG102531**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_VEN	3	1=enable clamp once every vsync.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ICLAMP_COAST_CLP_DIS	2	1 = disable clamp during COAST region (synced).	
	ICLAMP_HSYNC_OR_HSOUT	1	0: Use HSYNC, 1: use HSOUT.	
	ICLAMP_CLP_EDGE	0	1: Raising edge, 0:falling edge.	
19h (102532h)	**REG102532**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICLAMP_VDLY[7:0]	7:0	Clamp pulse line delay for vsync mode.	
19h (102533h)	**REG102533**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICLAMP_CLK_RATE_IN	7	Analog iclamp clk polarity, 0:pass, 1:inverit.	
	ICLAMP_CLK_RATE[1:0]	6:5	00: X1 Analog ICLAMP. 01: X2. 10: X4. 11: X4.	
	ICLAMP_COAST_EXT_CNT[2:0]	4:2	Coast extend 0~7 line option.	
	ICLAMP_EN_COAST_EXT_CNT	1	1: Enable coast extend 0~7 line option.	
	ICLAMP_EN_HACT	0	1: Enable HACT window.	
21h (102542h)	**REG102542**	**7:0**	**Default : 0x80**	**Access : R/W**
	ICLAMP_R_BLANK_LVL[7:0]	7:0	Blanking level = 128 (RGB).	
21h (102543h)	**REG102543**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_R_BLANK_LVL[11:8]	3:0	See description of '102542h'.	
22h (102544h)	**REG102544**	**7:0**	**Default : 0x05**	**Access : R/W**
	ICLAMP_R_LOCK_LEVEL[7:0]	7:0	Lock level threshold.	
22h (102545h)	**REG102545**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_R_LOCK_LEVEL[11:8]	3:0	See description of '102544h'.	
23h (102546h)	**REG102546**	**7:0**	**Default : 0xD0**	**Access : R/W**
	ICLAMP_R_LOCK_CNT[7:0]	7:0	Match REG_ICLAMP_LOCK_LEVEL counter.	
23h (102547h)	**REG102547**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_R_LOCK_CNT[12:8]	4:0	See description of '102546h'.	
24h (102548h)	**REG102548**	**7:0**	**Default : 0x60**	**Access : R/W**
	ICLAMP_R_K1_STB[0]	7	K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Stable.	
	ICLAMP_R_K1_INI[6:0]	6:0	K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Initial.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (102549h)	**REG102549**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ICLAMP_R_K1_STB[6:1]	5:0	See description of '102548h'.	
25h (10254Ah)	**REG10254A**	**7:0**	**Default : 0xA0**	**Access : R/W**
	ICLAMP_R_K1_EN	7	Clamping = leakage + err * gain_true * k1 * k1_en;	
	ICLAMP_R_K2[6:0]	6:0	K2 = 2^(CLMP_K2[6:3]-8) * (1 + CLMP_K2[2:0]/8);	
25h (10254Bh)	**REG10254B**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_R_FREZ_CLMP[2:0]	4:2	Clamping = leakage. Leakage is frozen. (Coast). K1_en = 0 and k2_en = 0. FREZ_CLMP = FREZ_CLMP_1 | FREZ_CLMP_2 | FREZ_CLMP_3;	
	ICLAMP_R_TYPE	1	0: Bottom clamping, RGB/YPbPr = 0; 1: Back-porch calmping.	
	ICLAMP_R_K2_EN	0	Leakage = leakage + err * gain_true * k1 * k2 * k2_en;	
26h (10254Ch)	**REG10254C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICLAMP_R_AGC_FINE[7:0]	7:0	Agc fine gain.	
26h (10254Dh)	**REG10254D**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	
	ICLAMP_R_AGC_COARSE[1:0]	5:4	Agc coarse gain.	
	ICLAMP_R_AGC_FINE[11:8]	3:0	See description of '10254Ch'.	
27h (10254Eh)	**REG10254E**	**7:0**	**Default : 0x40**	**Access : R/W**
	ICLAMP_R_PGA_OFST[7:0]	7:0	Pga offset.	
27h (10254Fh)	**REG10254F**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_R_ERR_MAX[4:0]	4:0	Bac_porch_level error < +- REG_CLMP_ERR_MAX <= +-31 * 8 !!!.	
28h	**REG102550**	**7:0**	**Default : 0x4A**	**Access : R/W**

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102550h)	ICLAMP_R_LKG_MODE[1:0]	7:6	001: Adaptive leakage tracking. 001: Adaptive leakage tracking. Leakage is bounded by +- REG_ICLAMP_LKG[4:0]. 010: Freeze leakage. 011: Load leakage = REG_ICLAMP_LKG[5] * REG_CLMP_LKG[4:0]; 100: Load K1'accu into leakage for quickly 1st order update.	
	ICLAMP_R_LKG[5:0]	5:0	[5]: Sign bit. 0: Posetive. 1: Negative. [4:0] : magnitude. 0 ~ 31 LSB of +-10uA/32. See REG_ICLAMP_LKG_MODE.	
28h (102551h)	**REG102551**	**7:0**	**Default : 0x08**	**Access : R/W**
	ICLAMP_R_DLKG_MAX[5:0]	7:2	Delta_leakage is bounded by +- (REG_CLMP_DLKG_MAX / 512). +- 1/8.	
	ICLAMP_R_FREZ_ZERO	1	1: Set CLMP_DSM = 0 when FREZ. 0: Set CLMP_DSM = lkg when FREZ.	
	ICLAMP_R_LKG_MODE[2]	0	See description of '102550h'.	
29h (102552h)	**REG102552**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ICLAMP_R_2DSM	1	1: 2nd-order. 0: 1st-order.	
	ICLAMP_R_FREZ_DSM	0	1: Delta-sigma frozen. CLAMP_fpga/chip[5:0] = round{CLMP_DSM[15:10]+CLMP_DSM[9]}. 0: Delta-sigma on.	
2Bh (102556h)	**REG102556**	**7:0**	**Default : 0x80**	**Access : R/W**
	ICLAMP_G_BLANK_LVL[7:0]	7:0	Blanking level = 128 (RGB).	
2Bh (102557h)	**REG102557**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_G_BLANK_LVL[11:8]	3:0	See description of '102556h'.	
2Ch (102558h)	**REG102558**	**7:0**	**Default : 0x05**	**Access : R/W**
	ICLAMP_G_LOCK_LEVEL[7:0]	7:0	Lock level threshold.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Ch (102559h)	**REG102559**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_G_LOCK_LEVEL[11:8]	3:0	See description of '102558h'.	
2Dh (10255Ah)	**REG10255A**	**7:0**	**Default : 0xD0**	**Access : R/W**
	ICLAMP_G_LOCK_CNT[7:0]	7:0	Match REG_ICLAMP_LOCK_LEVEL counter.	
2Dh (10255Bh)	**REG10255B**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_G_LOCK_CNT[12:8]	4:0	See description of '10255Ah'.	
2Eh (10255Ch)	**REG10255C**	**7:0**	**Default : 0x60**	**Access : R/W**
	ICLAMP_G_K1_STB[0]	7	K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Stable.	
	ICLAMP_G_K1_INI[6:0]	6:0	K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Initial.	
2Eh (10255Dh)	**REG10255D**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ICLAMP_G_K1_STB[6:1]	5:0	See description of '10255Ch'.	
2Fh (10255Eh)	**REG10255E**	**7:0**	**Default : 0xA0**	**Access : R/W**
	ICLAMP_G_K1_EN	7	Clamping = leakage + err * gain_true * k1 * k1_en;	
	ICLAMP_G_K2[6:0]	6:0	K2 = 2^(CLMP_K2[6:3]-8) * (1 + CLMP_K2[2:0]/8);	
2Fh (10255Fh)	**REG10255F**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_G_FREZ_CLMP[2:0]	4:2	Clamping = leakage. Leakage is frozen. (Coast). K1_en = 0 and k2_en = 0. FREZ_CLMP = FREZ_CLMP_1 | FREZ_CLMP_2 | FREZ_CLMP_3;	
	ICLAMP_G_TYPE	1	0: Bottom clamping, RGB/YPbPr = 0; 1: Back-porch calmping.	
	ICLAMP_G_K2_EN	0	Leakage = leakage + err * gain_true * k1 * k2 * k2_en;	
30h (102560h)	**REG102560**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICLAMP_G_AGC_FINE[7:0]	7:0	Agc fine gain.	
30h (102561h)	**REG102561**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ICLAMP_G_AGC_COARSE[1:0]	5:4	Agc coarse gain.	
	ICLAMP_G_AGC_FINE[11:8]	3:0	See description of '102560h'.	
31h (102562h)	**REG102562**	**7:0**	**Default : 0x40**	**Access : R/W**
	ICLAMP_G_PGA_OFST[7:0]	7:0	Pga offset.	
31h (102563h)	**REG102563**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_G_ERR_MAX[4:0]	4:0	Bac_porch_level error < +- REG_CLMP_ERR_MAX <= +-31 * 8 !!!.	
32h (102564h)	**REG102564**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ICLAMP_G_LKG_MODE[1:0]	7:6	001: Adaptive leakage tracking. 001: Adaptive leakage tracking. Leakage is bounded by +- REG_ICLAMP_LKG[4:0]. 010: Freeze leakage. 011: Load leakage = REG_ICLAMP_LKG[5] * REG_CLMP_LKG[4:0]; 100: Load K1'accu into leakage for quickly 1st order update.	
	ICLAMP_G_LKG[5:0]	5:0	[5]: Sign bit. 0: Posetive. 1: Negative. [4:0] : magnitude. 0 ~ 31 LSB of +-10uA/32. See REG_ICLAMP_LKG_MODE.	
32h (102565h)	**REG102565**	**7:0**	**Default : 0x08**	**Access : R/W**
	ICLAMP_G_DLKG_MAX[5:0]	7:2	Delta_leakage is bounded by +- (REG_CLMP_DLKG_MAX / 512). +- 1/8.	
	ICLAMP_G_FREZ_ZERO	1	1: Set CLMP_DSM = 0 when FREZ. 0: Set CLMP_DSM = lkg when FREZ.	
	ICLAMP_G_LKG_MODE[2]	0	See description of '102564h'.	
33h (102566h)	**REG102566**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ICLAMP_G_2DSM	1	1: 2nd-order. 0: 1st-order.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ICLAMP_G_FREZ_DSM	0	1: Delta-sigma frozen. CLAMP_fpga/chip[5:0] = round{CLMP_DSM[15:10]+CLMP_DSM[9]}. 0: Delta-sigma on.	
35h (10256Ah)	**REG10256A**	**7:0**	**Default : 0x80**	**Access : R/W**
	ICLAMP_B_BLANK_LVL[7:0]	7:0	Blanking level = 128 (RGB).	
35h (10256Bh)	**REG10256B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_B_BLANK_LVL[11:8]	3:0	See description of '10256Ah'.	
36h (10256Ch)	**REG10256C**	**7:0**	**Default : 0x05**	**Access : R/W**
	ICLAMP_B_LOCK_LEVEL[7:0]	7:0	Lock level threshold.	
36h (10256Dh)	**REG10256D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ICLAMP_B_LOCK_LEVEL[11:8]	3:0	See description of '10256Ch'.	
37h (10256Eh)	**REG10256E**	**7:0**	**Default : 0xD0**	**Access : R/W**
	ICLAMP_B_LOCK_CNT[7:0]	7:0	Match REG_ICLAMP_LOCK_LEVEL counter.	
37h (10256Fh)	**REG10256F**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_B_LOCK_CNT[12:8]	4:0	See description of '10256Eh'.	
38h (102570h)	**REG102570**	**7:0**	**Default : 0x60**	**Access : R/W**
	ICLAMP_B_K1_STB[0]	7	K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Stable.	
	ICLAMP_B_K1_INI[6:0]	6:0	K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Initial.	
38h (102571h)	**REG102571**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ICLAMP_B_K1_STB[6:1]	5:0	See description of '102570h'.	
39h (102572h)	**REG102572**	**7:0**	**Default : 0xA0**	**Access : R/W**
	ICLAMP_B_K1_EN	7	Clamping = leakage + err * gain_true * k1 * k1_en;	
	ICLAMP_B_K2[6:0]	6:0	K2 = 2^(CLMP_K2[6:3]-8) * (1 + CLMP_K2[2:0]/8);	
39h (102573h)	**REG102573**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:5	Reserved.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ICLAMP_B_FREZ_CLMP[2:0]	4:2	Clamping = leakage. Leakage is frozen. (Coast). K1_en = 0 and k2_en = 0. FREZ_CLMP = FREZ_CLMP_1 | FREZ_CLMP_2 | FREZ_CLMP_3;	
	ICLAMP_B_TYPE	1	0: Bottom clamping, RGB/YPbPr = 0; 1: Back-porch calmping.	
	ICLAMP_B_K2_EN	0	Leakage = leakage + err * gain_true * k1 * k2 * k2_en;	
3Ah (102574h)	**REG102574**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICLAMP_B_AGC_FINE[7:0]	7:0	Agc fine gain.	
3Ah (102575h)	**REG102575**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	
	ICLAMP_B_AGC_COARSE[1:0]	5:4	Agc coarse gain.	
	ICLAMP_B_AGC_FINE[11:8]	3:0	See description of '102574h'.	
3Bh (102576h)	**REG102576**	**7:0**	**Default : 0x40**	**Access : R/W**
	ICLAMP_B_PGA_OFST[7:0]	7:0	Pga offset.	
3Bh (102577h)	**REG102577**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	ICLAMP_B_ERR_MAX[4:0]	4:0	Bac_porch_level error < +- REG_CLMP_ERR_MAX <= +-31 * 8 !!!.	
3Ch (102578h)	**REG102578**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ICLAMP_B_LKG_MODE[1:0]	7:6	001: Adaptive leakage tracking. 001: Adaptive leakage tracking. Leakage is bounded by +- REG_ICLAMP_LKG[4:0]. 010: Freeze leakage. 011: Load leakage = REG_ICLAMP_LKG[5] * REG_CLMP_LKG[4:0]; 100: Load K1'accu into leakage for quickly 1st order update.	
	ICLAMP_B_LKG[5:0]	5:0	[5]: Sign bit. 0: Posetive. 1: Negative. [4:0] : magnitude. 0 ~ 31 LSB of +-10uA/32. See REG_ICLAMP_LKG_MODE.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ch (102579h)	**REG102579**	**7:0**	**Default : 0x08**	**Access : R/W**
	ICLAMP_B_DLKG_MAX[5:0]	7:2	Delta_leakage is bounded by +- (REG_CLMP_DLKG_MAX / 512). +- 1/8.	
	ICLAMP_B_FREZ_ZERO	1	1: Set CLMP_DSM = 0 when FREZ. 0: Set CLMP_DSM = lkg when FREZ.	
	ICLAMP_B_LKG_MODE[2]	0	See description of '102578h'.	
3Dh (10257Ah)	**REG10257A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ICLAMP_B_2DSM	1	1: 2nd-order. 0: 1st-order.	
	ICLAMP_B_FREZ_DSM	0	1: Delta-sigma frozen. CLAMP_fpga/chip[5:0] = round{CLMP_DSM[15:10]+CLMP_DSM[9]}. 0: Delta-sigma on.	
4Dh (10259Ah)	**REG10259A**	**7:0**	**Default : 0x20**	**Access : R/W**
	HACT_DELAY[7:0]	7:0	Delay for HSOUT pulse.	
4Dh (10259Bh)	**REG10259B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HACT_DELAY[11:8]	3:0	See description of '10259Ah'.	
4Eh (10259Ch)	**REG10259C**	**7:0**	**Default : 0x20**	**Access : R/W**
	HACT_DURATION[7:0]	7:0	Duration for HACT window.	
4Eh (10259Dh)	**REG10259D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HACT_DURATION[11:8]	3:0	See description of '10259Ch'.	
50h (1025A0h)	**REG1025A0**	**7:0**	**Default : 0x80**	**Access : R/W**
	UG_R_BLACK_LEVEL[7:0]	7:0	Black level(12).	
50h (1025A1h)	**REG1025A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_R_PIX_SEL[2:0]	6:4	Pixel select.	
	UG_R_BLACK_LEVEL[11:8]	3:0	See description of '1025A0h'.	
51h (1025A2h)	**REG1025A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_R_USER_GAIN[7:0]	7:0	User gain(14.12).	
51h	**REG1025A3**	**7:0**	**Default : 0x10**	**Access : R/W**

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1025A3h)	-	7:6	Reserved.	
	UG_R_USER_GAIN[13:8]	5:0	See description of '1025A2h'.	
52h (1025A4h)	**REG1025A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_R_USER_OFFSET[7:0]	7:0	User offset (S12).	
52h (1025A5h)	**REG1025A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_R_DIT_MODE[1:0]	6:5	00: Round, 01:truncate, 10:dithering.	
	UG_R_USER_OFFSET[12:8]	4:0	See description of '1025A4h'.	
55h (1025AAh)	**REG1025AA**	**7:0**	**Default : 0x80**	**Access : R/W**
	UG_G_BLACK_LEVEL[7:0]	7:0	Black level(12).	
55h (1025ABh)	**REG1025AB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_G_PIX_SEL[2:0]	6:4	Pixel select.	
	UG_G_BLACK_LEVEL[11:8]	3:0	See description of '1025AAh'.	
56h (1025ACh)	**REG1025AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_G_USER_GAIN[7:0]	7:0	User gain(14.12).	
56h (1025ADh)	**REG1025AD**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	UG_G_USER_GAIN[13:8]	5:0	See description of '1025ACh'.	
57h (1025AEh)	**REG1025AE**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_G_USER_OFFSET[7:0]	7:0	User offset (S12).	
57h (1025AFh)	**REG1025AF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_G_DIT_MODE[1:0]	6:5	00: Round, 01:truncate, 10:dithering.	
	UG_G_USER_OFFSET[12:8]	4:0	See description of '1025AEh'.	
5Ah (1025B4h)	**REG1025B4**	**7:0**	**Default : 0x80**	**Access : R/W**
	UG_B_BLACK_LEVEL[7:0]	7:0	Black level(12).	
5Ah (1025B5h)	**REG1025B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_B_PIX_SEL[2:0]	6:4	Pixel select.	
	UG_B_BLACK_LEVEL[11:8]	3:0	See description of '1025B4h'.	
5Bh (1025B6h)	**REG1025B6**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_B_USER_GAIN[7:0]	7:0	User gain(14.12).	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Bh (1025B7h)	**REG1025B7**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	UG_B_USER_GAIN[13:8]	5:0	See description of '1025B6h'.	
5Ch (1025B8h)	**REG1025B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_B_USER_OFFSET[7:0]	7:0	User offset (S12).	
5Ch (1025B9h)	**REG1025B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_B_DIT_MODE[1:0]	6:5	00: Round, 01:truncate, 10:dithering.	
	UG_B_USER_OFFSET[12:8]	4:0	See description of '1025B8h'.	
60h (1025C0h)	**REG1025C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_Y_BLACK_LEVEL[7:0]	7:0	Black level(12).	
60h (1025C1h)	**REG1025C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_Y_PIX_SEL[2:0]	6:4	Pixel select.	
	UG_Y_BLACK_LEVEL[11:8]	3:0	See description of '1025C0h'.	
61h (1025C2h)	**REG1025C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_Y_USER_GAIN[7:0]	7:0	User gain(14.12).	
61h (1025C3h)	**REG1025C3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	UG_Y_USER_GAIN[13:8]	5:0	See description of '1025C2h'.	
62h (1025C4h)	**REG1025C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	UG_Y_USER_OFFSET[7:0]	7:0	User offset (S12).	
62h (1025C5h)	**REG1025C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UG_Y_DIT_MODE[1:0]	6:5	00: Round, 01:truncate, 10:dithering.	
	UG_Y_USER_OFFSET[12:8]	4:0	See description of '1025C4h'.	
63h (1025C6h)	**REG1025C6**	**7:0**	**Default : 0x0F**	**Access : R/W**
	UG_RGB_EN[0]	7	Enable UG_BLACK/UG_GAIN/UG_OFFSET register.	
	UG_RGB_OV	6	Override UG_BLACK/UG_GAIN/UG_OFFSET.	
	UG_RGB_LD_VD_DLY[5:0]	5:0	Delay for Load VD fine gain.	
63h (1025C7h)	**REG1025C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	UG_RGB_EN[2:1]	1:0	See description of '1025C6h'.	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
64h (1025C8h)	**REG1025C8**	**7:0**	**Default : 0x0F**	**Access : R/W**
	UG_Y_EN[0]	7	Enable UG_BLACK/UG_GAIN/UG_OFFSET register.	
	UG_Y_OV	6	Override UG_BLACK/UG_GAIN/UG_OFFSET.	
	UG_Y_LD_VD_DLY[5:0]	5:0	Delay for Load VD fine gain.	
64h (1025C9h)	**REG1025C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	UG_Y_EN[2:1]	1:0	See description of '1025C8h'.	
65h (1025CAh)	**REG1025CA**	**7:0**	**Default : 0x33**	**Access : R/W**
	ANALOG_PGA_GAIN_G[3:0]	7:4	ADC Gain control: 4'b0000 : 14/5 (Vin=0.5Vpp). 4'b0001 : 14/5 (Vin=0.6Vpp). 4'b0010 : 14/5 (Vin=0.7Vpp). . . 4'b1111 : 14/20 (Vin=2.0Vpp).	
	ANALOG_PGA_GAIN_R[3:0]	3:0	ADC Gain control: 4'b0000 : 14/5 (Vin=0.5Vpp). 4'b0001 : 14/5 (Vin=0.6Vpp). 4'b0010 : 14/5 (Vin=0.7Vpp). . . 4'b1111 : 14/20 (Vin=2.0Vpp).	
65h (1025CBh)	**REG1025CB**	**7:0**	**Default : 0x33**	**Access : R/W**
	ANALOG_PGA_GAIN_Y[3:0]	7:4	ADC Gain control: 4'b0000 : 14/5 (Vin=0.5Vpp). 4'b0001 : 14/5 (Vin=0.6Vpp). 4'b0010 : 14/5 (Vin=0.7Vpp). . . 4'b1111 : 14/20 (Vin=2.0Vpp).	
	ANALOG_PGA_GAIN_B[3:0]	3:0	ADC Gain control: 4'b0000 : 14/5 (Vin=0.5Vpp). 4'b0001 : 14/5 (Vin=0.6Vpp). 4'b0010 : 14/5 (Vin=0.7Vpp). . . 4'b1111 : 14/20 (Vin=2.0Vpp).	

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ADC_TOP Register (Bank = 1025)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
68h (1025D0h)	**REG1025D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FIFO_BYPASS_Y	3	1=fifo bypass mode for y.	
	FIFO_BYPASS_RGB	2	1=fifo bypass mode for rgb.	
	-	1:0	Reserved.	
74h (1025E8h)	**REG1025E8**	**7:0**	**Default : 0x05**	**Access : R/W**
	MASK_DELAY[7:0]	7:0	Delay for HSOUT/HSYNC pulse.	
74h (1025E9h)	**REG1025E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MASK_EN	4	Enable blank ADC for CAL.	
	MASK_DELAY[11:8]	3:0	See description of '1025E8h'.	
75h (1025EAh)	**REG1025EA**	**7:0**	**Default : 0x05**	**Access : R/W**
	MASK_DURATION[7:0]	7:0	Duration for MASK window.	
75h (1025EBh)	**REG1025EB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MASK_COAST	7	1=enable mask data by coast.	
	MASK_CDIS	6	1=disable mask during coast.	
	MASK_HSYNC_OR_HSOUT	5	0: HSYNC, 1:HSOU.	
	MASK_EDGE	4	Select mask HSYNC start edge, 1: HSYNC rising edge, 0:falling edge.	
	MASK_DURATION[11:8]	3:0	See description of '1025EAh'.	
7Fh (1025FEh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

ADC_DTOP Register (Bank = 1026)

ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102600h)	**REG102600**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCB_TOGV2	7	1=ADC B channel interleaving every 2 VSYNC.	
	ADCB_TOGH2	6	1=ADC G channel interleaving every 2 VSYNC.	
	ADCG_TOGV2	5	1=ADC R channel interleaving every 2 VSYNC.	
	ADCG_TOGH2	4	1=ADC B channel interleaving every 2 HSYNC.	
	ADCR_TOGV2	3	1=ADC G channel interleaving every 2 HSYNC.	

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ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADCR_TOGH2	2	1=ADC R channel interleaving every 2 HSYNC.	
	RGB_NO_VRAND	1	1=no ADCA interleve V dithering.	
	RGB_NO_RAND	0	1=no ADCA interleve H/V dithering.	
01h (102602h)	**REG102602**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	RGB_INT_V_POLARITY	1	1=ADCA interleave vsync reference pulse polarity high.	
	RGB_INT_H_POLARITY	0	1=ADCA interleave hsync reference pulse polarity high.	
02h (102604h)	**REG102604**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_REF_CYC[7:0]	7:0	ADCA calibration trigger reference pulse cycle number.	
02h (102605h)	**REG102605**	**7:0**	**Default : 0x18**	**Access : R/W, WO**
	-	7:6	Reserved.	
	RGB_SELF_CAL_ALL_GAIN	5	1=ADCA calibration all gain mode enable.	
	RGB_SELF_CAL_MODE[1:0]	4:3	[0]=1: ADCA linear calibration enable. [1]=1: ADCA offset/gain calibration enable.	
	RGB_SELF_CAL_STOP	2	1=ADCA calibration stop in live mode.	
	RGB_SELF_CAL_LIVE	1	1=ADCA calibration live mode enable.	
	RGB_SELF_CAL_START	0	1=ADCA calibration start.	
03h (102606h)	**REG102606**	**7:0**	**Default : 0x10**	**Access : R/W**
	RGB_SELF_CAL_DLY[7:0]	7:0	ADCA claibration delay from reference pulse to linear/offset/gain calibration state.	
03h (102607h)	**REG102607**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_LIVE_WAIT_DLY[7:0]	7:0	ADCA claibration wait delay number of reference pulse before re-starting new calibration in live mode.	
04h (102608h)	**REG102608**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_SELF_CAL_GPUSE_SEL	3	1=ADCA SELF_CAL_G active high during linear calibration & gain calibration; Otherwise, ADCA SELF_CAL_G active high only during linear calibration.	
	RGB_SELF_CAL_BYPASS[2:0]	2:0	[0]=1: bypass ADC R calibration. [1]=1: bypass ADC G calibration. [2]=1: bypass ADC B calibration.	

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ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (10260Ch)	**REG10260C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RGB_LINEAR_CAL_MODE	0	1=ADCA linear calibration long mode.	
06h (10260Dh)	**REG10260D**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RGB_LINEAR_CAL_VREF_SEL[3:0]	7:4	ADCA VCAL setting during linear calibration.	
	RGB_LINEAR_CAL_PGA[3:0]	3:0	ADCA PGA setting during linear calibration.	
07h (10260Eh)	**REG10260E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ADCB_LCAL_EN	2	1=ADC B linear calibration update enable.	
	ADCG_LCAL_EN	1	1=ADC G linear calibration update enable.	
	ADCR_LCAL_EN	0	1=ADC R linear calibration update enable.	
08h (102610h)	**REG102610**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RGB_LINEAR_CAL_DLY[7:0]	7:0	ADCA linear calibration delay samples after reference pulse rising.	
08h (102611h)	**REG102611**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_LINEAR_CAL_DLY[11:8]	3:0	See description of '102610h'.	
09h (102612h)	**REG102612**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RGB_LINEAR_CAL_DUR[7:0]	7:0	ADCA linear calibration duration samples after reference pulse rising.	
12h (102624h)	**REG102624**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ADCB_OCAL_EN	3	1=ADC B offset calibration update enable.	
	ADCG_OCAL_EN	2	1=ADC G offset calibration update enable.	
	ADCR_OCAL_EN	1	1=ADC R offset calibration update enable.	
	RGB_OFFSET_CAL_MODE	0	1=ADCA offset calibration long mode.	
13h (102626h)	**REG102626**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RGB_OFFSET_CAL_DLY[7:0]	7:0	ADCA offset calibration delay samples after reference pulse rising.	
13h (102627h)	**REG102627**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_OFFSET_CAL_DLY[11:8]	3:0	See description of '102626h'.	
14h	**REG102628**	**7:0**	**Default : 0xFF**	**Access : R/W**

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ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102628h)	RGB_OFFSET_CAL_DUR[7:0]	7:0	ADCA offset calibration duration samples after reference pulse rising.	
1Fh (10263Eh)	**REG10263E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RGB_GAIN_CAL_MISMATCH_ONLY	4	1=ADCA gain calibration only calibrate channel0/channel1 mismatch.	
	ADCB_GCAL_EN	3	1=ADC B gain calibration update enable.	
	ADCG_GCAL_EN	2	1=ADC G gain calibration update enable.	
	ADCR_GCAL_EN	1	1=ADC R gain calibration update enable.	
	RGB_GAIN_CAL_MODE	0	1=ADCA gain calibration long mode.	
20h (102640h)	**REG102640**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RGB_GAIN_CAL_DLY[7:0]	7:0	ADCA gain calibration delay samples after reference pulse rising.	
20h (102641h)	**REG102641**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_GAIN_CAL_DLY[11:8]	3:0	See description of '102640h'.	
21h (102642h)	**REG102642**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RGB_GAIN_CAL_DUR[7:0]	7:0	ADCA gain calibration duration samples after reference pulse rising.	
21h (102643h)	**REG102643**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RGB_GAIN_CAL_DUR[15:8]	7:0	See description of '102642h'.	
3Fh (10267Eh)	**REG10267E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_GAIN_CAL_LVREF[3:0]	7:4	ADCA gain calibration low VCAL write value.	
	RGB_GAIN_CAL_HVREF[3:0]	3:0	ADCA gain calibration high VCAL write value.	
3Fh (10267Fh)	**REG10267F**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	RGB_GAIN_CAL_VREF_WP	7	ADCA gain calibration VCAL write enable.	
	-	6:4	Reserved.	
	RGB_GAIN_CAL_VREF_WG[3:0]	3:0	ADCA gain calibration VCAL write related gain setting.	
40h (102680h)	**REG102680**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_GAIN_CAL_TARGET[7:0]	7:0	ADCA gain calibration VCAL_HIGH-VCAL_LOW target digital code write value.	
40h (102681h)	**REG102681**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_GAIN_CAL_TARGET[11:8]	3:0	See description of '102680h'.	

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ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102682h)	**REG102682**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	RGB_GAIN_CAL_TARGET_WP	7	ADCA gain calibration (VCAL_HIGH-VCAL_LOW) target digital code write enable.	
	-	6:4	Reserved.	
	RGB_GAIN_CAL_TARGET_WG[3:0]	3:0	ADCA gain calibration VCAL_HIGH-VCAL_LOW target digital code write related gain setting.	
51h (1026A2h)	**REG1026A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ADCY_TOGV2	3	1=ADC Y channel interleaving every 2 VSYNC.	
	ADCY_TOGH2	2	1=ADC Y channel interleaving every 2 HSYNC.	
	CYU_NO_VRAND	1	1=no ADCB interleve V dithering.	
	CYU_NO_RAND	0	1=no ADCB interleve H/V dithering.	
52h (1026A4h)	**REG1026A4**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	CYU_INT_V_POLARITY	1	1=ADCB interleave vsync reference pulse polarity high.	
	CYU_INT_H_POLARITY	0	1=ADCB interleave hsync reference pulse polarity high.	
53h (1026A6h)	**REG1026A6**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_SELF_CAL_REF_CYC[7:0]	7:0	ADCB calibration trigger reference pulse cycle number.	
53h (1026A7h)	**REG1026A7**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	-	7:6	Reserved.	
	CYU_SELF_CAL_ALL_GAIN	5	1=ADCB calibration all gain mode enable.	
	CYU_SELF_CAL_MODE[1:0]	4:3	[0]=1: ADCB linear calibration enable. [1]=1: ADCB offset/gain calibration enable.	
	CYU_SELF_CAL_STOP	2	1=ADCB calibration stop in live mode.	
	CYU_SELF_CAL_LIVE	1	1=ADCB calibration live mode enable.	
	CYU_SELF_CAL_START	0	1=ADCB calibration start.	
54h (1026A8h)	**REG1026A8**	**7:0**	**Default : 0x10**	**Access : R/W**
	CYU_SELF_CAL_DLY[7:0]	7:0	ADCB claibration delay from reference pulse to linear/offset/gain calibration state.	
54h	**REG1026A9**	**7:0**	**Default : 0x00**	**Access : R/W**

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ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1026A9h)	CYU_SELF_CAL_LIVE_WAIT_DLY[7:0]	7:0	ADCB claibration wait delay number of reference pulse before re-starting new calibration in live mode.	
55h (1026AAh)	**REG1026AA**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	CYU_SELF_CAL_GPUSE_SEL	0	1=ADCB SELF_CAL_G active high during linear calibration & gain calibration; Otherwise, ADCB SELF_CAL_G active high only during linear calibration.	
57h (1026AEh)	**REG1026AE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CYU_LINEAR_CAL_MODE	0	1=ADCB linear calibration long mode.	
57h (1026AFh)	**REG1026AF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	CYU_LINEAR_CAL_VREF_SEL[3:0]	7:4	ADCB VCAL setting during linear calibration.	
	CYU_LINEAR_CAL_PGA[3:0]	3:0	ADCB PGA setting during linear calibration.	
58h (1026B0h)	**REG1026B0**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:1	Reserved.	
	ADCY_LCAL_EN	0	1=ADC Y linear calibration update enable.	
5Bh (1026B6h)	**REG1026B6**	**7:0**	**Default : 0x1F**	**Access : R/W**
	CYU_LINEAR_CAL_DLY[7:0]	7:0	ADCB linear calibration delay samples after reference pulse rising.	
5Bh (1026B7h)	**REG1026B7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CYU_LINEAR_CAL_DLY[11:8]	3:0	See description of '1026B6h'.	
5Ch (1026B8h)	**REG1026B8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CYU_LINEAR_CAL_DUR[7:0]	7:0	ADCB linear calibration duration samples after reference pulse rising.	
5Dh (1026BAh)	**REG1026BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ADCY_OCAL_EN	1	1=ADC Y offset calibration update enable.	
	CYU_OFFSET_CAL_MODE	0	1=ADCB offset calibration long mode.	
5Eh (1026BCh)	**REG1026BC**	**7:0**	**Default : 0x1F**	**Access : R/W**
	CYU_OFFSET_CAL_DLY[7:0]	7:0	ADCB offset calibration delay samples after reference pulse rising.	
5Eh	**REG1026BD**	**7:0**	**Default : 0x00**	**Access : R/W**

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ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1026BDh)	-	7:4	Reserved.	
	CYU_OFFSET_CAL_DLY[11:8]	3:0	See description of '1026BCh'.	
5Fh	**REG1026BE**	**7:0**	**Default : 0xFF**	**Access : R/W**
(1026BEh)	CYU_OFFSET_CAL_DUR[7:0]	7:0	ADCB offset calibration duration samples after reference pulse rising.	
64h	**REG1026C8**	**7:0**	**Default : 0x04**	**Access : R/W**
(1026C8h)	-	7:3	Reserved.	
	CYU_GAIN_CAL_MISMATCH_ONLY	2	1=ADCB gain calibration only calibrate channel0/channel1 mismatch.	
	ADCY_GCAL_EN	1	1=ADC Y gain calibration update enable.	
	CYU_GAIN_CAL_MODE	0	1=ADCB gain calibration long mode.	
65h	**REG1026CA**	**7:0**	**Default : 0x1F**	**Access : R/W**
(1026CAh)	CYU_GAIN_CAL_DLY[7:0]	7:0	ADCB gain calibration delay samples after reference pulse rising.	
65h	**REG1026CB**	**7:0**	**Default : 0x00**	**Access : R/W**
(1026CBh)	-	7:4	Reserved.	
	CYU_GAIN_CAL_DLY[11:8]	3:0	See description of '1026CAh'.	
66h	**REG1026CC**	**7:0**	**Default : 0xFF**	**Access : R/W**
(1026CCh)	CYU_GAIN_CAL_DUR[7:0]	7:0	ADCB gain calibration duration samples after reference pulse rising.	
66h	**REG1026CD**	**7:0**	**Default : 0xFF**	**Access : R/W**
(1026CDh)	CYU_GAIN_CAL_DUR[15:8]	7:0	See description of '1026CCh'.	
72h	**REG1026E4**	**7:0**	**Default : 0x00**	**Access : R/W**
(1026E4h)	CYU_GAIN_CAL_LVREF[3:0]	7:4	ADCB gain calibration low VCAL write value.	
	CYU_GAIN_CAL_HVREF[3:0]	3:0	ADCB gain calibration high VCAL write value.	
72h	**REG1026E5**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
(1026E5h)	CYU_GAIN_CAL_VREF_WP	7	ADCB gain calibration VCAL write enable.	
	-	6:4	Reserved.	
	CYU_GAIN_CAL_VREF_WG[3:0]	3:0	ADCB gain calibration VCAL write related gain setting.	
73h	**REG1026E6**	**7:0**	**Default : 0x00**	**Access : R/W**
(1026E6h)	CYU_GAIN_CAL_TARGET[7:0]	7:0	ADCB gain calibration VCAL_HIGH-VCAL_LOW target digital code write value.	
73h	**REG1026E7**	**7:0**	**Default : 0x00**	**Access : R/W**
(1026E7h)	-	7:4	Reserved.	

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ADC_DTOP Register (Bank = 1026)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CYU_GAIN_CAL_TARGET[11:8]	3:0	See description of '1026E6h'.	
74h (1026E8h)	**REG1026E8**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	CYU_GAIN_CAL_TARGET_WP	7	ADCB gain calibration (VCAL_HIGH-VCAL_LOW) target digital code write enable.	
	-	6:4	Reserved.	
	CYU_GAIN_CAL_TARGET_WG[3:0]	3:0	ADCB gain calibration VCAL_HIGH-VCAL_LOW target digital code write related gain setting.	
7Bh (1026F6h)	**REG1026F6**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_REF_DLY[7:0]	7:0	The delay samples of ADCA calibration reference pulse after Hsync/Vsync.	
7Bh (1026F7h)	**REG1026F7**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_REF_SEL[2:0]	7:5	[2:0]=1xx : ADCA using VSYNC as calibration reference pulse. [2:0]=01x : ADCA using HSYNC as calibration reference pulse. [2:0]=001 : ADCA using HSOUT as calibration reference pulse. [2:0]=000 : ADCA calibration reference always high.	
	RGB_SELF_CAL_REF_EDGE	4	1=ADCA calibration reference using trailing edge of hsync/vsync.	
	RGB_SELF_CAL_REF_DLY[11:8]	3:0	See description of '1026F6h'.	
7Ch (1026F8h)	**REG1026F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_SELF_CAL_REF_DLY[7:0]	7:0	The delay samples of ADCB calibration reference pulse after Hsync/Vsync.	
7Ch (1026F9h)	**REG1026F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_SELF_CAL_REF_SEL[2:0]	7:5	[2:0]=1xx : ADCB using VSYNC as calibration reference pulse. [2:0]=01x : ADCB using HSYNC as calibration reference pulse. [2:0]=001 : ADCB using HSOUT as calibration reference pulse. [2:0]=000 : ADCB calibration reference always high.	
	CYU_SELF_CAL_REF_EDGE	4	1=ADCB calibration reference using trailing edge of hsync/vsync.	
	CYU_SELF_CAL_REF_DLY[11:8]	3:0	See description of '1026F8h'.	
7Dh ~ 7Fh	**-**	**7:0**	**Default : -**	**Access : -**

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ADC_DTOP Register (Bank = 1026)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(1026FAh ~ 1026FFh)	-	-	Reserved.

GE Register (Bank = 1028)

GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102800h)	**REG102800**	**7:0**	**Default : 0x01**	**Access : R/W**
	EN_GE_DCK	7	Enable Destination Color Key. 0: Disable. 1: Enable.	
	EN_GE_SCK	6	Enable Source Color Key. 0: Disable. 1: Enable.	
	EN_GE_ROP	5	Enable ROP2. 0: Disable (equal to setting GE_ROP2 = 4'hc). 1: Enable.	
	EN_GE_ABL_DCK	4	Enable Alpha Destination Color Key. 0: Disable. 1: Enable.	
	EN_GE_ABL_SCK	3	Enable Alpha Source Color Key. 0: Disable. 1: Enable.	
	EN_GE_ABL	2	Enable Alpha Blending. 0: Disable. 1: Enable.	
	EN_GE_DITHER	1	Enable Dither. 0: Disable. 1: Enable.	
	EN_GE	0	Enable Graphics Engine (Unqueue). 0: Disable and reset to initial state. 1: Enable.	
00h (102801h)	**REG102801**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EN_GE_DSTAC	4	Enable Destination Alpha Compare. 0: Disable. 1: Enable.	
	EN_GE_ALPHA_CMP	3	Enable Alpha Compare. 0: Disable. 1: Enable.	
	EN_GE_DFB	2	Enable DFB alpha blending function. 0: Disable. 1: Enable.	
	EN_GE_RN	1	Enable Random Noise. 0: Disable. 1: Enable.	
	EN_GE_LPT	0	Enable Line Pattern Test. 0: Disable. 1: Enable.	
01h (102802h)	**REG102802**	**7:0**	**Default : 0x01**	**Access : R/W**
	EN_GE_LENGTH_LIMIT	7	Enable MIU Length Limitation (unqueue). 0: Disable. 1: Enable.	
	EN_GE_ITC	6	Enable Italic Font. 0: Disable. 1: Enable.	
	EN_GE_CLIP_CHK	5	Enable Clipping Check. 0: Disable. 1: Enable.	
	EN_GE_STBB	4	Enable Stretch BitBlt. 0: Disable (force to Do Non Stretch BitBlt). 1: Enable (Do Stretch BitBlt if GE_STBB_DX = 1.0 or GE_STBB_DY = 1.0; Do Non Stretch BitBlt if GE_STBB_DX = 1.0 and GE_STBB_DY = 1.0).	
	-	3:2	Reserved.	
	EN_GE_VCMQ	1	Enable Virtual Command Queue (unqueue). 0: Disable. 1: Enable.	
	EN_GE_CMQ	0	Enable Command Queue (unqueue). 0: Disable. 1: Enable.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102803h)	**REG102803**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_GE_CLKGATE	7	Enable Dynamic Clock Gating (unqueue). 0: Disable. 1: Enable.	
	-	6:5	Reserved.	
	EN_GE_CLR_MIU_INVALID	4	Clear Invalid MIU Flag (unqueue). 0: Disable. 1: Enable.	
	EN_GE_MIU1_PMA	3	Enable MIU1 protection (unqueue). 0: Disable. 1: Enable.	
	EN_GE_MIU0_PMA	2	Enable MIU0 protection (unqueue). 0: Disable. 1: Enable.	
	-	1:0	Reserved.	
02h (102804h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (102805h)	**REG102805**	**7:0**	**Default : 0x3F**	**Access : R/W**
	GE_LENGTH_MODE	7	GE MIU Length Limit Mode (unqueue). 0: Fix Mode. 1: Auto Change Mode.	
	GE_LENGTH_AUTO_POL	6	Polarity of Varient Mode (unqueue).	
	GE_LENGTH_TH[5:0]	5:0	GE MIU most access count (unqueue).	
03h (102806h)	**REG102806**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_W_TH[3:0]	7:4	Virtual Command Write Queue Threshold (unqueue).	
	GE_STBB_TH[3:0]	3:0	Reading Source Threshold.	
03h (102807h)	**REG102807**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_VCMQ_R_TH[3:0]	3:0	Virtual Command Read Queue Threshold (unqueue).	
04h ~ 07h (102808h ~ 10280Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
08h	**REG102810**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102810h)	GE_MIU0_PMA_LTH[7:0]	7:0	MIU 0 Protection Memory Address Range Low Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
08h (102811h)	**REG102811**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU0_PMA_LTH[15:8]	7:0	See description of '102810h'.	
09h (102812h)	**REG102812**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU0_PMA_LTH[23:16]	7:0	See description of '102810h'.	
09h (102813h)	**REG102813**	**7:0**	**Default : 0x80**	**Access : R/W**
	GE_MIU0_PMA_MODE	7	In the miu0 protection range (unqueue). 0: The address in this range is invalid. 1: The address in this range is valid.	
	-	6:5	Reserved.	
	GE_MIU0_PMA_LTH[28:24]	4:0	See description of '102810h'.	
0Ah (102814h)	**REG102814**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU0_PMA_HTH[7:0]	7:0	MIU 0 Protection Memory Address Range High Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
0Ah (102815h)	**REG102815**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU0_PMA_HTH[15:8]	7:0	See description of '102814h'.	
0Bh (102816h)	**REG102816**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU0_PMA_HTH[23:16]	7:0	See description of '102814h'.	
0Bh (102817h)	**REG102817**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	GE_MIU0_PMA_HTH[28:24]	4:0	See description of '102814h'.	
0Ch (102818h)	**REG102818**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU1_PMA_LTH[7:0]	7:0	MIU 1 Protection Memory Address Range Low Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
0Ch (102819h)	**REG102819**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU1_PMA_LTH[15:8]	7:0	See description of '102818h'.	
0Dh (10281Ah)	**REG10281A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU1_PMA_LTH[23:16]	7:0	See description of '102818h'.	
0Dh (10281Bh)	**REG10281B**	**7:0**	**Default : 0x80**	**Access : R/W**
	GE_MIU1_PMA_MODE	7	In the miu1 protection range (unqueue). 0: The address in this range is invalid. 1: The address in this range is valid.	
	-	6:5	Reserved.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_MIU1_PMA_LTH[28:24]	4:0	See description of '102818h'.	
0Eh (10281Ch)	**REG10281C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU1_PMA_HTH[7:0]	7:0	MIU 1 Protection Memory Address Range High Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
0Eh (10281Dh)	**REG10281D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU1_PMA_HTH[15:8]	7:0	See description of '10281Ch'.	
0Fh (10281Eh)	**REG10281E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU1_PMA_HTH[23:16]	7:0	See description of '10281Ch'.	
0Fh (10281Fh)	**REG10281F**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	GE_MIU1_PMA_HTH[28:24]	4:0	See description of '10281Ch'.	
10h (102820h)	**REG102820**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	GE_ROP2[3:0]	3:0	Raster Operation ROP2.	
11h (102822h)	**REG102822**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_ABL_COEF[3:0]	3:0	Coefficient of Alpha Blending. Csrc is the source color. Cdst is the destination or background color. Asrc is the alpha value of source. Adst is the alpha value of destination. Aconst is the constant alpha value. If the dfb enable is on, the register will disable. 0: Csrc. 1: Csrc * Aconst + Cdst * (1 - Aconst). 2: Csrc * Asrc + Cdst * (1 - Asrc). 3: Csrc * Adst + Cdst * (1 - Adst). 4: ((Asrc * Aconst) * Csrc + (1-(Asrc *Aconst)) * Cdst). 5: ((Asrc * Aconst) * Csrc + Adst * Cdst * (1-(Asrc * Aconst))) / ((Asrc * Aconst) + Adst * (1- Asrc * Aconst)). 6: ((Asrc * Aconst) * Csrc * (1-Adst) + Adst * Cdst) / (Asrc * Aconst) * (1-Adst) + Adst). 7: Csrc * Aconst. 8: Cdst. 9: Csrc * (1 - Aconst) + Cdst * Aconst. a: Csrc * (1 - Asrc) + Cdst * Asrc. b: Csrc * (1 - Adst) + Cdst * Adst. c: (Csrc * Adst * Asrc * Aconst + Cdst * Adst * (1 - Asrc * Aconst)) / (Adst * Asrc * Aconst + Adst * (1 - Asrc * Aconst). d: (Cdst * Asrc * Aconst * Adst + Csrc * Asrc * Aconst * (1 - Adst)) / (Asrc * Aconst * (1 - Adst) + Asrc * Aconst * Adst). e: ((1 - Adst) * Csrc * Asrc * Aconst + Adst * Cdst * (1 - Asrc * Aconst)) / (Asrc * Aconst * (1 - Adst) + Adst * (1 - Asrc * Aconst)). f: Csrc * (1 - Aconst). Others: Reserved.	
11h (102823h)	**REG102823**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_ABL_1555[7:0]	7:0	Alpha value of ARGB1555.	
12h (102825h)	**REG102825**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_DB_ABL[3:0]	3:0	Alpha value of writing to Destination after Alpha Color Key. If the dfb is enable, this register will disable. 0: Aconst (DFB). 1: Asrc. 2: Adst. 3: Asrc * Aconst. 4: Asrc * Aconst * Adst. 5: Adst * (1 - Asrc * Aconst). 6: Asrc * Aconst * (1 - Adst). 7: Asrc * Aconst * (1 - Adst) + Adst. 8: 1 - Aconst (DFB). 9: 1 - Asrc. a: 1 - Adst. b: Adst * Asrc * Aconst + Adst * (1 - Asrc * Aconst) A atop B. c: Asrc * Aconst * Adst + Asrc * Aconst * (1 - Adst) B atop A. d: (1 - Adst) * Asrc * Aconst + Adst * (1 - Asrc * Aconst) A xor B. e: Asrc * Asrc * Aconst + Adst * (1 - Asrc * Aconst). f: Asrc * (1 - Asrc * Aconst) + Adst * Asrc * Aconst. Others: Reserved.	
13h (102826h)	**REG102826**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ABL_CONST[7:0]	7:0	Constant Alpha Register for Alpha Blending.	
14h (102828h)	**REG102828**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[7:0]	7:0	Source Color Key High Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
14h (102829h)	**REG102829**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[15:8]	7:0	See description of '102828h'.	
15h (10282Ah)	**REG10282A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[23:16]	7:0	See description of '102828h'.	
15h (10282Bh)	**REG10282B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[31:24]	7:0	See description of '102828h'.	
16h	**REG10282C**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10282Ch)	GE_SCK_LTH[7:0]	7:0	Source Color Key Low Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
16h (10282Dh)	**REG10282D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[15:8]	7:0	See description of '10282Ch'.	
17h (10282Eh)	**REG10282E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[23:16]	7:0	See description of '10282Ch'.	
17h (10282Fh)	**REG10282F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[31:24]	7:0	See description of '10282Ch'.	
18h (102830h)	**REG102830**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[7:0]	7:0	Destination Color Key High Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
18h (102831h)	**REG102831**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[15:8]	7:0	See description of '102830h'.	
19h (102832h)	**REG102832**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[23:16]	7:0	See description of '102830h'.	
19h (102833h)	**REG102833**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[31:24]	7:0	See description of '102830h'.	
1Ah (102834h)	**REG102834**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[7:0]	7:0	Destination Color Key Low Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
1Ah (102835h)	**REG102835**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[15:8]	7:0	See description of '102834h'.	
1Bh (102836h)	**REG102836**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[23:16]	7:0	See description of '102834h'.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Bh (102837h)	**REG102837**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[31:24]	7:0	See description of '102834h'.	
1Ch (102838h)	**REG102838**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_DSTAC_MODE	5	Destination Alpha Compare Mode. 0: If the destination alpha is in the threshold, and GE won't do the alpha operation. 1: If the destination isn't in the Threshold, GE won't do the alpha operation.	
	GE_ALPHA_CMP_MODE	4	Alpha Compare Mode. 0: Maximum Alpha of Source and Destination. 1: Minimum Alpha of Source and Destination.	
	GE_ABL_DCK_OP_MODE	3	Destination Alpha Key Operation Mode. 0: If the color is not equal to the destination color key, the color will be replaced by the source color. 1: If the color is equal to the source color key, the color will be replaced by the source color.	
	GE_ABL_SCK_OP_MODE	2	Source Alpha Key Operation Mode. 0: If the color is equal to the source color key, the color will be replaced by the destination color. 1: If the color is not equal to the source color key, the color will be replaced by the destination color.	
	GE_DCK_OP_MODE	1	Destination Color Key Operation Mode. 0: If the color is not equal to the destination color key, the color will be replaced by the source color. 1: If the color is equal to the destination color key, the color will be replaced by the source color.	
	GE_SCK_OP_MODE	0	Source Color Key Operation Mode. 0: If the color is equal to the source color key, the color will be replaced by the destination color. 1: If the color is not equal to the source color key, the color will be replaced by the destination color.	
1Dh (10283Ah)	**REG10283A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTAC_HTH[7:0]	7:0	Destination Alpha Compare Value High Threshold.	
1Dh (10283Bh)	**REG10283B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTAC_LTH[7:0]	7:0	Destination Alpha Comparison Value Low Threshold.	
1Eh	**REG10283C**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10283Ch)	GE_IRQ_MASK[1:0]	7:6	Interrupt Mask.	
	-	5:0	Reserved.	
1Eh (10283Dh)	**REG10283D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	IRQ_RAW_STATUS[1:0]	7:6	Status of Interrupt on IP Side.	
	IRQ_FINAL_STATUS[1:0]	5:4	Status of Interrupt on CPU Side.	
	GE_IRQ_CLR[1:0]	3:2	Interrupt Clear.	
	GE_IRQ_FORCE[1:0]	1:0	Force Interrupt Enable.	
1Fh (10283Eh)	**REG10283E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_YUV_FM[1:0]	7:6	YUV destination 422 format. 0: CbY1CrY0. 1: CrY1CbY0. 2: Y1CbY0Cr. 3: Y1CrY0Cb.	
	GE_SB_YUV_FM[1:0]	5:4	YUV source 422 format. 0: CbY1CrY0. 1: CrY1CbY0. 2: Y1CbY0Cr. 3: Y1CrY0Cb.	
	GE_YUV_IN	3	UV input range. 0: 0~255. 1: -128~127.	
	GE_YUV_RANGE	2	YUV output range. 0: 0~255. 1: Y: 16~235, UV: 16~240.	
	GE_YUV_FILTER	1	UV 1 1 filter. 0: Disable. 1: Enable.	
	GE_DC_CSC_FM	0	Color Space Conversion Format for Decode (RGB to YUV). 0: Computer Mode (Y: 16~235, UV: 0~240). 1: CSC to 0~255. Others: Reserved.	
1Fh (10283Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h	**REG102840**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102840h)	GE_SB_BASE[7:0]	7:0	Base Address of Graphics Engine Source Buffer (unit = byte). The start of Source Buffer storage must be pixel aligned.	
20h (102841h)	**REG102841**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_BASE[15:8]	7:0	See description of '102840h'.	
21h (102842h)	**REG102842**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_BASE[23:16]	7:0	See description of '102840h'.	
21h (102843h)	**REG102843**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_MIU_SEL	7	Source Buffer MIU selection. 0: MIU0. 1: MIU1.	
	-	6:5	Reserved.	
	GE_SB_BASE[28:24]	4:0	See description of '102840h'.	
26h (10284Ch)	**REG10284C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[7:0]	7:0	Base Address of Graphics Engine Destination Buffer (unit = byte). The Destination Buffer storage must be pixel aligned.	
26h (10284Dh)	**REG10284D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[15:8]	7:0	See description of '10284Ch'.	
27h (10284Eh)	**REG10284E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[23:16]	7:0	See description of '10284Ch'.	
27h (10284Fh)	**REG10284F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_MIU_SEL	7	Destination Buffer MIU selection. 0: MIU0. 1: MIU1.	
	-	6:5	Reserved.	
	GE_DB_BASE[28:24]	4:0	See description of '10284Ch'.	
28h (102850h)	**REG102850**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_BASE[7:0]	7:0	Base Address of Virtual Command Queue (unqueue). The Unit of Base is Byte. The Destination Buffer storage must be 64bit alignment. [2:0] will be ignored.	
28h (102851h)	**REG102851**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_BASE[15:8]	7:0	See description of '102850h'.	
29h	**REG102852**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102852h)	GE_VCMQ_BASE[23:16]	7:0	See description of '102850h'.	
29h (102853h)	**REG102853**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_MIU_SEL	7	Virtual Command Queue MIU selection (unqueue). 0: MIU0. 1: MIU1.	
	-	6:5	Reserved.	
	GE_VCMQ_BASE[28:24]	4:0	See description of '102850h'.	
2Ah (102854h)	**REG102854**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_VCMQ_SIZE[2:0]	2:0	Size of Virtual Command Queue (unqueue). 0: 8k. 1: 16k. 2: 32k. 3: 64k. 4: 128k. 5: 256k. 6: 512k. 7: 1024k.	
2Ah (102855h)	**REG102855**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTBLEND[3:0]	7:4	Destination Blend. 0: ZERO [Adst * 0, Cdst * 0]. 1: ONE [Adst * 1, Cdst * 1]. 2: SRCCOLOR [Adst * Asrc, Cdst * Csrc]. 3: INVSRCCOLOR [Adst * (1 - Asrc), Cdst * (1 - Csrc)]. 4: SRCALPHA [Adst * Asrc, Cdst * Asrc]. 5: INVSRCALPHA [Adst * (1 - Asrc), Cdst * (1- Asrc)]. 6: DESTALPHA [Adst * Adst, Cdst * Adst]. 7: INVDESTALPHA [Adst * (1 - Adst), Cdst * (1 - Adst)]. 8: DESTCOLOR [Adst * Adst, Cdst * Cdst]. 9: INVDESTCOLOR [Adst * (1 - Adst), Cdst * (1 - Cdst)]. 10: SRCALPHASAT [Adst * 1, Cdst * min(Asrc, (1 - Adst))].	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_SRCBLEND[3:0]	3:0	Source Blend. 0: ZERO [Asrc * 0, Csrc * 0]. 1: ONE [Asrc * 1, Csrc * 1]. 2: SRCCOLOR [Asrc * Asrc, Csrc * Csrc]. 3: INVSRCCOLOR [Asrc * (1 - Asrc), Csrc * (1 - Csrc)]. 4: SRCALPHA [Asrc * Asrc, Csrc * Asrc]. 5: INVSRCALPHA [Asrc * (1 - Asrc), Csrc * (1- Asrc)]. 6: DESTALPHA [Asrc * Adst, Csrc * Adst]. 7: INVDESTALPHA [Asrc * (1 - Adst), Csrc * (1 - Adst)]. 8: DESTCOLOR [Asrc * Adst, Csrc * Cdst]. 9: INVDESTCOLOR [Asrc * (1 - Adst), Csrc * (1 - Cdst)]. 10: SRCALPHASAT [Asrc * 1, Csrc * min(Asrc, (1 - Adst))].	
2Bh (102856h)	**REG102856**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DEMUL	7	Csrc is the source color. Cdst is the destination color. 0: [Asrc, Csrc]. 1: [Asrc / Asrc, Csrc / Asrc].	
	GE_XOR	6	Asrc is the source alpha. Adst is the destination alpha. Csrc is the source color. Cdst is the destination color. 0: [Adst, Cdst]. 1: [Asrc^Adst, Csrc^Cdst].	
	GE_DST_PREMUL	5	Csrc is the source color. Adst is the alpha value of destination. 0: Cdst. 1: Cdst * Adst.	
	GE_SRC_PRECOL	4	Csrc is the source color. Aconst is the constant alpha value. 0: Csrc. 1: Csrc * Aconst.	
	GE_SRC_PREMUL	3	Asrc is the alpha value of source. Csrc is the source color. 0: Csrc. 1: Csrc * Asrc.	
	GE_COLORIZE	2	Csrc is the source color. Cconst is the constant color value. 0: Csrc. 1: Csrc * Cconst.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_ALPHACH	1	Asrc is the alpha value of source. Aconst is the constant alpha value. Asmask is the source mask alpha. If coloralpha and source mask are all disable, this register is nouse. 0: Aconst. 1: Asrc * Aconst or Asrc * Asmask.	
	GE_COLORALPHA	0	Asrc is the alpha value of source. Aconst is the constant alpha value. 0: Asrc. 1: Asrc * Aconst (alphach enable) or Aconst (alphach disable).	
2Bh (102857h)	**REG102857**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_B_CONST[7:0]	7:0	Constant blue.	
2Ch (102858h)	**REG102858**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_G_CONST[7:0]	7:0	Constant green.	
2Ch (102859h)	**REG102859**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_R_CONST[7:0]	7:0	Constant red.	
2Dh (10285Ah)	**REG10285A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_B[7:0]	7:0	256 Pallette Table Blue.	
2Dh (10285Bh)	**REG10285B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_G[7:0]	7:0	256 Pallette Table Green.	
2Eh (10285Ch)	**REG10285C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_R[7:0]	7:0	256 Pallette Table Red.	
2Eh (10285Dh)	**REG10285D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_A[7:0]	7:0	256 Pallette Table Alpha.	
2Fh (10285Eh)	**REG10285E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_INDEX[7:0]	7:0	Index of 256 Pallette Table.	
2Fh (10285Fh)	**REG10285F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GE_P256_RW	0	256 Pallette Table read/write.	
30h (102860h)	**REG102860**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_PIT[7:0]	7:0	Pitch of Graphics Engine Source Buffer (unit = byte). In I1, I2, and I4 modes: the pitch must be 8-bit aligned. In other modes: the pitch must be 32-bit aligned.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102861h)	**REG102861**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_SB_PIT[13:8]	5:0	See description of '102860h'.	
31h (102862h)	**REG102862**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[7:0]	7:0	Tag Register.	
31h (102863h)	**REG102863**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[15:8]	7:0	See description of '102862h'.	
32h (102864h)	**REG102864**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[23:16]	7:0	See description of '102862h'.	
32h (102865h)	**REG102865**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[31:24]	7:0	See description of '102862h'.	
33h (102866h)	**REG102866**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_PIT[7:0]	7:0	Pitch of Graphics Engine Destination Buffer (unit = byte). The pitch must be 32-bit aligned.	
33h (102867h)	**REG102867**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_DB_PIT[13:8]	5:0	See description of '102866h'.	
34h (102868h)	**REG102868**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_SB_FM[4:0]	4:0	Format of Graphics Engine Source Buffer. 0: 1 bit, Intensity 1. 1: 2 bits, Intensity 2. 2: 4 bits, Intensity 4. 4: 8 bits, Palette 8. 5: RGB332[7:0]. 6: 16 bits, FaBaFgBg2266[15:0]. 7: 16 bits, 1ABFgBg12355[15:0]. 8: 16 bits, RGB565[15:0]. 9: 16 bits, ARGB1555[15:0]. a: 16 bits, ARGB4444[15:0]. e: 16 bits, YUYV422[15:0]. f: 32 bits, ARGB8888[31:0]. 10: RGBA5551[15:0]. 11: RGBA4444[15:0]. 1f: ABGR8888[31:0]. Others: Reserved.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
34h (102869h)	**REG102869**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_DB_FM[4:0]	4:0	Format of Graphics Engine Destination Buffer. 4: 8 bits, Palette 8. 5: RGB332. 6: 16 bits, FaBaFgBg2266[15:0]. 7: 16 bits, 1ABFgBg12355[15:0]. 8: 16 bits, RGB565[15:0]. 9: 16 bits, 0RGB1555[15:0]. a: 16 bits, ARGB4444[15:0]. c: 16 bits, ARGB1555[15:0]. e: 16 bits, YUYV422[15:0]. f: ARGB8888[31:0]. 10: RGBA5551[15:0]. 11: RGBA4444[15:0]. 1f: ABGR8888[31:0]. Others: Reserved.	
35h (10286Ah)	**REG10286A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[7:0]	7:0	Intensity 0 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
35h (10286Bh)	**REG10286B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[15:8]	7:0	See description of '10286Ah'.	
36h (10286Ch)	**REG10286C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[23:16]	7:0	See description of '10286Ah'.	
36h (10286Dh)	**REG10286D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[31:24]	7:0	See description of '10286Ah'.	
37h	**REG10286E**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10286Eh)	GE_I1_C[7:0]	7:0	Intensity 1 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
37h (10286Fh)	**REG10286F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[15:8]	7:0	See description of '10286Eh'.	
38h (102870h)	**REG102870**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[23:16]	7:0	See description of '10286Eh'.	
38h (102871h)	**REG102871**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[31:24]	7:0	See description of '10286Eh'.	
39h (102872h)	**REG102872**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[7:0]	7:0	Intensity 2 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
39h (102873h)	**REG102873**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[15:8]	7:0	See description of '102872h'.	
3Ah (102874h)	**REG102874**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[23:16]	7:0	See description of '102872h'.	
3Ah (102875h)	**REG102875**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[31:24]	7:0	See description of '102872h'.	
3Bh (102876h)	**REG102876**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[7:0]	7:0	Intensity 3 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
3Bh	**REG102877**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102877h)	GE_I3_C[15:8]	7:0	See description of '102876h'.	
3Ch (102878h)	**REG102878**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[23:16]	7:0	See description of '102876h'.	
3Ch (102879h)	**REG102879**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[31:24]	7:0	See description of '102876h'.	
3Dh (10287Ah)	**REG10287A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[7:0]	7:0	Intensity 4 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
3Dh (10287Bh)	**REG10287B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[15:8]	7:0	See description of '10287Ah'.	
3Eh (10287Ch)	**REG10287C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[23:16]	7:0	See description of '10287Ah'.	
3Eh (10287Dh)	**REG10287D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[31:24]	7:0	See description of '10287Ah'.	
3Fh (10287Eh)	**REG10287E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[7:0]	7:0	Intensity 5 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
3Fh (10287Fh)	**REG10287F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[15:8]	7:0	See description of '10287Eh'.	
40h (102880h)	**REG102880**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[23:16]	7:0	See description of '10287Eh'.	
40h (102881h)	**REG102881**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[31:24]	7:0	See description of '10287Eh'.	
41h	**REG102882**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102882h)	GE_I6_C[7:0]	7:0	Intensity 6 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
41h (102883h)	**REG102883**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[15:8]	7:0	See description of '102882h'.	
42h (102884h)	**REG102884**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[23:16]	7:0	See description of '102882h'.	
42h (102885h)	**REG102885**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[31:24]	7:0	See description of '102882h'.	
43h (102886h)	**REG102886**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[7:0]	7:0	Intensity 7 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
43h (102887h)	**REG102887**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[15:8]	7:0	See description of '102886h'.	
44h (102888h)	**REG102888**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[23:16]	7:0	See description of '102886h'.	
44h (102889h)	**REG102889**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[31:24]	7:0	See description of '102886h'.	
45h (10288Ah)	**REG10288A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[7:0]	7:0	Intensity 8 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
45h	**REG10288B**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10288Bh)	GE_I8_C[15:8]	7:0	See description of '10288Ah'.	
46h (10288Ch)	**REG10288C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[23:16]	7:0	See description of '10288Ah'.	
46h (10288Dh)	**REG10288D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[31:24]	7:0	See description of '10288Ah'.	
47h (10288Eh)	**REG10288E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[7:0]	7:0	Intensity 9 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
47h (10288Fh)	**REG10288F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[15:8]	7:0	See description of '10288Eh'.	
48h (102890h)	**REG102890**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[23:16]	7:0	See description of '10288Eh'.	
48h (102891h)	**REG102891**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[31:24]	7:0	See description of '10288Eh'.	
49h (102892h)	**REG102892**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[7:0]	7:0	Intensity 10 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
49h (102893h)	**REG102893**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[15:8]	7:0	See description of '102892h'.	
4Ah (102894h)	**REG102894**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[23:16]	7:0	See description of '102892h'.	
4Ah (102895h)	**REG102895**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[31:24]	7:0	See description of '102892h'.	
4Bh	**REG102896**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102896h)	GE_I11_C[7:0]	7:0	Intensity 11 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
4Bh (102897h)	**REG102897**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[15:8]	7:0	See description of '102896h'.	
4Ch (102898h)	**REG102898**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[23:16]	7:0	See description of '102896h'.	
4Ch (102899h)	**REG102899**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[31:24]	7:0	See description of '102896h'.	
4Dh (10289Ah)	**REG10289A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[7:0]	7:0	Intensity 12 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
4Dh (10289Bh)	**REG10289B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[15:8]	7:0	See description of '10289Ah'.	
4Eh (10289Ch)	**REG10289C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[23:16]	7:0	See description of '10289Ah'.	
4Eh (10289Dh)	**REG10289D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[31:24]	7:0	See description of '10289Ah'.	
4Fh (10289Eh)	**REG10289E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[7:0]	7:0	Intensity 13 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
4Fh	**REG10289F**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10289Fh)	GE_I13_C[15:8]	7:0	See description of '10289Eh'.	
50h (1028A0h)	**REG1028A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[23:16]	7:0	See description of '10289Eh'.	
50h (1028A1h)	**REG1028A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[31:24]	7:0	See description of '10289Eh'.	
51h (1028A2h)	**REG1028A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[7:0]	7:0	Intensity 14 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
51h (1028A3h)	**REG1028A3**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[15:8]	7:0	See description of '1028A2h'.	
52h (1028A4h)	**REG1028A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[23:16]	7:0	See description of '1028A2h'.	
52h (1028A5h)	**REG1028A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[31:24]	7:0	See description of '1028A2h'.	
53h (1028A6h)	**REG1028A6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[7:0]	7:0	Intensity 15 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
53h (1028A7h)	**REG1028A7**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[15:8]	7:0	See description of '1028A6h'.	
54h (1028A8h)	**REG1028A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[23:16]	7:0	See description of '1028A6h'.	
54h (1028A9h)	**REG1028A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[31:24]	7:0	See description of '1028A6h'.	
55h (1028AAh)	**REG1028AA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_CLIP_LEFT[7:0]	7:0	2D Clipping Window Left Setting (11).	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (1028ABh)	**REG1028AB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_LEFT[11:8]	3:0	See description of '1028AAh'.	
56h (1028ACh)	**REG1028AC**	**7:0**	**Default : 0xD0**	**Access : R/W**
	GE_CLIP_RIGHT[7:0]	7:0	2D Clipping Window Right Setting (11).	
56h (1028ADh)	**REG1028AD**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_RIGHT[11:8]	3:0	See description of '1028ACh'.	
57h (1028AEh)	**REG1028AE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_CLIP_TOP[7:0]	7:0	2D Clipping Window Top Setting (11).	
57h (1028AFh)	**REG1028AF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_TOP[11:8]	3:0	See description of '1028AEh'.	
58h (1028B0h)	**REG1028B0**	**7:0**	**Default : 0x40**	**Access : R/W**
	GE_CLIP_BOT[7:0]	7:0	2D Clipping Window Bottom Setting (11).	
58h (1028B1h)	**REG1028B1**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_BOT[11:8]	3:0	See description of '1028B0h'.	
59h (1028B2h)	**REG1028B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_TYPE[1:0]	7:6	Strech Bitblt with Color Key Type. 0: Do nothing. 1: Nearest When the Color Key happened. 2: Replace the Key to Custom Color. 3: Reserved.	
	-	5:2	Reserved.	
	GE_ROT[1:0]	1:0	Coordinate Rotation Degree (Clockwise). 0: 0. 1: 90. 2: 180. 3: 270.	
5Ch (1028B8h)	**REG1028B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_B[7:0]	7:0	Stretch Bitblt Replace Blue.	
5Ch (1028B9h)	**REG1028B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_G[7:0]	7:0	Stretch Bitblt Replace Green.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Dh (1028BAh)	**REG1028BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_R[7:0]	7:0	Stretch Bitblt Replace Blue.	
5Dh (1028BBh)	**REG1028BB**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_A[7:0]	7:0	Stretch Bitblt Replace Alpha.	
5Eh (1028BCh)	**REG1028BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_INI_DX[7:0]	7:0	Initial Delta X for Stretch BitBlt (s.12).	
5Eh (1028BDh)	**REG1028BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_INI_DX[12:8]	4:0	See description of '1028BCh'.	
5Fh (1028BEh)	**REG1028BE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_INI_DY[7:0]	7:0	Initial Delta Y for Stretch BitBlt (s.12).	
5Fh (1028BFh)	**REG1028BF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_INI_DY[12:8]	4:0	See description of '1028BEh'.	
60h (1028C0h)	**REG1028C0**	**7:0**	**Default : 0x40**	**Access : R/W**
	GE_PRI_S_X_DIR	7	For Rectangle Fill and BitBlt: Primitive Drawing Direction in X Coordinates for Source. If the source direction is not equal to the destination direction, it means X mirror. 0: Positive Direction: From Left to Right. 1: Negative Direction: From Right to Left.	
	GE_PRIM_TYPE[2:0]	6:4	Primitive Type of 2D Graphics. A write to this register will cause an engine fire. 1: Line. 3: Rectangle Fill. 4: BitBlt. 7: Freeze. Others: Reserved.	
	-	3:0	Reserved.	
60h (1028C1h)	**REG1028C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_PATCH	7	Stretch BitBlt Patch Pixel Type. 0: Add zeros. 1: Duplicate last pixel or first pixel.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_STBB_TYPE	6	Stretch BitBlt Type. 0: Bilinear Mode. 1: Nearest Mode (8-bit palette and 16-bit index must use this mode).	
	GE_RECT_CV	5	Rectangle Fill Vertical Color Type. 0: Constant Color Fill. 1: Gradient Color Fill.	
	GE_RECT_CH	4	Rectangle Fill Horizontal Color Type. 0: Constant Color Fill. 1: Gradient Color Fill.	
	GE_LINE_C_TYPE	3	Color Type Setting for Line Drawing. 0: Constant Color Line Draw. 1: Gradient Color Line Draw.	
	GE_PRI_Y_DIR	2	For Rectangle Fill and BitBlt: Primitive Drawing Direction in Y Coordinates for Destination. 0: Positive Direction: From Top to Bottom. 1: Negative Direction: From Top to Bottom.	
	GE_PRI_X_DIR	1	For Rectangle Fill and BitBlt: Primitive Drawing Direction in X Coordinates for Destination. For Line Drawing: Primitive Drawing Direction in Major Coordinates defined in GE_LINE_MAJOR. 0: Positive Direction: From Left to Right. 1: Negative Direction: From Right to Left.	
	GE_PRI_S_Y_DIR	0	For Rectangle Fill and BitBlt: Primitive Drawing Direction in Y Coordinates for Destination. 0: Positive Direction: From Top to Bottom. 1: Negative Direction: From Bottom to Top.	
61h (1028C2h)	**REG1028C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_LINE_DELTA[6:0]	7:1	Delta value of minor direction for Line Drawing. X delta value for BitBlt (s1.12).	
	-	0	Reserved.	
61h	**REG1028C3**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1028C3h)	GE_LINE_MAJOR	7	Major Direction Setting for Line Drawing. 0: X is the major direction. 1: Y is the major direction.	
	GE_LINE_DELTA[13:7]	6:0	See description of '1028C2h'.	
62h (1028C4h)	**REG1028C4**	**7:0**	**Default : 0x3F**	**Access : R/W**
	GE_LPT_RPF[1:0]	7:6	Line Pattern Repeat Factor. 00: Repeat Factor = 1. 01: Repeat Factor = 2. 10: Repeat Factor = 3. 11: Repeat Factor = 4.	
	GE_LPT[5:0]	5:0	Line Pattern. [5:0] Line Pattern. LSB will be used first.	
62h (1028C5h)	**REG1028C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GE_LINE_LAST	1	Line Last Pixel Control. 0: Do not draw the last pixel of line. 1: Draw the last pixel of line.	
	GE_LPT_RST	0	Line Pattern Reset Control. Writing 1 to this bit will cause a Line Pattern Reset. After the reset, HW will automatically set this bit back to 0. 0: Do not reset Line Pattern for Line Drawing. 1: Reset Line Pattern for Line Drawing.	
63h (1028C6h)	**REG1028C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_LINE_LENGTH[7:0]	7:0	Line Length.	
63h (1028C7h)	**REG1028C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_LINE_LENGTH[11:8]	3:0	See description of '1028C6h'.	
64h (1028C8h)	**REG1028C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_DX[7:0]	7:0	Delta X for Stretch BitBlt (1.12).	
64h (1028C9h)	**REG1028C9**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_DX[12:8]	4:0	See description of '1028C8h'.	
65h (1028CAh)	**REG1028CA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_DY[7:0]	7:0	Delta Y for Stretch BitBlt (1.12).	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
65h (1028CBh)	**REG1028CB**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_DY[12:8]	4:0	See description of '1028CAh'.	
66h (1028CCh)	**REG1028CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ITC_DIS[7:0]	7:0	Initial distance of the italic font.	
66h (1028CDh)	**REG1028CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ITC_LINE[7:0]	7:0	Initial line of the italic font.	
67h (1028CEh)	**REG1028CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_ITC_DELTA[4:0]	4:0	Delta value of Italic BitBlt (s1.3).	
68h (1028D0h)	**REG1028D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V0_X[7:0]	7:0	X0, Coordinate X of Primitive Vertex 0. (unit: pixel limit:4079).	
68h (1028D1h)	**REG1028D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V0_X[11:8]	3:0	See description of '1028D0h'.	
69h (1028D2h)	**REG1028D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V0_Y[7:0]	7:0	Y0, Coordinate Y of Primitive Vertex 0. (unit: pixel limit:4095).	
69h (1028D3h)	**REG1028D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V0_Y[11:8]	3:0	See description of '1028D2h'.	
6Ah (1028D4h)	**REG1028D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V1_X[7:0]	7:0	X1, Coordinate X of Primitive Vertex 1. (unit: pixel limit: 4079).	
6Ah (1028D5h)	**REG1028D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V1_X[11:8]	3:0	See description of '1028D4h'.	
6Bh (1028D6h)	**REG1028D6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V1_Y[7:0]	7:0	Y1, Coordinate Y of Primitive Vertex 1. (unit:pixel limit: 4095).	
6Bh (1028D7h)	**REG1028D7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V1_Y[11:8]	3:0	See description of '1028D6h'.	

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Ch (1028D8h)	**REG1028D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V2_X[7:0]	7:0	X2, Coordinate X of Primitive Vertex 2. (unit:pixel limit 4079).	
6Ch (1028D9h)	**REG1028D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V2_X[11:8]	3:0	See description of '1028D8h'.	
6Dh (1028DAh)	**REG1028DA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V2_Y[7:0]	7:0	Y2, Coordinate Y of Primitive Vertex 2. (unit:pixel limit: 4095).	
6Dh (1028DBh)	**REG1028DB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V2_Y[11:8]	3:0	See description of '1028DAh'.	
6Eh (1028DCh)	**REG1028DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_S_W[7:0]	7:0	BitBlt Source Width (limit: 4080).	
6Eh (1028DDh)	**REG1028DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_STBB_S_W[11:8]	3:0	See description of '1028DCh'.	
6Fh (1028DEh)	**REG1028DE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_S_H[7:0]	7:0	BitBlt Source Height (limit: 4080).	
6Fh (1028DFh)	**REG1028DF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_STBB_S_H[11:8]	3:0	See description of '1028DEh'.	
70h (1028E0h)	**REG1028E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_ST[7:0]	7:0	Bst, Start Value of Primitive B Color. 1BAAFgBg123433 FgBg. 1ABFgBg12355 Bg. Palette 8.	
70h (1028E1h)	**REG1028E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_ST[7:0]	7:0	Gst, Start Value of Primitive G Color. 1BAAFgBg123433 A. 1ABFgBg12355 Fg.	
71h	**REG1028E2**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1028E2h)	GE_PRI_R_ST[7:0]	7:0	Rst, Start Value of Primitive R Color. 1BAAFgBg123433 BA. 1ABFgBg12355 AB.	
71h (1028E3h)	**REG1028E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_ST[7:0]	7:0	Ast, Start Value of Primitive Alpha Factor. 1BAAFgBg123433 1. 1ABFgBg12355 1.	
72h (1028E4h)	**REG1028E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DX[7:0]	7:0	Rdx, Primitive Parameter delta R in X direction for Rectangle Fill. Primitive Parameter delta R for Line Draw (s7.12).	
72h (1028E5h)	**REG1028E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DX[15:8]	7:0	See description of '1028E4h'.	
73h (1028E6h)	**REG1028E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_R_DX[19:16]	3:0	See description of '1028E4h'.	
74h (1028E8h)	**REG1028E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DY[7:0]	7:0	Rdy, Primitive Parameter delta R in Y direction for Rectangle Draw (s7.12).	
74h (1028E9h)	**REG1028E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DY[15:8]	7:0	See description of '1028E8h'.	
75h (1028EAh)	**REG1028EA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_R_DY[19:16]	3:0	See description of '1028E8h'.	
76h (1028ECh)	**REG1028EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DX[7:0]	7:0	Gdx, Primitive Parameter delta G in X direction for Rectangle Fill. Primitive Parameter delta G for Line Draw (s7.12).	
76h (1028EDh)	**REG1028ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DX[15:8]	7:0	See description of '1028ECh'.	
77h (1028EEh)	**REG1028EE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_G_DX[19:16]	3:0	See description of '1028ECh'.	
78h	**REG1028F0**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1028F0h)	GE_PRI_G_DY[7:0]	7:0	Gdy, Primitive Parameter delta G in Y direction for Rectangle Fill (s7.12).	
78h (1028F1h)	**REG1028F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DY[15:8]	7:0	See description of '1028F0h'.	
79h (1028F2h)	**REG1028F2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_G_DY[19:16]	3:0	See description of '1028F0h'.	
7Ah (1028F4h)	**REG1028F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DX[7:0]	7:0	Bdx, Primitive Parameter delta B in X direction for Rectangle Fill. Primitive Parameter delta B for Line Draw (s7.12).	
7Ah (1028F5h)	**REG1028F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DX[15:8]	7:0	See description of '1028F4h'.	
7Bh (1028F6h)	**REG1028F6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_B_DX[19:16]	3:0	See description of '1028F4h'.	
7Ch (1028F8h)	**REG1028F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DY[7:0]	7:0	Bdy, Primitive Parameter delta B in Y direction for Rectangle Fill (s7.12).	
7Ch (1028F9h)	**REG1028F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DY[15:8]	7:0	See description of '1028F8h'.	
7Dh (1028FAh)	**REG1028FA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_B_DY[19:16]	3:0	See description of '1028F8h'.	
7Eh (1028FCh)	**REG1028FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DX[7:0]	7:0	Adx, Primitive Parameter delta A in X direction for Rectangle Fill. Primitive Parameter delta A for Line Draw (s4.11).	
7Eh (1028FDh)	**REG1028FD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DX[15:8]	7:0	See description of '1028FCh'.	
7Fh (1028FEh)	**REG1028FE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DY[7:0]	7:0	Ady, Primitive Parameter delta A in Y direction for Rectangle Fill (s4.11).	
7Fh	**REG1028FF**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE Register (Bank = 1028)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(1028FFh)	GE_PRI_A_DY[15:8]	7:0	See description of '1028FEh'.

CHIPGPIO Register (Bank = 102B)

CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102B00h)	**REG102B00**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_BT_IN00	2	GPIO_BT_IN00.	
	GPIO_BT_OEN00	1	GPIO_BT_OEN00.	
	GPIO_BT_OUT00	0	GPIO_BT_OUT00.	
00h (102B01h)	**REG102B01**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_BT_IN01	2	GPIO_BT_IN01.	
	GPIO_BT_OEN01	1	GPIO_BT_OEN01.	
	GPIO_BT_OUT01	0	GPIO_BT_OUT01.	
01h (102B02h)	**REG102B02**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_BT_IN02	2	GPIO_BT_IN02.	
	GPIO_BT_OEN02	1	GPIO_BT_OEN02.	
	GPIO_BT_OUT02	0	GPIO_BT_OUT02.	
01h (102B03h)	**REG102B03**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_BT_IN03	2	GPIO_BT_IN03.	
	GPIO_BT_OEN03	1	GPIO_BT_OEN03.	
	GPIO_BT_OUT03	0	GPIO_BT_OUT03.	
02h (102B04h)	**REG102B04**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_BT_IN04	2	GPIO_BT_IN04.	
	GPIO_BT_OEN04	1	GPIO_BT_OEN04.	
	GPIO_BT_OUT04	0	GPIO_BT_OUT04.	
02h	**REG102B05**	**7:0**	**Default : 0x02**	**Access : RO, R/W**

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102B05h)	-	7:3	Reserved.	
	GPIO_BT_IN05	2	GPIO_BT_IN05.	
	GPIO_BT_OEN05	1	GPIO_BT_OEN05.	
	GPIO_BT_OUT05	0	GPIO_BT_OUT05.	
03h (102B06h)	**REG102B06**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_BT_IN06	2	GPIO_BT_IN06.	
	GPIO_BT_OEN06	1	GPIO_BT_OEN06.	
	GPIO_BT_OUT06	0	GPIO_BT_OUT06.	
03h (102B07h)	**REG102B07**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_BT_IN07	2	GPIO_BT_IN07.	
	GPIO_BT_OEN07	1	GPIO_BT_OEN07.	
	GPIO_BT_OUT07	0	GPIO_BT_OUT07.	
04h (102B09h)	**REG102B09**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN00	2	GPIO_G_IN00.	
	GPIO_G_OEN00	1	GPIO_G_OEN00.	
	GPIO_G_OUT00	0	GPIO_G_OUT00.	
05h (102B0Ah)	**REG102B0A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN01	2	GPIO_G_IN01.	
	GPIO_G_OEN01	1	GPIO_G_OEN01.	
	GPIO_G_OUT01	0	GPIO_G_OUT01.	
05h (102B0Bh)	**REG102B0B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN02	2	GPIO_G_IN02.	
	GPIO_G_OEN02	1	GPIO_G_OEN02.	
	GPIO_G_OUT02	0	GPIO_G_OUT02.	
06h (102B0Ch)	**REG102B0C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN03	2	GPIO_G_IN03.	
	GPIO_G_OEN03	1	GPIO_G_OEN03.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_G_OUT03	0	GPIO_G_OUT03.	
06h (102B0Dh)	**REG102B0D**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN04	2	GPIO_G_IN04.	
	GPIO_G_OEN04	1	GPIO_G_OEN04.	
	GPIO_G_OUT04	0	GPIO_G_OUT04.	
07h (102B0Eh)	**REG102B0E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN05	2	GPIO_G_IN05.	
	GPIO_G_OEN05	1	GPIO_G_OEN05.	
	GPIO_G_OUT05	0	GPIO_G_OUT05.	
07h (102B0Fh)	**REG102B0F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN06	2	GPIO_G_IN06.	
	GPIO_G_OEN06	1	GPIO_G_OEN06.	
	GPIO_G_OUT06	0	GPIO_G_OUT06.	
08h (102B10h)	**REG102B10**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN07	2	GPIO_G_IN07.	
	GPIO_G_OEN07	1	GPIO_G_OEN07.	
	GPIO_G_OUT07	0	GPIO_G_OUT07.	
08h (102B11h)	**REG102B11**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN08	2	GPIO_G_IN08.	
	GPIO_G_OEN08	1	GPIO_G_OEN08.	
	GPIO_G_OUT08	0	GPIO_G_OUT08.	
09h (102B12h)	**REG102B12**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN09	2	GPIO_G_IN09.	
	GPIO_G_OEN09	1	GPIO_G_OEN09.	
	GPIO_G_OUT09	0	GPIO_G_OUT09.	
09h (102B13h)	**REG102B13**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_G_IN10	2	GPIO_G_IN10.	
	GPIO_G_OEN10	1	GPIO_G_OEN10.	
	GPIO_G_OUT10	0	GPIO_G_OUT10.	
0Ah (102B14h)	**REG102B14**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN11	2	GPIO_G_IN11.	
	GPIO_G_OEN11	1	GPIO_G_OEN11.	
	GPIO_G_OUT11	0	GPIO_G_OUT11.	
0Ah (102B15h)	**REG102B15**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN12	2	GPIO_G_IN12.	
	GPIO_G_OEN12	1	GPIO_G_OEN12.	
	GPIO_G_OUT12	0	GPIO_G_OUT12.	
0Bh (102B16h)	**REG102B16**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN13	2	GPIO_G_IN13.	
	GPIO_G_OEN13	1	GPIO_G_OEN13.	
	GPIO_G_OUT13	0	GPIO_G_OUT13.	
0Bh (102B17h)	**REG102B17**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN14	2	GPIO_G_IN14.	
	GPIO_G_OEN14	1	GPIO_G_OEN14.	
	GPIO_G_OUT14	0	GPIO_G_OUT14.	
0Ch (102B18h)	**REG102B18**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN15	2	GPIO_G_IN15.	
	GPIO_G_OEN15	1	GPIO_G_OEN15.	
	GPIO_G_OUT15	0	GPIO_G_OUT15.	
0Ch (102B19h)	**REG102B19**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN16	2	GPIO_G_IN16.	
	GPIO_G_OEN16	1	GPIO_G_OEN16.	
	GPIO_G_OUT16	0	GPIO_G_OUT16.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Dh (102B1Ah)	**REG102B1A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN17	2	GPIO_G_IN17.	
	GPIO_G_OEN17	1	GPIO_G_OEN17.	
	GPIO_G_OUT17	0	GPIO_G_OUT17.	
0Dh (102B1Bh)	**REG102B1B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN18	2	GPIO_G_IN18.	
	GPIO_G_OEN18	1	GPIO_G_OEN18.	
	GPIO_G_OUT18	0	GPIO_G_OUT18.	
0Eh (102B1Ch)	**REG102B1C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN19	2	GPIO_G_IN19.	
	GPIO_G_OEN19	1	GPIO_G_OEN19.	
	GPIO_G_OUT19	0	GPIO_G_OUT19.	
0Eh (102B1Dh)	**REG102B1D**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN20	2	GPIO_G_IN20.	
	GPIO_G_OEN20	1	GPIO_G_OEN20.	
	GPIO_G_OUT20	0	GPIO_G_OUT20.	
0Fh (102B1Eh)	**REG102B1E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN21	2	GPIO_G_IN21.	
	GPIO_G_OEN21	1	GPIO_G_OEN21.	
	GPIO_G_OUT21	0	GPIO_G_OUT21.	
0Fh (102B1Fh)	**REG102B1F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN22	2	GPIO_G_IN22.	
	GPIO_G_OEN22	1	GPIO_G_OEN22.	
	GPIO_G_OUT22	0	GPIO_G_OUT22.	
10h (102B20h)	**REG102B20**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN23	2	GPIO_G_IN23.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_G_OEN23	1	GPIO_G_OEN23.	
	GPIO_G_OUT23	0	GPIO_G_OUT23.	
10h (102B21h)	**REG102B21**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN24	2	GPIO_G_IN24.	
	GPIO_G_OEN24	1	GPIO_G_OEN24.	
	GPIO_G_OUT24	0	GPIO_G_OUT24.	
11h (102B22h)	**REG102B22**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN25	2	GPIO_G_IN25.	
	GPIO_G_OEN25	1	GPIO_G_OEN25.	
	GPIO_G_OUT25	0	GPIO_G_OUT25.	
11h (102B23h)	**REG102B23**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN26	2	GPIO_G_IN26.	
	GPIO_G_OEN26	1	GPIO_G_OEN26.	
	GPIO_G_OUT26	0	GPIO_G_OUT26.	
12h (102B24h)	**REG102B24**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN27	2	GPIO_G_IN27.	
	GPIO_G_OEN27	1	GPIO_G_OEN27.	
	GPIO_G_OUT27	0	GPIO_G_OUT27.	
12h (102B25h)	**REG102B25**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN28	2	GPIO_G_IN28.	
	GPIO_G_OEN28	1	GPIO_G_OEN28.	
	GPIO_G_OUT28	0	GPIO_G_OUT28.	
13h (102B26h)	**REG102B26**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN29	2	GPIO_G_IN29.	
	GPIO_G_OEN29	1	GPIO_G_OEN29.	
	GPIO_G_OUT29	0	GPIO_G_OUT29.	
13h	**REG102B27**	**7:0**	**Default : 0x02**	**Access : RO, R/W**

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102B27h)	-	7:3	Reserved.	
	GPIO_G_IN30	2	GPIO_G_IN30.	
	GPIO_G_OEN30	1	GPIO_G_OEN30.	
	GPIO_G_OUT30	0	GPIO_G_OUT30.	
14h (102B28h)	**REG102B28**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN31	2	GPIO_G_IN31.	
	GPIO_G_OEN31	1	GPIO_G_OEN31.	
	GPIO_G_OUT31	0	GPIO_G_OUT31.	
14h (102B29h)	**REG102B29**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN32	2	GPIO_G_IN32.	
	GPIO_G_OEN32	1	GPIO_G_OEN32.	
	GPIO_G_OUT32	0	GPIO_G_OUT32.	
15h (102B2Ah)	**REG102B2A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN33	2	GPIO_G_IN33.	
	GPIO_G_OEN33	1	GPIO_G_OEN33.	
	GPIO_G_OUT33	0	GPIO_G_OUT33.	
15h (102B2Bh)	**REG102B2B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN34	2	GPIO_G_IN34.	
	GPIO_G_OEN34	1	GPIO_G_OEN34.	
	GPIO_G_OUT34	0	GPIO_G_OUT34.	
16h (102B2Ch)	**REG102B2C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN35	2	GPIO_G_IN35.	
	GPIO_G_OEN35	1	GPIO_G_OEN35.	
	GPIO_G_OUT35	0	GPIO_G_OUT35.	
16h (102B2Dh)	**REG102B2D**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN36	2	GPIO_G_IN36.	
	GPIO_G_OEN36	1	GPIO_G_OEN36.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_G_OUT36	0	GPIO_G_OUT36.	
17h (102B2Eh)	**REG102B2E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN37	2	GPIO_G_IN37.	
	GPIO_G_OEN37	1	GPIO_G_OEN37.	
	GPIO_G_OUT37	0	GPIO_G_OUT37.	
17h (102B2Fh)	**REG102B2F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_G_IN38	2	GPIO_G_IN38.	
	GPIO_G_OEN38	1	GPIO_G_OEN38.	
	GPIO_G_OUT38	0	GPIO_G_OUT38.	
18h (102B31h)	**REG102B31**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN00	2	GPIO_GPS_IN00.	
	GPIO_GPS_OEN00	1	GPIO_GPS_OEN00.	
	GPIO_GPS_OUT00	0	GPIO_GPS_OUT00.	
19h (102B32h)	**REG102B32**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN01	2	GPIO_GPS_IN01.	
	GPIO_GPS_OEN01	1	GPIO_GPS_OEN01.	
	GPIO_GPS_OUT01	0	GPIO_GPS_OUT01.	
19h (102B33h)	**REG102B33**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN02	2	GPIO_GPS_IN02.	
	GPIO_GPS_OEN02	1	GPIO_GPS_OEN02.	
	GPIO_GPS_OUT02	0	GPIO_GPS_OUT02.	
1Ah (102B34h)	**REG102B34**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN03	2	GPIO_GPS_IN03.	
	GPIO_GPS_OEN03	1	GPIO_GPS_OEN03.	
	GPIO_GPS_OUT03	0	GPIO_GPS_OUT03.	
1Ah (102B35h)	**REG102B35**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_GPS_IN04	2	GPIO_GPS_IN04.	
	GPIO_GPS_OEN04	1	GPIO_GPS_OEN04.	
	GPIO_GPS_OUT04	0	GPIO_GPS_OUT04.	
1Bh (102B36h)	**REG102B36**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN05	2	GPIO_GPS_IN05.	
	GPIO_GPS_OEN05	1	GPIO_GPS_OEN05.	
	GPIO_GPS_OUT05	0	GPIO_GPS_OUT05.	
1Bh (102B37h)	**REG102B37**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN06	2	GPIO_GPS_IN06.	
	GPIO_GPS_OEN06	1	GPIO_GPS_OEN06.	
	GPIO_GPS_OUT06	0	GPIO_GPS_OUT06.	
1Ch (102B38h)	**REG102B38**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN07	2	GPIO_GPS_IN07.	
	GPIO_GPS_OEN07	1	GPIO_GPS_OEN07.	
	GPIO_GPS_OUT07	0	GPIO_GPS_OUT07.	
1Ch (102B39h)	**REG102B39**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_GPS_IN08	2	GPIO_GPS_IN08.	
	GPIO_GPS_OEN08	1	GPIO_GPS_OEN08.	
	GPIO_GPS_OUT08	0	GPIO_GPS_OUT08.	
1Dh (102B3Bh)	**REG102B3B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_I2CM_IN00	2	GPIO_I2CM_IN00.	
	GPIO_I2CM_OEN00	1	GPIO_I2CM_OEN00.	
	GPIO_I2CM_OUT00	0	GPIO_I2CM_OUT00.	
1Eh (102B3Ch)	**REG102B3C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_I2CM_IN01	2	GPIO_I2CM_IN01.	
	GPIO_I2CM_OEN01	1	GPIO_I2CM_OEN01.	
	GPIO_I2CM_OUT01	0	GPIO_I2CM_OUT01.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Fh (102B3Eh)	**REG102B3E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN00	2	GPIO_TTL_IN00.	
	GPIO_TTL_OEN00	1	GPIO_TTL_OEN00.	
	GPIO_TTL_OUT00	0	GPIO_TTL_OUT00.	
1Fh (102B3Fh)	**REG102B3F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN01	2	GPIO_TTL_IN01.	
	GPIO_TTL_OEN01	1	GPIO_TTL_OEN01.	
	GPIO_TTL_OUT01	0	GPIO_TTL_OUT01.	
20h (102B40h)	**REG102B40**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN02	2	GPIO_TTL_IN02.	
	GPIO_TTL_OEN02	1	GPIO_TTL_OEN02.	
	GPIO_TTL_OUT02	0	GPIO_TTL_OUT02.	
20h (102B41h)	**REG102B41**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN03	2	GPIO_TTL_IN03.	
	GPIO_TTL_OEN03	1	GPIO_TTL_OEN03.	
	GPIO_TTL_OUT03	0	GPIO_TTL_OUT03.	
21h (102B42h)	**REG102B42**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN04	2	GPIO_TTL_IN04.	
	GPIO_TTL_OEN04	1	GPIO_TTL_OEN04.	
	GPIO_TTL_OUT04	0	GPIO_TTL_OUT04.	
21h (102B43h)	**REG102B43**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN05	2	GPIO_TTL_IN05.	
	GPIO_TTL_OEN05	1	GPIO_TTL_OEN05.	
	GPIO_TTL_OUT05	0	GPIO_TTL_OUT05.	
22h (102B44h)	**REG102B44**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN06	2	GPIO_TTL_IN06.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_TTL_OEN06	1	GPIO_TTL_OEN06.	
	GPIO_TTL_OUT06	0	GPIO_TTL_OUT06.	
22h (102B45h)	**REG102B45**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN07	2	GPIO_TTL_IN07.	
	GPIO_TTL_OEN07	1	GPIO_TTL_OEN07.	
	GPIO_TTL_OUT07	0	GPIO_TTL_OUT07.	
23h (102B46h)	**REG102B46**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN08	2	GPIO_TTL_IN08.	
	GPIO_TTL_OEN08	1	GPIO_TTL_OEN08.	
	GPIO_TTL_OUT08	0	GPIO_TTL_OUT08.	
23h (102B47h)	**REG102B47**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN09	2	GPIO_TTL_IN09.	
	GPIO_TTL_OEN09	1	GPIO_TTL_OEN09.	
	GPIO_TTL_OUT09	0	GPIO_TTL_OUT09.	
24h (102B48h)	**REG102B48**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN10	2	GPIO_TTL_IN10.	
	GPIO_TTL_OEN10	1	GPIO_TTL_OEN10.	
	GPIO_TTL_OUT10	0	GPIO_TTL_OUT10.	
24h (102B49h)	**REG102B49**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TTL_IN11	2	GPIO_TTL_IN11.	
	GPIO_TTL_OEN11	1	GPIO_TTL_OEN11.	
	GPIO_TTL_OUT11	0	GPIO_TTL_OUT11.	
28h (102B50h)	**REG102B50**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_IIS_IN00	2	GPIO_IIS_IN00.	
	GPIO_IIS_OEN00	1	GPIO_IIS_OEN00.	
	GPIO_IIS_OUT00	0	GPIO_IIS_OUT00.	
28h	**REG102B51**	**7:0**	**Default : 0x02**	**Access : RO, R/W**

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102B51h)	-	7:3	Reserved.	
	GPIO_IIS_IN01	2	GPIO_IIS_IN01.	
	GPIO_IIS_OEN01	1	GPIO_IIS_OEN01.	
	GPIO_IIS_OUT01	0	GPIO_IIS_OUT01.	
29h (102B52h)	**REG102B52**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_IIS_IN02	2	GPIO_IIS_IN02.	
	GPIO_IIS_OEN02	1	GPIO_IIS_OEN02.	
	GPIO_IIS_OUT02	0	GPIO_IIS_OUT02.	
29h (102B53h)	**REG102B53**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_IIS_IN03	2	GPIO_IIS_IN03.	
	GPIO_IIS_OEN03	1	GPIO_IIS_OEN03.	
	GPIO_IIS_OUT03	0	GPIO_IIS_OUT03.	
2Ch (102B58h)	**REG102B58**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN00	2	GPIO_MPIF_IN00.	
	GPIO_MPIF_OEN00	1	GPIO_MPIF_OEN00.	
	GPIO_MPIF_OUT00	0	GPIO_MPIF_OUT00.	
2Ch (102B59h)	**REG102B59**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN01	2	GPIO_MPIF_IN01.	
	GPIO_MPIF_OEN01	1	GPIO_MPIF_OEN01.	
	GPIO_MPIF_OUT01	0	GPIO_MPIF_OUT01.	
2Dh (102B5Ah)	**REG102B5A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN02	2	GPIO_MPIF_IN02.	
	GPIO_MPIF_OEN02	1	GPIO_MPIF_OEN02.	
	GPIO_MPIF_OUT02	0	GPIO_MPIF_OUT02.	
2Dh (102B5Bh)	**REG102B5B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN03	2	GPIO_MPIF_IN03.	
	GPIO_MPIF_OEN03	1	GPIO_MPIF_OEN03.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_MPIF_OUT03	0	GPIO_MPIF_OUT03.	
2Eh (102B5Ch)	**REG102B5C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN04	2	GPIO_MPIF_IN04.	
	GPIO_MPIF_OEN04	1	GPIO_MPIF_OEN04.	
	GPIO_MPIF_OUT04	0	GPIO_MPIF_OUT04.	
2Eh (102B5Dh)	**REG102B5D**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN05	2	GPIO_MPIF_IN05.	
	GPIO_MPIF_OEN05	1	GPIO_MPIF_OEN05.	
	GPIO_MPIF_OUT05	0	GPIO_MPIF_OUT05.	
2Fh (102B5Eh)	**REG102B5E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN06	2	GPIO_MPIF_IN06.	
	GPIO_MPIF_OEN06	1	GPIO_MPIF_OEN06.	
	GPIO_MPIF_OUT06	0	GPIO_MPIF_OUT06.	
2Fh (102B5Fh)	**REG102B5F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_MPIF_IN07	2	GPIO_MPIF_IN07.	
	GPIO_MPIF_OEN07	1	GPIO_MPIF_OEN07.	
	GPIO_MPIF_OUT07	0	GPIO_MPIF_OUT07.	
31h (102B62h)	**REG102B62**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN00	2	GPIO_NF_IN00.	
	GPIO_NF_OEN00	1	GPIO_NF_OEN00.	
	GPIO_NF_OUT00	0	GPIO_NF_OUT00.	
31h (102B63h)	**REG102B63**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN01	2	GPIO_NF_IN01.	
	GPIO_NF_OEN01	1	GPIO_NF_OEN01.	
	GPIO_NF_OUT01	0	GPIO_NF_OUT01.	
32h (102B64h)	**REG102B64**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_NF_IN02	2	GPIO_NF_IN02.	
	GPIO_NF_OEN02	1	GPIO_NF_OEN02.	
	GPIO_NF_OUT02	0	GPIO_NF_OUT02.	
32h (102B65h)	**REG102B65**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN03	2	GPIO_NF_IN03.	
	GPIO_NF_OEN03	1	GPIO_NF_OEN03.	
	GPIO_NF_OUT03	0	GPIO_NF_OUT03.	
33h (102B66h)	**REG102B66**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN04	2	GPIO_NF_IN04.	
	GPIO_NF_OEN04	1	GPIO_NF_OEN04.	
	GPIO_NF_OUT04	0	GPIO_NF_OUT04.	
33h (102B67h)	**REG102B67**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN05	2	GPIO_NF_IN05.	
	GPIO_NF_OEN05	1	GPIO_NF_OEN05.	
	GPIO_NF_OUT05	0	GPIO_NF_OUT05.	
34h (102B68h)	**REG102B68**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN06	2	GPIO_NF_IN06.	
	GPIO_NF_OEN06	1	GPIO_NF_OEN06.	
	GPIO_NF_OUT06	0	GPIO_NF_OUT06.	
34h (102B69h)	**REG102B69**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN07	2	GPIO_NF_IN07.	
	GPIO_NF_OEN07	1	GPIO_NF_OEN07.	
	GPIO_NF_OUT07	0	GPIO_NF_OUT07.	
35h (102B6Ah)	**REG102B6A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN08	2	GPIO_NF_IN08.	
	GPIO_NF_OEN08	1	GPIO_NF_OEN08.	
	GPIO_NF_OUT08	0	GPIO_NF_OUT08.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
35h (102B6Bh)	**REG102B6B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN09	2	GPIO_NF_IN09.	
	GPIO_NF_OEN09	1	GPIO_NF_OEN09.	
	GPIO_NF_OUT09	0	GPIO_NF_OUT09.	
36h (102B6Ch)	**REG102B6C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN10	2	GPIO_NF_IN10.	
	GPIO_NF_OEN10	1	GPIO_NF_OEN10.	
	GPIO_NF_OUT10	0	GPIO_NF_OUT10.	
36h (102B6Dh)	**REG102B6D**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN11	2	GPIO_NF_IN11.	
	GPIO_NF_OEN11	1	GPIO_NF_OEN11.	
	GPIO_NF_OUT11	0	GPIO_NF_OUT11.	
37h (102B6Eh)	**REG102B6E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN12	2	GPIO_NF_IN12.	
	GPIO_NF_OEN12	1	GPIO_NF_OEN12.	
	GPIO_NF_OUT12	0	GPIO_NF_OUT12.	
37h (102B6Fh)	**REG102B6F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN13	2	GPIO_NF_IN13.	
	GPIO_NF_OEN13	1	GPIO_NF_OEN13.	
	GPIO_NF_OUT13	0	GPIO_NF_OUT13.	
38h (102B70h)	**REG102B70**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN14	2	GPIO_NF_IN14.	
	GPIO_NF_OEN14	1	GPIO_NF_OEN14.	
	GPIO_NF_OUT14	0	GPIO_NF_OUT14.	
38h (102B71h)	**REG102B71**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN15	2	GPIO_NF_IN15.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_NF_OEN15	1	GPIO_NF_OEN15.	
	GPIO_NF_OUT15	0	GPIO_NF_OUT15.	
39h (102B72h)	**REG102B72**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN16	2	GPIO_NF_IN16.	
	GPIO_NF_OEN16	1	GPIO_NF_OEN16.	
	GPIO_NF_OUT16	0	GPIO_NF_OUT16.	
39h (102B73h)	**REG102B73**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN17	2	GPIO_NF_IN17.	
	GPIO_NF_OEN17	1	GPIO_NF_OEN17.	
	GPIO_NF_OUT17	0	GPIO_NF_OUT17.	
3Ah (102B74h)	**REG102B74**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_NF_IN18	2	GPIO_NF_IN18.	
	GPIO_NF_OEN18	1	GPIO_NF_OEN18.	
	GPIO_NF_OUT18	0	GPIO_NF_OUT18.	
3Ch (102B79h)	**REG102B79**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN00	2	GPIO_SD_IN00.	
	GPIO_SD_OEN00	1	GPIO_SD_OEN00.	
	GPIO_SD_OUT00	0	GPIO_SD_OUT00.	
3Dh (102B7Ah)	**REG102B7A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN01	2	GPIO_SD_IN01.	
	GPIO_SD_OEN01	1	GPIO_SD_OEN01.	
	GPIO_SD_OUT01	0	GPIO_SD_OUT01.	
3Dh (102B7Bh)	**REG102B7B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN02	2	GPIO_SD_IN02.	
	GPIO_SD_OEN02	1	GPIO_SD_OEN02.	
	GPIO_SD_OUT02	0	GPIO_SD_OUT02.	
3Eh	**REG102B7C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102B7Ch)	-	7:3	Reserved.	
	GPIO_SD_IN03	2	GPIO_SD_IN03.	
	GPIO_SD_OEN03	1	GPIO_SD_OEN03.	
	GPIO_SD_OUT03	0	GPIO_SD_OUT03.	
3Eh (102B7Dh)	**REG102B7D**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN04	2	GPIO_SD_IN04.	
	GPIO_SD_OEN04	1	GPIO_SD_OEN04.	
	GPIO_SD_OUT04	0	GPIO_SD_OUT04.	
3Fh (102B7Eh)	**REG102B7E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN05	2	GPIO_SD_IN05.	
	GPIO_SD_OEN05	1	GPIO_SD_OEN05.	
	GPIO_SD_OUT05	0	GPIO_SD_OUT05.	
3Fh (102B7Fh)	**REG102B7F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN06	2	GPIO_SD_IN06.	
	GPIO_SD_OEN06	1	GPIO_SD_OEN06.	
	GPIO_SD_OUT06	0	GPIO_SD_OUT06.	
40h (102B80h)	**REG102B80**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN07	2	GPIO_SD_IN07.	
	GPIO_SD_OEN07	1	GPIO_SD_OEN07.	
	GPIO_SD_OUT07	0	GPIO_SD_OUT07.	
40h (102B81h)	**REG102B81**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN08	2	GPIO_SD_IN08.	
	GPIO_SD_OEN08	1	GPIO_SD_OEN08.	
	GPIO_SD_OUT08	0	GPIO_SD_OUT08.	
41h (102B82h)	**REG102B82**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN09	2	GPIO_SD_IN09.	
	GPIO_SD_OEN09	1	GPIO_SD_OEN09.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_SD_OUT09	0	GPIO_SD_OUT09.	
41h (102B83h)	**REG102B83**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN10	2	GPIO_SD_IN10.	
	GPIO_SD_OEN10	1	GPIO_SD_OEN10.	
	GPIO_SD_OUT10	0	GPIO_SD_OUT10.	
42h (102B84h)	**REG102B84**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN11	2	GPIO_SD_IN11.	
	GPIO_SD_OEN11	1	GPIO_SD_OEN11.	
	GPIO_SD_OUT11	0	GPIO_SD_OUT11.	
42h (102B85h)	**REG102B85**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN12	2	GPIO_SD_IN12.	
	GPIO_SD_OEN12	1	GPIO_SD_OEN12.	
	GPIO_SD_OUT12	0	GPIO_SD_OUT12.	
43h (102B86h)	**REG102B86**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN13	2	GPIO_SD_IN13.	
	GPIO_SD_OEN13	1	GPIO_SD_OEN13.	
	GPIO_SD_OUT13	0	GPIO_SD_OUT13.	
43h (102B87h)	**REG102B87**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN14	2	GPIO_SD_IN14.	
	GPIO_SD_OEN14	1	GPIO_SD_OEN14.	
	GPIO_SD_OUT14	0	GPIO_SD_OUT14.	
44h (102B88h)	**REG102B88**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN15	2	GPIO_SD_IN15.	
	GPIO_SD_OEN15	1	GPIO_SD_OEN15.	
	GPIO_SD_OUT15	0	GPIO_SD_OUT15.	
44h (102B89h)	**REG102B89**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_SD_IN16	2	GPIO_SD_IN16.	
	GPIO_SD_OEN16	1	GPIO_SD_OEN16.	
	GPIO_SD_OUT16	0	GPIO_SD_OUT16.	
45h (102B8Ah)	**REG102B8A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SD_IN17	2	GPIO_SD_IN17.	
	GPIO_SD_OEN17	1	GPIO_SD_OEN17.	
	GPIO_SD_OUT17	0	GPIO_SD_OUT17.	
4Ah (102B94h)	**REG102B94**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SPDIFO_IN	2	GPIO_SPDIFO_IN.	
	GPIO_SPDIFO_OEN	1	GPIO_SPDIFO_OEN.	
	GPIO_SPDIFO_OUT	0	GPIO_SPDIFO_OUT.	
4Bh (102B96h)	**REG102B96**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN01	2	GPIO_SR_IN01.	
	GPIO_SR_OEN01	1	GPIO_SR_OEN01.	
	GPIO_SR_OUT01	0	GPIO_SR_OUT01.	
4Bh (102B97h)	**REG102B97**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN00	2	GPIO_SR_IN00.	
	GPIO_SR_OEN00	1	GPIO_SR_OEN00.	
	GPIO_SR_OUT00	0	GPIO_SR_OUT00.	
4Ch (102B98h)	**REG102B98**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN03	2	GPIO_SR_IN03.	
	GPIO_SR_OEN03	1	GPIO_SR_OEN03.	
	GPIO_SR_OUT03	0	GPIO_SR_OUT03.	
4Ch (102B99h)	**REG102B99**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN02	2	GPIO_SR_IN02.	
	GPIO_SR_OEN02	1	GPIO_SR_OEN02.	
	GPIO_SR_OUT02	0	GPIO_SR_OUT02.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Dh (102B9Ah)	**REG102B9A**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN05	2	GPIO_SR_IN05.	
	GPIO_SR_OEN05	1	GPIO_SR_OEN05.	
	GPIO_SR_OUT05	0	GPIO_SR_OUT05.	
4Dh (102B9Bh)	**REG102B9B**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN04	2	GPIO_SR_IN04.	
	GPIO_SR_OEN04	1	GPIO_SR_OEN04.	
	GPIO_SR_OUT04	0	GPIO_SR_OUT04.	
4Eh (102B9Ch)	**REG102B9C**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN07	2	GPIO_SR_IN07.	
	GPIO_SR_OEN07	1	GPIO_SR_OEN07.	
	GPIO_SR_OUT07	0	GPIO_SR_OUT07.	
4Eh (102B9Dh)	**REG102B9D**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN06	2	GPIO_SR_IN06.	
	GPIO_SR_OEN06	1	GPIO_SR_OEN06.	
	GPIO_SR_OUT06	0	GPIO_SR_OUT06.	
4Fh (102B9Eh)	**REG102B9E**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN09	2	GPIO_SR_IN09.	
	GPIO_SR_OEN09	1	GPIO_SR_OEN09.	
	GPIO_SR_OUT09	0	GPIO_SR_OUT09.	
4Fh (102B9Fh)	**REG102B9F**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN08	2	GPIO_SR_IN08.	
	GPIO_SR_OEN08	1	GPIO_SR_OEN08.	
	GPIO_SR_OUT08	0	GPIO_SR_OUT08.	
50h (102BA0h)	**REG102BA0**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN10	2	GPIO_SR_IN10.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_SR_OEN10	1	GPIO_SR_OEN10.	
	GPIO_SR_OUT10	0	GPIO_SR_OUT10.	
50h (102BA1h)	**REG102BA1**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN11	2	GPIO_SR_IN11.	
	GPIO_SR_OEN11	1	GPIO_SR_OEN11.	
	GPIO_SR_OUT11	0	GPIO_SR_OUT11.	
51h (102BA2h)	**REG102BA2**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN12	2	GPIO_SR_IN12.	
	GPIO_SR_OEN12	1	GPIO_SR_OEN12.	
	GPIO_SR_OUT12	0	GPIO_SR_OUT12.	
51h (102BA3h)	**REG102BA3**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_SR_IN13	2	GPIO_SR_IN13.	
	GPIO_SR_OEN13	1	GPIO_SR_OEN13.	
	GPIO_SR_OUT13	0	GPIO_SR_OUT13.	
53h (102BA6h)	**REG102BA6**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN00	2	GPIO_TCON_IN00.	
	GPIO_TCON_OEN00	1	GPIO_TCON_OEN00.	
	GPIO_TCON_OUT00	0	GPIO_TCON_OUT00.	
53h (102BA7h)	**REG102BA7**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN01	2	GPIO_TCON_IN01.	
	GPIO_TCON_OEN01	1	GPIO_TCON_OEN01.	
	GPIO_TCON_OUT01	0	GPIO_TCON_OUT01.	
54h (102BA8h)	**REG102BA8**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN02	2	GPIO_TCON_IN02.	
	GPIO_TCON_OEN02	1	GPIO_TCON_OEN02.	
	GPIO_TCON_OUT02	0	GPIO_TCON_OUT02.	
54h	**REG102BA9**	**7:0**	**Default : 0x02**	**Access : RO, R/W**

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102BA9h)	-	7:3	Reserved.	
	GPIO_TCON_IN03	2	GPIO_TCON_IN03.	
	GPIO_TCON_OEN03	1	GPIO_TCON_OEN03.	
	GPIO_TCON_OUT03	0	GPIO_TCON_OUT03.	
55h (102BAAh)	**REG102BAA**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN04	2	GPIO_TCON_IN04.	
	GPIO_TCON_OEN04	1	GPIO_TCON_OEN04.	
	GPIO_TCON_OUT04	0	GPIO_TCON_OUT04.	
55h (102BABh)	**REG102BAB**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN05	2	GPIO_TCON_IN05.	
	GPIO_TCON_OEN05	1	GPIO_TCON_OEN05.	
	GPIO_TCON_OUT05	0	GPIO_TCON_OUT05.	
56h (102BACh)	**REG102BAC**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN06	2	GPIO_TCON_IN06.	
	GPIO_TCON_OEN06	1	GPIO_TCON_OEN06.	
	GPIO_TCON_OUT06	0	GPIO_TCON_OUT06.	
56h (102BADh)	**REG102BAD**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN07	2	GPIO_TCON_IN07.	
	GPIO_TCON_OEN07	1	GPIO_TCON_OEN07.	
	GPIO_TCON_OUT07	0	GPIO_TCON_OUT07.	
57h (102BAEh)	**REG102BAE**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_TCON_IN08	2	GPIO_TCON_IN08.	
	GPIO_TCON_OEN08	1	GPIO_TCON_OEN08.	
	GPIO_TCON_OUT08	0	GPIO_TCON_OUT08.	
58h (102BB0h)	**REG102BB0**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN00	2	GPIO_UART_IN00.	
	GPIO_UART_OEN00	1	GPIO_UART_OEN00.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_UART_OUT00	0	GPIO_UART_OUT00.	
58h (102BB1h)	**REG102BB1**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN01	2	GPIO_UART_IN01.	
	GPIO_UART_OEN01	1	GPIO_UART_OEN01.	
	GPIO_UART_OUT01	0	GPIO_UART_OUT01.	
59h (102BB2h)	**REG102BB2**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN03	2	GPIO_UART_IN03.	
	GPIO_UART_OEN03	1	GPIO_UART_OEN03.	
	GPIO_UART_OUT03	0	GPIO_UART_OUT03.	
59h (102BB3h)	**REG102BB3**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN02	2	GPIO_UART_IN02.	
	GPIO_UART_OEN02	1	GPIO_UART_OEN02.	
	GPIO_UART_OUT02	0	GPIO_UART_OUT02.	
5Ah (102BB4h)	**REG102BB4**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN05	2	GPIO_UART_IN05.	
	GPIO_UART_OEN05	1	GPIO_UART_OEN05.	
	GPIO_UART_OUT05	0	GPIO_UART_OUT05.	
5Ah (102BB5h)	**REG102BB5**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN04	2	GPIO_UART_IN04.	
	GPIO_UART_OEN04	1	GPIO_UART_OEN04.	
	GPIO_UART_OUT04	0	GPIO_UART_OUT04.	
5Bh (102BB6h)	**REG102BB6**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN07	2	GPIO_UART_IN07.	
	GPIO_UART_OEN07	1	GPIO_UART_OEN07.	
	GPIO_UART_OUT07	0	GPIO_UART_OUT07.	
5Bh (102BB7h)	**REG102BB7**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_UART_IN06	2	GPIO_UART_IN06.	
	GPIO_UART_OEN06	1	GPIO_UART_OEN06.	
	GPIO_UART_OUT06	0	GPIO_UART_OUT06.	
5Ch (102BB8h)	**REG102BB8**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN09	2	GPIO_UART_IN09.	
	GPIO_UART_OEN09	1	GPIO_UART_OEN09.	
	GPIO_UART_OUT09	0	GPIO_UART_OUT09.	
5Ch (102BB9h)	**REG102BB9**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN08	2	GPIO_UART_IN08.	
	GPIO_UART_OEN08	1	GPIO_UART_OEN08.	
	GPIO_UART_OUT08	0	GPIO_UART_OUT08.	
5Dh (102BBAh)	**REG102BBA**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN11	2	GPIO_UART_IN11.	
	GPIO_UART_OEN11	1	GPIO_UART_OEN11.	
	GPIO_UART_OUT11	0	GPIO_UART_OUT11.	
5Dh (102BBBh)	**REG102BBB**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN10	2	GPIO_UART_IN10.	
	GPIO_UART_OEN10	1	GPIO_UART_OEN10.	
	GPIO_UART_OUT10	0	GPIO_UART_OUT10.	
5Eh (102BBCh)	**REG102BBC**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN13	2	GPIO_UART_IN13.	
	GPIO_UART_OEN13	1	GPIO_UART_OEN13.	
	GPIO_UART_OUT13	0	GPIO_UART_OUT13.	
5Eh (102BBDh)	**REG102BBD**	**7:0**	**Default : 0x02**	**Access : RO, R/W**
	-	7:3	Reserved.	
	GPIO_UART_IN12	2	GPIO_UART_IN12.	
	GPIO_UART_OEN12	1	GPIO_UART_OEN12.	
	GPIO_UART_OUT12	0	GPIO_UART_OUT12.	

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CHIPGPIO Register (Bank = 102B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h ~ 67h (102BC0h ~ 102BCFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

Scalar0 (Bank = 102E)

IPMUX Register (Bank = 102E)

IPMUX Register (Bank = 102E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102E02h)	**REG102E02**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPMUX_SEL2[3:0]	7:4	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
	IPMUX_SEL1[3:0]	3:0	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
01h (102E03h)	**REG102E03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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IPMUX Register (Bank = 102E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPMUX_SEL0[3:0]	3:0	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
02h (102E04h)	**REG102E04**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPMUX_SEL2_SC1[3:0]	7:4	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
	-	3:0	Reserved.	
02h (102E05h)	**REG102E05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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IPMUX Register (Bank = 102E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPMUX_SEL0_SC1[3:0]	3:0	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
03h (102E06h)	**REG102E06**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPMUX_SEL2_SC2[3:0]	7:4	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
	IPMUX_SEL1_SC2[3:0]	3:0	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
03h (102E07h)	**REG102E07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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IPMUX Register (Bank = 102E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPMUX_SEL0_SC2[3:0]	3:0	Input source select. 0: ADC A. 2: VD. 3: MVOP (DC0). 5: Ext VD. 6: ADC B. 7: Capture SC0. 10: Capture SC1. 13: Capture SC2. 14: Sensor ICP. 15: Ext VD2. Others: Debug mode.	
71h (102EE2h)	**REG102EE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SC2CMDQ_SEL2[1:0]	7:6	Sc2cmdq[2] source select.	
	SC2CMDQ_SEL1[2:0]	5:3	Sc2cmdq[1] source select.	
	SC2CMDQ_SEL0[2:0]	2:0	Sc2cmdq[0] source select : 0: SC0 IP_F1. 1: SC0 IP_F2. 2: SC0 OP. 3: SC1 IP_F2. 4: SC1 OP. 5: SC2 IP_F1. 6: SC2 IP_F2. 7: SC2 OP.	
71h (102EE3h)	**REG102EE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SC2CMDQ_SEL4[2:0]	6:4	Sc2cmdq[4] source select.	
	SC2CMDQ_SEL3[2:0]	3:1	Sc2cmdq[3] source select.	
	SC2CMDQ_SEL2[2]	0	See description of '102EE2h'.	

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Scaler1 Register (Bank = 102F)

GOP_INT Register (Bank = 102F, Sub-bank = 00)

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102F00h)	**REG102F00**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler.	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]: SWRST1[4]: IP, include F1 and F2. SWRST1[3]: OP include OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_MCLK_ON	7	Clk_miu enable.	
	-	6:2	Reserved.	
	PDMD[1:0]	1:0	PowerDown mode: 01: IDCLK. Others: IDCLK and ODCLK.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x10**	**Access : R/W**
	GCLK_MD[7:0]	7:0	PowerDown control: [1]: Live Fclk gated enable. [4]: Fclk gated control.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.	

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	COP_EN	7	Enable cop for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO**

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F20h)	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
13h	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F27h)	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Eh)	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**

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GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F47h)	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '102F48h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0xE1**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F1Ah)	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F1Fh)	DUMMY0F_8_15[7:0]	7:0		
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. #0: Left result. #1: right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. #0: Not clear. #1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. #0: Update every frame. #1: Keep the history value.	
	JITTER	3	JITTER function Result. #0: No JITTER. #1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. #0: Update every frame. #1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. #0: Result not ready. #1: Result ready.	
	ATS_EN	0	Auto position function Enable. #0: Disable. #1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	THOLD[3:0]	7:4	Auto position Valid Data Value. #0000: Valid if data >= 0000 0000. #0001: Valid if data >= 0001 0000. #0010: Valid if data >= 0010 0000. .. #1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Positoin Force Pixel Mode. #0 : DE or Pixel decide by the Source. #1 : Force Pixel Mode.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Aoto Gain Value. (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F35h)	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ch)	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Eh)	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh	**REG102F5C**	**7:0**	**Default : 0x01**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F5Ch)	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. #0: Can gate the GOP clock. #1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. #0: Don't gate the idclk. #1: Can gate the idclk.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATS_B_SKIP	2	Auto search ignore B data.	
	ATS_G_SKIP	1	Auto search ignore G data.	
	ATS_R_SKIP	0	Auto search ignore R data.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DE_BYPASS_MODE	7	Use input DE to replace SPRange_H as output DE.	
	-	6:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F65h)	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Bh)	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Atuto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	
40h ~ 43h (102F80h ~ 102F86h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FDET_STATUS_INTLAC_DET0	0	Mode detect result 0.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	

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IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	
60h ~ 60h (102FC0h ~ 102FC1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
70h ~ 70h (102FE0h ~ 102FE1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
71h (102FE3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 02)

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	PREV_DOWN_3D	4	PREV_DOWN_3D.	
	-	3:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x08**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	
	YDELAY_EN	4	Y delay enable.	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	44TO42_DITH_EN	0	444 to 422 filter dith enable.	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FILL_BLACK_NUM[5:0]	5:0	Fill black number.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILL_BLACK_ACT	7	FILL_BLACK_ACT.	
	FILL_BLACK_CLR	6	Clear fill_black register manually.	
	-	5:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OSD_HSK_MD	5	Ip2 osd handshaking mode.	
	FORCE_OSD_HSK	4	Force ip2 to osd in handshaking mode.	
	-	3	Reserved.	
	IP2_VS_SEL	2	1: Use mvop_vs to generate vs to opvs 0:use ip1_vs to generate vs to opvs.	
	FORCE_PRE2LAST	1	1: Use vsd last valid as pre align 0: use original pre align.	
	MVOP_DIN_EN	0	1: Data is form mvop 0: form yc delay.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RANDOM_SEL[1:0]	5:4	//random mode 0:1 1:3/4 2:1/2 3:1/4 rdy.	
	ALTIVE_LINE	3	//1: use chessboard data 0:use non line altive data;	
	CHESS_EN	2	//1: use chessboard data 0:use nomo data;	
	PAT_DATA_SEL	1	//1: use patgen data 0:use input data;	
	PAT_TIMING_SEL	0	//1: use patgen timing 1:use input timing;	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0xD0**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen h total.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0xE0**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen v total.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '102F24h'.	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x40**	**Access : R/W**
	H_BLOCK[7:0]	7:0	Patgen h block.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen v block.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	V_BLOCK[9:8]	1:0	See description of '102F28h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xF2**	**Access : R/W**
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x1F**	**Access : R/W**
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x5E**	**Access : R/W**
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xF4**	**Access : R/W**
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x0C**	**Access : R/W**
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x5A**	**Access : R/W**
	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x37**	**Access : R/W**
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0xF5**	**Access : R/W**
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y0. Format: S7 of 2's complement (-15 <= Y0 <= 15).	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 127).	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x17**	**Access : R/W**
	HSD_CT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_CT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x0B**	**Access : R/W**
	HSD_CT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_CT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x29**	**Access : R/W**
	HSD_CT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C3. Format: Fix 8 (0 <= C3 <= 255).	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x01**	**Access : R/W**
	HSD_CT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C4. Format: S7 of 2's complement (-63 <= C4 <= + 63).	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x04**	**Access : R/W**
	HSD_CT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
29h	**REG102F52**	**7:0**	**Default : 0x3C**	**Access : R/W**

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F52h)	HSD_CT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C2. Format: Fix 8 (0 <= C2 <= 127).	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:0	Reserved.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IP2DIP_SEL	0	IP2 to DIP source select: 1'b0: before HSD/VSD. 1'b1: after HSD/VSD.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IP2VE_VS_SEL	2	IP to VE vsync selection. 1'b0: IP1 vsync. 1'b1: original vsync.	
	IP2VE_CAP_EN	1	IP to VE cap enable.	
	IP2VE_PATH_EN	0	IP to VE enable.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2VE_HBLANK[3:0]	7:4	IP to VE H-blanking length.	
	IP2VE_RATE[3:0]	3:0	IP to VE flow control.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIN_CTRL_EN	7	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	6	IP2 VSD input line count number setting enable.	
	-	5	Reserved.	
	VSD_IN_NUM_USR[12:8]	4:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VOUT_CTRL_EN	7	IP2 VSD output line count control enable.	
	-	6:5	Reserved.	
	VSD_OUT_NUMBER[12:8]	4:0	See description of '102F6Eh'.	
38h	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F70h)	VSD_USR_VACT_VIDEO[7:0]	7:0	VSD user mode v_active region.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_USR_VACT_VIDEO_EN	7	VSD user mode v_active region enable.	
	-	6:5	Reserved.	
	VSD_USR_VACT_VIDEO[12:8]	4:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	VSD_VACT_VIDEO_READ[7:0]	7:0	VSD user mode v_active region.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	VSD_VACT_VIDEO_READ[12:8]	4:0	See description of '102F72h'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_HSD_OUT_CNT[12:8]	4:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_VSD_OUT_CNT[12:8]	4:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PREFLT_ALPHA_EN	7	IP2 Pre-Filter alpha blending enable.	
	-	6:5	Reserved.	
	PREFLT_ALPHA[4:0]	4:0	IP2 Pre-Filter alpha blending for original and filter.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_Y_TAP0[3:0]	3:0	IP2 Pre-Filter coefficient 0 [s.3] (T8).	
48h	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F91h)	PRE_FILTER_EN	7	IP2 Pre-Filter enable.	
	FIR_DITH_EN	6	IP2 Pre-Filter dith enable.	
	-	5:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP1[6:0]	6:0	IP2 Pre-Filter coefficient 1 [s.6] (T8).	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP2[6:0]	6:0	IP2 Pre-Filter coefficient 2 [s.6] (T8).	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP3[7:0]	7:0	IP2 Pre-Filter coefficient 3 [s.7] (T8).	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP4[7:0]	7:0	IP2 Pre-Filter coefficient 4 [s.8] (T8).	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PRE_Y_TAP4[8]	0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP5[7:0]	7:0	IP2 Pre-Filter coefficient 5 [s.9] (T8).	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP5[9:8]	1:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP6[7:0]	7:0	IP2 Pre-Filter coefficient 6 [0.10] (T8).	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP6[9:8]	1:0	See description of '102F9Ch'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FLT_MODE	0	In advance mode 0:use 4 phase blending 1: use 8 phase blending.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT3_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x0D**	**Access : R/W**
	HSD_YT3_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x5C**	**Access : R/W**
	HSD_YT3_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x23**	**Access : R/W**
	HSD_YT3_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT3_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x03**	**Access : R/W**
	HSD_YT3_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_YT4_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x3B**	**Access : R/W**
	HSD_YT4_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT4_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_YT4_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GOP_REQ_CNT[4:0]	4:0	In mvop handshake mode, gen gop needs timing.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2GOP_SRC_SEL	7	For GOPD src of ip2 0: IP2IN 1:IP2OUT.	
	-	6:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable bpseudo blanking.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x08**	**Access : R/W**
	LB_SPLIT_BLANK[7:0]	7:0	LB pseudo blank cycle.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x18**	**Access : R/W**
	PRE_ADJ_SPLIT_BLANK[7:0]	7:0	Adj pseudo blank cycle.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EXT_LR_EN	4	Enable external lr signal.	
	-	3:1	Reserved.	
	INIT_3D_STAT	0	Initialize 3d stat.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	WAIT_LEFT_FRM_INV	5	Reg_wait_right_frm.	
	WAIT_LEFT_FRM	4	WAIT_LEFT_FRM.	
	-	3:1	Reserved.	
	EXT_LR_INV	0	Inverse external lr signal.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	INI_LR_IDX	4	0: L is the first frame 1: R is the first frame.	
	-	3	Reserved.	
	ADJ_FORCE_EN	2	Adj bypass enable.	
	LR_CHG_MODE[1:0]	1:0	0: Line 1:block 2:frame.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAX_LOOP[2:0]	6:4	3d mode setting.	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:1	Reserved.	
	SPLIT_HALF	0	Split 1 frame into 2 frame.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VACT_SPC_EN[1:0]	5:4	3d mode setting.	
	-	3	Reserved.	
	MASK_EN[2:0]	2:0	3d mode setting.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GEN_VS_ACT[3:0]	7:4	Enable gen pseudo vsync in 3d.	
	GEN_VS_EN[3:0]	3:0	Enable gen pseudo vsync in 3d.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_VIDEO[7:0]	7:0	V_active region.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_VIDEO[12:8]	4:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_0[7:0]	7:0	V blanking between field1&field2 or field3&field4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_0[12:8]	4:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_1[7:0]	7:0	V blanking between field2&field3.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_1[12:8]	4:0	See description of '102FCEh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0xC0**	**Access : R/W**
	LB_AUTO	7	LB_AUTO.	
	VSD_FAC_AUTO_RST_EN	6	VSD 3d auto factor reset mode enable.	
	AUTO_VACT_VIDEO_RST	5	AUTO vact_video mode reset.	
	-	4:0	Reserved.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable dat_adj to src force ready.	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADJ_AUTO	0	ADJ_AUTO.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[7:0]	7:0	Debug.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_DIFF[7:0]	7:0	Number of fifo.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LR_ALT_LINE	2	LR_ALT_LINE.	
	LR_FST_PIX	1	LR_FST_PIX.	
	PIX_SEP_EN	0	PIX_SEP_EN.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HALF_PIX[7:0]	7:0	IP2 separation half pix number in user mode.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	HALF_PIX_USR_EN	7	IP2 separation user mode.	
	-	6:3	Reserved.	
	HALF_PIX[10:8]	2:0	See description of '102FD8h'.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSP_PH0_COEF0[7:0]	7:0	RSP_PH0_COEF0.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x80**	**Access : R/W**
	RSP_PH0_COEF1[7:0]	7:0	RSP_PH0_COEF1.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSP_PH1_COEF0[7:0]	7:0	RSP_PH1_COEF0.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x40**	**Access : R/W**
	RSP_PH1_COEF1[7:0]	7:0	RSP_PH1_COEF1.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RSP_LINE7_PH	7	RSP_LINE7_PH.	
	RSP_LINE6_PH	6	RSP_LINE6_PH.	
	RSP_LINE5_PH	5	RSP_LINE5_PH.	

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IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RSP_LINE4_PH	4	RSP_LINE4_PH.	
	RSP_LINE3_PH	3	RSP_LINE3_PH.	
	RSP_LINE2_PH	2	RSP_LINE2_PH.	
	RSP_LINE1_PH	1	RSP_LINE1_PH.	
	RSP_LINE0_PH	0	RSP_LINE0_PH.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RSP_FIELD_USR_EN	6	Re-sample local toggle field flag.	
	RSP_FIELD_INV	5	Re-sample field polarity invert.	
	RSP_FIELD_EN	4	Re-sample field mode.	
	-	3:1	Reserved.	
	RESAMP_EN	0	RESAMP_EN.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_CLR[7:0]	7:0	DUMMY_CLR.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_CLR[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[7:0]	7:0	DUMMY_SET.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[15:8]	7:0	See description of '102FFEh'.	

IP1_S Register (Bank = 102F, Sub-bank = 03)

IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0		
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. #0: Left result. #1: right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. #0: Not clear. #1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. #0: Update every frame. #1: Keep the history value.	
	JITTER	3	JITTER function Result. #0: No JITTER. #1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. #0: Update every frame. #1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. #0: Result not ready. #1: Result ready.	
	ATS_EN	0	Auto position function Enable. #0: Disable. #1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F21h)	THOLD[3:0]	7:4	Auto position Valid Data Value. #0000: Valid if data >= 0000 0000. #0001: Valid if data >= 0001 0000. #0010: Valid if data >= 0010 0000. .. #1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Positoin Force Pixel Mode. #0 : DE or Pixel decide by the Source. #1 : Force Pixel Mode.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Aoto Gain Value. (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Bh)	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Bh)	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F42h)	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ah)	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x01**	**Access : R/W**
	_	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. #0: Can gate the GOP clock. #1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. #0: Don't gate the idclk. #1: Can gate the idclk.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:3	Reserved.	
	ATS_B_SKIP	2	Auto search ignore B data.	
	ATS_G_SKIP	1	Auto search ignore G data.	
	ATS_R_SKIP	0	Auto search ignore R data.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DE_BYPASS_MODE	7	Use input DE to replace SPRange_H as output DE.	
	-	6:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Ah)	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Atuto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	
40h ~ 43h (102F80h ~ 102F86h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F93h)	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	
	FDET_STATUS_INTLAC_DET0	0	Mode detect result 0.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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IP1_S Register (Bank = 102F, Sub-bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	

IP2_S Register (Bank = 102F, Sub-bank = 04)

IP2_S Register (Bank = 102F, Sub-bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	

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IP2_S Register (Bank = 102F, Sub-bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	-	6:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_S Register (Bank = 102F, Sub-bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Fh)	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	-	4:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x08**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	
	YDELAY_EN	4	Y delay enable.	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	44TO42_DITH_EN	0	444 to 422 filter dith enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FILL_BLACK_NUM[5:0]	5:0	Fill black number.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILL_BLACK_ACT	7	FILL_BLACK_ACT.	
	FILL_BLACK_CLR	6	Clear fill_black register manually.	
	-	5:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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IP2_S Register (Bank = 102F, Sub-bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_HSK_MD	5	Ip2 osd handshaking mode.	
	FORCE_OSD_HSK	4	Force ip2 to osd in handshaking mode.	
	IP2_MVOP_DAT_SEL	3	0: IP_f1 connect to DC1 IP_f2 connect to DC0 1:IP1_f1 connect to DC0 IP2_f2 connect to DC1.	
	IP2_VS_SEL	2	1: Use mvop_vs to generate vs to opvs 0:use ip1_vs to generate vs to opvs.	
	FORCE_PRE2LAST	1	1: Use vsd last valid as pre align 0: use original pre align.	
	MVOP_DIN_EN	0	1: Data is form mvop 0: form yc delay.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RANDOM_SEL[1:0]	5:4	//random mode 0:1 1:3/4 2:1/2 3:1/4 rdy.	
	-	3:2	Reserved.	
	PAT_DATA_SEL	1	//1: use patgen data 0:use input data;	
	PAT_TIMING_SEL	0	//1: use patgen timing 1:use input timing;	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0xD0**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen h total.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0xE0**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen v total.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x40**	**Access : R/W**
	H_BLOCK[7:0]	7:0	Patgen h block.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen v block.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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IP2_S Register (Bank = 102F, Sub-bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	V_BLOCK[9:8]	1:0	See description of '102F28h'.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:0	Reserved.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IP2DIP_SEL	0	IP2 to DIP source select: 1'b0: before HSD/VSD. 1'b1: after HSD/VSD.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IP2VE_VS_SEL	2	IP to VE vsync selection. 1'b0: IP1 vsync. 1'b1: original vsync.	
	IP2VE_CAP_EN	1	IP to VE cap enable.	
	IP2VE_PATH_EN	0	IP to VE enable.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIN_CTRL_EN	7	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	6	IP2 VSD input line count number setting enable.	
	-	5	Reserved.	
	VSD_IN_NUM_USR[12:8]	4:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VOUT_CTRL_EN	7	IP2 VSD output line count control enable.	
	-	6:5	Reserved.	
	VSD_OUT_NUMBER[12:8]	4:0	See description of '102F6Eh'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_HSD_OUT_CNT[12:8]	4:0	See description of '102F7Ch'.	

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IP2_S Register (Bank = 102F, Sub-bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_VSD_OUT_CNT[12:8]	4:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable bpseudo blanking.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x08**	**Access : R/W**
	SPLIT_BLANK[7:0]	7:0	Pseudo blank cycle.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable dat_adj to src force ready.	
	ADJ_AUTO	0	ADJ_AUTO.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[7:0]	7:0	Debug.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_DIFF[7:0]	7:0	Number of fifo.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_CLR[7:0]	7:0	DUMMY_CLR.	
7Eh	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_S Register (Bank = 102F, Sub-bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FFDh)	DUMMY_CLR[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[7:0]	7:0	DUMMY_SET.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[15:8]	7:0	See description of '102FFEh'.	

PNR Register (Bank = 102F, Sub-bank = 05)

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F1	7	Sub Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F1	6	Sub Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F1	5	Sub Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F1	4	Sub Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F1	3	Sub Window Post Noise Reduction for Y.	
	PNR_ENC_F1	2	Sub Window Post Noise Reduction for C.	
	RATIOYC_F1[1:0]	1:0	Sub Wimdow Motion Ratio.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F1	0	Sub Window select next field inverter for noc_sel.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F1	7	Sub Window DHD 3f mode enable.	
	PCCS_3F_EN_F1	6	Sub Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F1	4	Sub Window PCCS dither enable.	
	DHD_DITHER_EN_F1	3	Sub Window DHD dither enable.	
	PNR_BYPASS_F1	2	Sub Window PNR function bypass enable.	
	NR_EN_F1	1	Sub Window Post NR enable.	
	PCCS_EN_F1	0	Sub Window Post CCS enable.	
02h	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**

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PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F05h)	-	7	Reserved.	
	PAL_EN_F1	6	Sub Window PAL enable.	
	-	5:0	Reserved.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F1[2:0]	7:5	Sub Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F1[2:0]	4:2	Sub Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F1	1	Sub Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F1	0	Sub Window user-defined Y motion threshold enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	NR_Y_ROUND_F1	6	Sub Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F1	5	Sub Window enable select max motion for c.	
	YMOT_MAX_SEL_F1	4	Sub Window enable select max motion for y.	
	CMOT_DIV_MODE_F1[1:0]	3:2	Sub Window C motion divide mode.	
	YMOT_DIV_MODE_F1[1:0]	1:0	Sub Window Y motion divide mode.	
0Bh (102F16h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:3	Reserved.	
	DITHER_FRAME_RST_CNT[1:0]	2:1	Dither frame reset count.	
	DITHER_FRAME_RST_EN	0	Dither frame reset enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_F2[1:0]	1:0	Main Wimdow Motion Ratio.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:1	Reserved.	

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PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for noc_sel.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F2	7	Main Window DHD 3f mode enable.	
	PCCS_3F_EN_F2	6	Main Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F2	4	Main Window PCCS dither enable.	
	DHD_DITHER_EN_F2	3	Main Window DHD dither enable.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PAL_EN_F2	6	Main Window PAL enable.	
	-	5:0	Reserved.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F2	5	Main Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F2	4	Main Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F2	3	Main Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F2	2	Main Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F2	1	Main Window DHD YMR02 enable.	

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PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_EN_F2	0	Main Window DHD enable.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F1	5	Sub Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F1	4	Sub Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F1	3	Sub Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F1	2	Sub Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F1	1	Sub Window DHD YMR02 enable.	
	DHD_EN_F1	0	Sub Window DHD enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR02_TH[5:0]	5:0	DHD YMR02 threshold.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR02_GAIN[2:0]	2:0	DHD YMR02 gain.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR04_TH[5:0]	5:0	DHD YMR04 threshold.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR04_GAIN[2:0]	2:0	DHD YMR04 gain.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_CVAL_GAIN[7:0]	7:0	DHD C value gain.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_DIFFPIX_GAIN[3:0]	3:0	DHD pixel diff gain.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR02_TH[5:0]	5:0	DHD C motion02 threshold.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR02_GAIN[2:0]	2:0	DHD C motion02 gain.	
25h	**REG102F4A**	**7:0**	**Default : 0x10**	**Access : R/W**

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PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ah)	-	7:6	Reserved.	
	DHD_CMR04_TH[5:0]	5:0	DHD C motion04 threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR04_GAIN[2:0]	2:0	DHD C motion04 gain.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x30**	**Access : R/W**
	DHD_CEDGE_GAIN[7:0]	7:0	DHD C edge gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_YEDGE_GAIN[7:0]	7:0	DHD Y edge gain.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_DEBUG0_EN	7	DHD debug0 enable.	
	DHD_DEBUG1_EN	6	DHD debug1 enable.	
	-	5:0	Reserved.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_YMR_IIR_ALPHA[2:0]	6:4	DHD YMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_YMR_IIR_STEP[1:0]	1:0	DHD YMR IIR step.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_CMR_IIR_ALPHA[2:0]	6:4	DHD CMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_CMR_IIR_STEP[1:0]	1:0	DHD CMR IIR step.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_CEDGE_TH[3:0]	3:0	DHD C edge threshold.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YEDGE_TH[5:0]	5:0	DHD Y edge threshold.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_CVAL_TH[3:0]	3:0	DHD C value threshold.	
4Ch	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**

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PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F98h)	-	7	Reserved.	
	INV_SAT_OFFSET[6:0]	6:0	PCCS invert saturation offset.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INV_SAT_POWNUM[2:0]	6:4	PCCS invert saturation pownum.	
	INV_SAT_W[3:0]	3:0	PCCS invert saturation weight.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TDELTA_C_POWNUM[3:0]	7:4	PCCS inv-saturation delta pownum.	
	TDELTA_C_W[3:0]	3:0	PCCS inv-saturation delta weight.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS Y Fn Fn-2 coring threshold.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS Y Fn Fn-2 pre wieght.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS Y Fn Fn-2 post pownum.	
	-	3	Reserved.	
	YDIFF_FNFN2_POST_W[2:0]	2:0	PCCS Y Fn Fn-2 post wieght.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-2 coring threshold.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS C Fn Fn-2 pre wieght.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-2 post pownum.	
	-	3	Reserved.	
	CDIFF_FNFN2_POST_W[2:0]	2:0	PCCS C Fn Fn-2 post wieght.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RC_EV_POWNUM[2:0]	6:4	PCCS real color edge value pownum.	
	RC_EV_W[3:0]	3:0	PCCS real color edge value weight.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCMODIFYFAC_POWNUM[3:0]	7:4	PCCS cross color edge value pownum.	
	CCMODIFYFAC_W[3:0]	3:0	PCCS cross color edge value weight.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	YEDGEFAC_UP_OFFSET[7:0]	7:0	PCCS Y edge offset.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YEDGEFAC_POWNUM[2:0]	6:4	PCCS Y edge pownum.	
	YEDGEFAC_W[3:0]	3:0	PCCS Y edge weight.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BLEND_LPF_TURN_OFF	1	PCCS factor low-pass filter off.	
	MEDIAN_TURN_OFF	0	PCCS factor median filter off.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INV_CDIFF_FNFN2_POWNUM[3:0]	7:4	PCCS invert C Fn Fn-2 diff pownum.	
	INV_CDIFF_FNFN2_W[3:0]	3:0	PCCS invert C Fn Fn-2 diff weight.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-4 diff threshold.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN4_PRE_W[2:0]	2:0	PCCS C Fn Fn-4 diff pre weight.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-4 diff post pownu,	
	-	3	Reserved.	
	CDIFF_FNFN4_POST_W[2:0]	2:0	PCCS C Fn Fn-4 diff post weight.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_3F_POST_POWNUM[2:0]	6:4	PCCS Y 3F diff post pownum.	
	-	3	Reserved.	

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PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	YDIFF_3F_POST_W[2:0]	2:0	PCCS Y 3F diff post weight.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[7:0]	7:0	PCCS Table.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[15:8]	7:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[23:16]	7:0	See description of '102FC0h'.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[31:24]	7:0	See description of '102FC0h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[39:32]	7:0	See description of '102FC0h'.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[47:40]	7:0	See description of '102FC0h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[55:48]	7:0	See description of '102FC0h'.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[63:56]	7:0	See description of '102FC0h'.	
78h ~ 78h (102FF0h ~ 102FF1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DNR Register (Bank = 102F, Sub-bank = 06)

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F1_DNR_CORE_EN	1	F1 DNR CORE FUNCTION EN.	
	F1_DNR_EN	0	F1 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F1_NR_TABLE_SEL_C	1	F1 DNR Table C Mapping Select. #0 : non-linear. #1 : linear.	
	F1_NR_TABLE_SEL_Y	0	F1 DNR Table Y Mapping Select. #0 : non-linear. #1 : linear.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F1_ROUND_MODE_C[1:0]	3:2	F1 DNR C blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
	F1_ROUND_MODE_Y[1:0]	1:0	F1 DNR Y blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F1_MAX_MOT_ENABLE_C	3	F1_MAX_MOT_ENABLE_C.	
	F1_MAX_MOT_ENABLE_Y	2	F1_MAX_MOT_ENABLE_Y.	
	F1_DNR_FILTER_EN_C	1	F1_DNR_FILTER_EN_C.	
	F1_DNR_FILTER_EN_Y	0	F1_DNR_FILTER_EN_Y.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_FILTER_DIV0_C[2:0]	7:5	F1_DNR_FILTER_DIV0_C.	
	F1_DNR_FILTER_DIV0_Y[2:0]	4:2	F1_DNR_FILTER_DIV0_Y.	
	-	1:0	Reserved.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_FILTER_MODE_C[1:0]	7:6	F1_DNR_FILTER_MODE_C.	
	F1_DNR_FILTER_MODE_Y[1:0]	5:4	F1_DNR_FILTER_MODE_Y.	
	F1_DNR_FILTER_DIV1_C[1:0]	3:2	F1_DNR_FILTER_DIV1_C.	
	F1_DNR_FILTER_DIV1_Y[1:0]	1:0	F1_DNR_FILTER_DIV1_Y.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. #0 : non-linear. #1 : linear.	
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. #0 : non-linear. #1 : linear.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.	
	SNR_EN	0	F2 SNR FUNCTION EN.	
24h (102F48h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.	
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.	
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	
27h	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**

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DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Eh)	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_SHARP_LEVEL[3:0]	3:0	SNR sharpness level.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0xBD**	**Access : R/W**
	F1_DNR_TABLEY_0[7:0]	7:0	F1 DNR TABLEY_0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x79**	**Access : R/W**
	F1_DNR_TABLEY_0[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x56**	**Access : R/W**
	F1_DNR_TABLEY_1[7:0]	7:0	F1 DNR TABLEY_1.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x34**	**Access : R/W**
	F1_DNR_TABLEY_1[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x12**	**Access : R/W**
	F1_DNR_TABLEY_2[7:0]	7:0	F1 DNR TABLEY_2.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_2[15:8]	7:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_3[7:0]	7:0	F1 DNR TABLEY_3.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_3[15:8]	7:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0xBD**	**Access : R/W**
	F1_DNR_TABLEC_0[7:0]	7:0	F1 DNR TABLEC_0.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x79**	**Access : R/W**
	F1_DNR_TABLEC_0[15:8]	7:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x56**	**Access : R/W**
	F1_DNR_TABLEC_1[7:0]	7:0	F1 DNR TABLEC_1.	

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DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x34**	**Access : R/W**
	F1_DNR_TABLEC_1[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x12**	**Access : R/W**
	F1_DNR_TABLEC_2[7:0]	7:0	F1 DNR TABLEC_2.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_2[15:8]	7:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_3[7:0]	7:0	F1 DNR TABLEC_3.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_3[15:8]	7:0	See description of '102F6Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h	**REG102F8B**	**7:0**	**Default : 0x34**	**Access : R/W**

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DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F8Bh)	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
58h ~ 5Bh (102FB0h ~ 102FB7h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
70h (102FE0h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
71h (102FE2h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	F2_WIN_EN	0	F2 DNR/SNR active window enable.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_XSTART[7:0]	7:0	F2 DNR/SNR active window start X.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XSTART[10:8]	2:0	See description of '102FE8h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_YSTART[7:0]	7:0	F2 DNR/SNR active window start Y.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YSTART[10:8]	2:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x68**	**Access : R/W**
	F2_WIN_XEND[7:0]	7:0	F2 DNR/SNR active window end X.	
76h	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**

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DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FEDh)	-	7:3	Reserved.	
	F2_WIN_XEND[10:8]	2:0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0xF0**	**Access : R/W**
	F2_WIN_YEND[7:0]	7:0	F2 DNR/SNR active window end Y.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YEND[10:8]	2:0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F1[7:0]	7:0	F1 hcnt for debug.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	STATUS_HCNT_F1[10:8]	2:0	See description of '102FF0h'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F1[7:0]	7:0	F1 vcnt for debug.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F1	7	F1 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F1[10:8]	2:0	See description of '102FF2h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F2[7:0]	7:0	F2 hcnt for debug.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	STATUS_HCNT_F2[10:8]	2:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F2[7:0]	7:0	F2 vcnt for debug.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F2	7	F2 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F2[10:8]	2:0	See description of '102FF6h'.	

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FILM Register (Bank = 102F, Sub-bank = 0A)

FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7	Reserved.	
	DET_FIELD_SEL_LC	6	DET_FIELD_SEL_LC.	
	-	5	Reserved.	
	DIFF_TH[12:8]	4:0	Difference threshold.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_CUR_ERROR_TH_F2[7:0]	7:0	32 current error threshold.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_PRE_ERROR_TH_F2[15:8]	7:0	32 previous error threshold.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_CUR_ERROR_TH_F2[7:0]	7:0	22 current error threshold.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_PRE_ERROR_TH_F2[15:8]	7:0	22 previous error threshold.	
05h ~ 05h (102F0Ah ~ 102F0Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	32_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	32 total error max th.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x7F**	**Access : R/W**
	32_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	32 total error sum th.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x08**	**Access : R/W**
	22_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	22 total error max th.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x7F**	**Access : R/W**
	22_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	22 total error sum th.	
08h ~ 09h (102F10h ~ 102F12h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	

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FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FIX_DIFF_TH[12:8]	4:0	Cur error sum th.	
0Ah ~ 0Bh (102F14h ~ 102F17h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[7:0]	7:0	F2 counter 1 threshold.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[7:0]	7:0	F2 counter 3 threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[7:0]	7:0	F2 counter fix threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[15:8]	7:0	See description of '102F1Ch'.	
0Fh ~ 10h (102F1Eh ~ 102F20h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x30**	**Access : R/W**
	FILM32_EN_F2	7	F2 32 film mode enable.	
	FILM22_EN_F2	6	F2 22 film mode enable.	
	-	5:4	Reserved.	
	PRE32_F2	3	F2 pre32.	
	-	2:0	Reserved.	
11h ~ 14h (102F22h ~ 102F29h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xEE**	**Access : R/W**
	MOT_TH_PATCH_F2[7:4]	7:4	F2 patch motion threshold.	
	FM_MOT_PIXTH_F2[3:0]	3:0	F2 motion ratio threshold.	

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FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x14**	**Access : R/W**
	FM_MOT_CNTTH_F2[15:8]	7:0	F2 unmatch threshold.	
16h ~ 17h (102F2Ch ~ 102F2Eh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FILM32_N1_EN_F2	7	F2 N1 film32 enable.	
	FILM22_N1_EN_F2	6	F2 N1 film22 enable.	
	-	5:0	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[7:0]	7:0	F2 read status.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[15:8]	7:0	See description of '102F30h'.	
19h ~ 19h (102F32h ~ 102F33h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[7:0]	7:0	F2 patch read status.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[15:8]	7:0	See description of '102F34h'.	
1Bh ~ 1Dh (102F36h ~ 102F3Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x50**	**Access : R/W**
	MULT_COEF_F2[7:4]	7:4	F2 multiplicant ratio.	
	-	3:1	Reserved.	
	RELATIVE_FM_EN_F2	0	F2 relative film mode frame diff enable.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x05**	**Access : R/W**
	LOWER_BOUND_FM_32_F2[15:8]	7:0	F2 frame diff lower bound.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[7:0]	7:0	F2 frame diff upper bound.	

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FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x03**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x0F**	**Access : R/W**
	CHECK_SEQ_F2[7:0]	7:0	F2 lock threshold to enter 22.	
20h ~ 22h (102F41h ~ 102F45h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x44**	**Access : R/W**
	SPEEDUP_STEP_F2[7:4]	7:4	F2 speedup step.	
	SPEEDUP_SHIFT_F2[3:0]	3:0	F2 speedup shift value.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x80**	**Access : R/W**
	SPEEDUP_EN_F2	7	F2 speedup enable.	
	-	6:0	Reserved.	
24h ~ 25h (102F48h ~ 102F4Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
40h ~ 43h (102F80h ~ 102F87h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
55h ~ 57h (102FAAh ~ 102FAFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SNR Register (Bank = 102F, Sub-bank = 0C)

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F1	6	De-blocking and SNR active threshold motion ratio enable F1.	

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SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SNR_MOTION_RATIO_EN_F1	5	SNR motion ratio enable F1.	
	SNR_EN_F1	4	SNR enable F1.	
	-	3	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F2	2	De-blocking and SNR active threshold motion ratio enable F2.	
	SNR_MOTION_RATIO_EN_F2	1	SNR motion ratio enable F2.	
	SNR_EN_F2	0	SNR enable F2.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x48**	**Access : R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	-	4	Reserved.	
	SNR_STRENGTH_GAIN_F2[3:0]	3:0	SNR strength F2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_STRENGTH_GAIN_F1[3:0]	3:0	SNR strength F1.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0xCF**	**Access : R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x69**	**Access : R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x24**	**Access : R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x01**	**Access : R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
50h	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**

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SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FA0h)	SNR_NM_DITHER_EN	7	Noise masking dither enable.	
	-	6	Reserved.	
	SNR_NM_MOTION_RATIO_EN_F1	5	Noise masking motion ratio enable F1.	
	SNR_NM_FILTER_EN_F1	4	Noise masking enable F1.	
	-	3:2	Reserved.	
	SNR_NM_MOTION_RATIO_EN_F2	1	Noise masking motion ratio enable F2.	
	SNR_NM_FILTER_EN_F2	0	Noise masking enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_15[1:0]	7:6	Reserved.	
	-	5:0	Reserved.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SNR_MR_LPF_EN_F1	4	De-blocking and SNR motion ratio low pass filter enable F1 (lpf is 3x3 mask).	
	-	3:1	Reserved.	
	SNR_MR_LPF_EN_F2	0	De-blocking and SNR motion ratio low pass filter enable F2 (lpf is 3x3 mask).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_9[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F2[5:0]	5:0	Noise masking gain F2.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_10[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F1[5:0]	5:0	Noise masking gain F1.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SNR_NM_MIN_THRD[3:0]	7:4	Noise masking min threshold bound.	
	SNR_NM_MAX_THRD[3:0]	3:0	Noise masking max threshold bound.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_01[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_01.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_23[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_23.	
59h	**REG102FB2**	**7:0**	**Default : 0x54**	**Access : R/W**

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SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB2h)	SNR_STD_LOW_MOTION_TABLE_45[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_45.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_67[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_67.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_89[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_89.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_AB[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_AB.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_CD[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_CD.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_EF[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_EF.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_MOTION_TABLE_01[7:0]	7:0	SNR motion ratio LUT_01.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_MOTION_TABLE_23[7:0]	7:0	SNR motion ratio LUT_23.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_MOTION_TABLE_45[7:0]	7:0	SNR motion ratio LUT_45.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_MOTION_TABLE_67[7:0]	7:0	SNR motion ratio LUT_67.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_MOTION_TABLE_89[7:0]	7:0	SNR motion ratio LUT_89.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_MOTION_TABLE_AB[7:0]	7:0	SNR motion ratio LUT_AB.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_MOTION_TABLE_CD[7:0]	7:0	SNR motion ratio LUT_CD.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_MOTION_TABLE_EF[7:0]	7:0	SNR motion ratio LUT_EF.	
6Ch	**REG102FD8**	**7:0**	**Default : 0x10**	**Access : R/W**

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SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FD8h)	SNR_NM_MOTION_TABLE_01[7:0]	7:0	Noise masking motion ratio LUT_01.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_NM_MOTION_TABLE_23[7:0]	7:0	Noise masking motion ratio LUT_23.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_NM_MOTION_TABLE_45[7:0]	7:0	Noise masking motion ratio LUT_45.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_NM_MOTION_TABLE_67[7:0]	7:0	Noise masking motion ratio LUT_67.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_NM_MOTION_TABLE_89[7:0]	7:0	Noise masking motion ratio LUT_89.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_NM_MOTION_TABLE_AB[7:0]	7:0	Noise masking motion ratio LUT_AB.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_NM_MOTION_TABLE_CD[7:0]	7:0	Noise masking motion ratio LUT_CD.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_NM_MOTION_TABLE_EF[7:0]	7:0	Noise masking motion ratio LUT_EF.	
70h ~ 70h (102FE0h ~ 102FE1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

RA Register (Bank = 102F, Sub-bank = 0D)

RA Register (Bank = 102F, Sub-bank = 0D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAX_LENGTH_R0[7:0]	7:0	MAX_LENGTH_R0.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAX_LENGTH_R1[7:0]	7:0	MAX_LENGTH_R1.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAX_LENGTH_ALL[7:0]	7:0	MAX_LENGTH_ALL.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HP_CUT_MIN0[7:0]	7:0	HP_CUT_MIN0.	
04h	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**

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RA Register (Bank = 102F, Sub-bank = 0D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F09h)	HP_CUT_IN_EN0	7	HP_CUT_IN_EN0.	
	-	6:0	Reserved.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HP_CUT_MIN1[7:0]	7:0	HP_CUT_MIN1.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HP_CUT_IN_EN1	7	HP_CUT_IN_EN1.	
	-	6:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HPMASK[1:0]	1:0	HPMASK.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	REQ_MASK[1:0]	1:0	REQ_MASK.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RST	7	SW_RST.	
	-	6:1	Reserved.	
	MRQ_MIU_SEL	0	MRQ_MIU_SEL.	
08h ~ 09h (102F10h ~ 102F13h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ch ~ 0Fh (102F18h ~ 102F1Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN	4	Reg_scm_arb_bypas_en.	
	SCM_ARB_SW_RST	3	SCM_ARB_SW_RST.	
	SCM_ARB_THD_HIT_LAST_EN	2	SCM_ARB_THD_HIT_LAST_EN.	
	SCM_ARB_FLOW_CTRL_EN	1	SCM_ARB_FLOW_CTRL_EN.	
	SCM_ARB_RDY1_FIRST	0	SCM_ARB_RDY1_FIRST.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x0C**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM[7:0]	7:0	SCM_ARB_MAX_REQ_NUM.	

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RA Register (Bank = 102F, Sub-bank = 0D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_RDY0_THD[7:0]	7:0	SCM_ARB_RDY0_THD.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_RDY1_THD[7:0]	7:0	SCM_ARB_RDY1_THD.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO_BO[3:0]	7:4	Main windowborder outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	
	-	3:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	S_VDEEND[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F30h)	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
19h ~ 1Ah (102F32h ~ 102F35h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F3Ah'.	
1Eh	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Ch)	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CM32[12:8]	4:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SMEN	7	SVM Main window Enable.	
	SMTE	6	SVM Main window Tap Enable.	
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
	SSWEN	3	SVM Sub window Enable.	
	SSWETE	2	SVM Sub window Tap Enable.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.	
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.	
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data. 11: Y with tap filter.	
	SCORING[3:0]	3:0	SVM Coring.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	-	4:2	Reserved.	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TO_MISC_NON_MAIN_WIN_SEL_PRE[1:0]	1:0	OSD blending window select. 2'b00 select main window as OSD window. 2'b01 select sub window as OSD window. others: Select main and sub window as OSD window.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_CHECK_ALPHA_PRE	7	Check pre osd blending alpha value. 1: Enable. 0: Disable.	
	OSD_CHECK_ALPHA	6	Check osd blending alpha value. 1: Enable. 0: Disable.	
	-	5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:4	Reserved.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (102F58h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	RESERVED[1:0]	6:5	RESERVED.	
	-	4:0	Reserved.	
2Dh ~ 2Fh (102F5Ah ~ 102F5Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (bri_function) for main window R.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (bri_function) for main window G.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (bri_function) for main window B.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '102F70h'.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_R[7:0]	7:0	Brightness offset (bri_function) for sub window R.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (bri_function) for sub window G.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (bri_function) for sub window B.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '102F7Ch'.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '102F82h'.	
42h ~ 45h (102F84h ~ 102F8Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CAP_STAGE[1:0]	5:4	Capture stage selection. 0: Before osd. 1: After osd. 2: VIP output.	
	-	3:0	Reserved.	
46h (102F8Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F8Fh)	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F9Ah'.	
4Eh	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F9Ch)	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FA7h)	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FREEZ_VCNT_VALUE[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when REG_NEW_LOCK_POINT is set high.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LOCK_VCNT_VALUE[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_VS_EN	6	Enable pseudo vsync for freeze region.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select insert_end point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_MAIN_R_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_R_MIN_LIMIT. REG_MAIN_R_MIN_SIGN = 0: MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '102FB2h'.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_MAIN_G_MIN_SIGN = 1: MAIN_G_MIN = -MAIN_G_MIN_LIMIT. REG_MAIN_G_MIN_SIGN = 0: MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_MAIN_B_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_B_MIN_LIMIT. REG_MAIN_B_MIN_SIGN = 0: MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '102FBAh'.	
5Eh	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FBCh)	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value , s.12 format sign bit is bit-12. REG_SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. REG_SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_SUB_G_MIN_SIGN = 1: MAIN_G_MIN = -SUB_G_MIN_LIMIT. REG_SUB_G_MIN_SIGN = 0: MAIN_G_MIN = SUB_G_MIN_LIMIT.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_SUB_B_MIN_SIGN = 1: MAIN_R_MIN = -SUB_B_MIN_LIMIT. REG_SUB_B_MIN_SIGN = 0: MAIN_R_MIN = SUB_B_MIN_LIMIT.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '102FC6h'.	
64h ~ 69h (102FC8h ~ 102FD3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[7:0]	7:0	New add function for RGB_compression.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[15:8]	7:0	See description of '102FD8h'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FWC_SUB_EN	4		
	-	3:2	Reserved.	
	FWC_DITHER_EN	1		
	FWC_MAIN_EN	0		
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0		
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FWC_SLOPE[5:0]	5:0		
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	FWC_CTH[7:0]	7:0		
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[7:0]	7:0		
72h	**REG102FE5**	**7:0**	**Default : 0x80**	**Access : R/W**

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FE5h)	FWC_DELTA_R[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '102FE4h'.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '102FE4h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '102FE4h'.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[47:40]	7:0	See description of '102FE4h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '102FE4h'.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '102FE4h'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '102FE4h'.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '102FE4h'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '102FE4h'.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '102FE4h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[7:0]	7:0		
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '102FF4h'.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '102FF4h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '102FF4h'.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '102FF4h'.	

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S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '102FF4h'.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '102FF4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '102FF4h'.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '102FF4h'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '102FF4h'.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '102FF4h'.	

SCMI Register (Bank = 102F, Sub-bank = 12)

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data config from mode 5 change to mode 4.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force madi off.	
	MADI_FORCE_ON_F2	4	F2 force madi on.	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	-	2	Reserved.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	OPM_LINEAR_BASE_SEL_F2	6	F2 linear mode base address selection.	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	IPM_LINEAR_EN_F2	4	F2 IP linear address enable.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	Y8_M4_ONLY_MODE_F2	3	F2 FB store Y8/M4 only mode.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	Y8_ONLY_MODE_F2	2	F2 FB store Y-8bits only.	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY04_14_14	6	F2 FB store Y-8bits only.	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_BYPASS_INTERLACE_FILM_F2	4	Film-supported bypass interlace mode.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F2	7	F2 memysnc write bank reset.	
	IPM_WREQ_HPRI_SEL_F2	6	F2 ipm wreq high priority selection: 1'b0: ipm local priority. 1'b1: ip2_adj priority.	
	FRC_FREEMD_F2	5	F2 Force output odd/even toggle when 2DDi for interlace input.	
	MIU_SELECT_F2	4	F2 access MIU0 or MIU1 select.	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x02**	**Access : R/W**
	DUMMY05_10_15[5:0]	7:2		
	OPM_F1_EN	1	Enable OPM F1 register.	
	BK_FIELD_SEL_F2	0	F2 memysnc fd selection.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WBANK_ALIGN_USR_F2[1:0]	3:2	[0] wbank align user mode. [1] wbank force align.	
	-	1:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RW_BANK_MAP_MSB_F2	7	F2 msb bit of read/write bank mapping mode.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_RBANK_SEL_MSB_F2	6	F2 OP force read bank select msb.	
	-	5:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x88**	**Access : R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x40**	**Access : R/W**
	RW_BANK_MAP_F2[2:0]	7:5	F2 read/write bank mapping mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IPM_BASE_ADDR0_F2[26:24]	2:0	See description of '102F10h'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_OFFSET_F2[12:8]	4:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_FETCH_NUM_F2[12:8]	4:0	See description of '102F1Eh'.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F20h'.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR0_F2[26:24]	2:0	See description of '102F20h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR1_F2[26:24]	2:0	See description of '102F24h'.	
14h ~ 14h (102F28h ~ 102F29h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F2[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F2Eh'.	
18h	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F30h)	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_EN_F2	7	F2 IP line count limit enable.	
	-	6:5	Reserved.	
	IPM_VCNT_LIMIT_NUM_F2[12:8]	4:0	See description of '102F30h'.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FORCE_MUTE_IPW_ENABLE_F2	5	Force IPM enable at av-mute case.	
	FIELD_NUM_F2[4:0]	4:0	F2 field number.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_FIELD_NUM_DEFINE_F2	7	Enable OPM F2 field number define.	
	OPM_FIELD_NUM_F2[4:0]	6:2	OPM F2 field number.	
	OPM_8READ_EN_F2	1	F2 opm 8read mode enable.	
	OPM_6READ_EN_F2	0	F2 opm 6read mode enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_EN_F2	7	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	6	F2 IP write limit flag 0: maximum 1: minimum.	
	-	5:3	Reserved.	
	IPM_W_LIMIT_ADR_F2[26:24]	2:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_EN_F2	7	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[14:8]	6:0	See description of '102F38h'.	
1Dh ~ 1Fh	**-**	**7:0**	**Default : -**	**Access : -**

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Ah ~ 102F3Fh)	-	-	Reserved.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_FLOW_CTRL_CNT[7:0]	7:0	OPW request flow control count.	
27h	**REG102F4E**	**7:0**	**Default : 0x88**	**Access : R/W**

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Eh)	OPW_VP_CNT_CLR	7	OPW write mask field count clear.	
	OPW_MASK_MODE[2:0]	6:4	OPW write mask number by field.	
	OPW_STATUS_CLR	3	OPW status clear enable.	
	OPW_REQ_RST	2	OPW write request reset.	
	-	1	Reserved.	
	OPW_WREQ_OFF_F2	0	OPW write request disable.	
27h ~ 28h (102F4Fh ~ 102F51h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_THRD[7:0]	7:0	OPW FIFO threshold for read request.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_HPRI[7:0]	7:0	OPW high priority threshold for read request.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPW_WREQ_MAX[7:0]	7:0	OPW read request max number.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x22**	**Access : R/W**
	OPW_WFIFO_DEPTH[7:0]	7:0	OPW line buffer length for memory data write.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at real line case.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at real line case.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPM_3D_SBS_FORCE_EN_F2	1	F2 IPM 3D side by side input enable.	
	IPM_3D_EN_F2	0	F2 IPM 3D input enable.	
30h ~ 32h (102F61h ~ 102F64h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
33h ~ 33h (102F66h ~ 102F67h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY34_7_7	7	HDMI 3D OPM side by side read using PIP.	
	-	6:0	Reserved.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[15:8]	7:0	See description of '102F6Ch'.	
37h ~ 37h (102F6Eh ~ 102F6Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[15:8]	7:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[15:8]	7:0	See description of '102F7Ch'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x18**	**Access : R/W**
	DUMMY40_5_15[2:0]	7:5		
	OPM_LB_CEN_MODE	4	OP Line buffer power ctrl.	
	UPDATE_MEM_CONFIG_EN	3	Update memory format enable.	
	-	2	Reserved.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_REG_DBF_EN_F2	1	F2 Register latch with input V sync enable.	
	OPM_REG_DBF_EN	0	Register latch with output V sync enable.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY40_5_15[10:3]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY41_7_6[1:0]	7:6		
	-	5:0	Reserved.	
41h ~ 42h (102F83h ~ 102F84h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MADI_FORCE_OFF_F1	5	F1 force madi off.	
	MADI_FORCE_ON_F1	4	F1 force madi on.	
	-	3:0	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_LINEAR_EN_F1	4	F1 IP linear address enable.	
	OPM_4READ_EN_F1	3	F1 OP read 4 fields enable.	
	OPM_3READ_EN_F1	2	F1 OP read 3 fields enable.	
	OPM_2READ_EN_F1	1	F1 OP read 2 fields enable.	
	OPM_1READ_EN_F1	0	F1 OP read 1 field enable.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	FILM_HIGH_PRI_F1	3	F1 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F1	2	F1 OP film dot line data select.	
	DOT_LN_PON_SEL_F1	1	F1 OP MADi dot line data select.	
	-	0	Reserved.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DUMMY44_2_3[1:0]	3:2		
	-	1:0	Reserved.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
44h (102F89h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F1	7	F1 memysnc write bank reset.	
	IPM_WREQ_HPRI_SEL_F1	6	F1 ipm wreq high priority selection: 1'b0: ipm local priority. 1'b1: ip2_adj priority.	
	-	5:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY45_9_15[6:0]	7:1		
	BK_FIELD_SEL_F1	0	F2 memysnc fd selection.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY46_4_7[3:0]	7:4		
	WBANK_ALIGN_USR_F1[1:0]	3:2	[0] wbank align user mode. [1] wbank force align.	
	-	1	Reserved.	
	WBANK_SRC_SEL_F1	0	F1 Wbank src selection: 1'b0: original. 1'b1: from sc1.	
46h ~ 49h (102F8Dh ~ 102F93h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
4Eh ~ 4Fh (102F9Ch ~ 102F9Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[7:0]	7:0	F1 OP frame buffer base address 0.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[23:16]	7:0	See description of '102FA0h'.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_BASE_ADDR0_F1[26:24]	2:0	See description of '102FA0h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[7:0]	7:0	F1 OP frame buffer base address 1.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[23:16]	7:0	See description of '102FA4h'.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR1_F1[26:24]	2:0	See description of '102FA4h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MWE_OFFSET_F1[7:0]	7:0	F1 OP demo mode pixel offset (pixel unit).	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_MWE_OFFSET_F1[11:8]	3:0	See description of '102FA8h'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F1[7:0]	7:0	F1 OP frame buffer line offset (pixel unit).	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F1[12:8]	4:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F1[7:0]	7:0	F1 OP fetch pixel number of one line.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F1[11:8]	3:0	See description of '102FAEh'.	
58h ~ 58h (102FB0h ~ 102FB1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FORCE_MUTE_IPW_ENABLE_F1	5	Force IPS enable at av-mute case.	
	-	4:0	Reserved.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:2	Reserved.	
	OPM_8READ_EN_F1	1	F1 opm 8read mode enable.	
	OPM_6READ_EN_F1	0	F1 opm 6read mode enable.	
5Ah ~ 5Dh (102FB4h ~ 102FBBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[7:0]	7:0	OPW write limit address.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[23:16]	7:0	See description of '102FBCh'.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_EN	7	OPW write limit enable.	
	OPW_W_LIMIT_MIN	6	OPW write limit flag 0: maximum 1: minimum.	
	-	5:3	Reserved.	
	OPW_W_LIMIT_ADR[26:24]	2:0	See description of '102FBCh'.	
60h ~ 62h (102FC0h ~ 102FC5h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_0	4	SCM first arbiter bypass function enable.	
	SCM_ARB_SW_RST_0	3	SCM first arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_0	2	SCM first arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_0	1	SCM first arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_0	0	SCM first arbiter client 1 having higher priority than client 0.	
63h	**REG102FC7**	**7:0**	**Default : 0x08**	**Access : R/W**

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FC7h)	SCM_ARB_MAX_REQ_NUM_0[7:0]	7:0	SCM first arbiter maximum request number for each last.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY0_THD_0[7:0]	7:0	SCM first arbiter threshold number of flow control of client 0.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_0[7:0]	7:0	SCM first arbiter threshold number of flow control of client 1.	
65h ~ 65h (102FCAh ~ 102FCBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY66_13_15[2:0]	7:5		
	-	4:0	Reserved.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FD_MASK_READ_F1	5	F1 fd mask read back.	
	FD_MASK_READ_F2	4	F2 fd mask read back.	
	-	3:2	Reserved.	
	OPW_WREQ_OFF_ALL	1	All OPW write request disable.	
	OPW_WREQ_OFF_F1	0	F1 OPW write request disable.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY67_8_15[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_1	4	SCM second arbiter bypass function enable.	
	SCM_ARB_SW_RST_1	3	SCM second arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_1	2	SCM second arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_1	1	SCM second arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_1	0	SCM second arbiter client 1 having higher priority than client 0.	
68h	**REG102FD1**	**7:0**	**Default : 0x08**	**Access : R/W**

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FD1h)	SCM_ARB_MAX_REQ_NUM_1[7:0]	7:0	SCM second arbiter maximum request number for each last.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY0_THD_1[7:0]	7:0	SCM second arbiter threshold number of flow control of client 0.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_1[7:0]	7:0	SCM second arbiter threshold number of flow control of client 1.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_2	4	SCM third arbiter bypass function enable.	
	SCM_ARB_SW_RST_2	3	SCM third arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_2	2	SCM third arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_2	1	SCM third arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_2	0	SCM third arbiter client 1 having higher priority than client 0.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x0C**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM_2[7:0]	7:0	SCM third arbiter maximum request number for each last.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_RDY0_THD_2[7:0]	7:0	SCM third arbiter threshold number of flow control of client 0.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_2[7:0]	7:0	SCM third arbiter threshold number of flow control of client 1.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at real line case.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
6Dh	**REG102FDA**	**7:0**	**Default : 0x12**	**Access : R/W**

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FDAh)	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at real line case.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
70h (102FE0h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
71h ~ 73h (102FE2h ~ 102FE6h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
74h ~ 76h (102FE8h ~ 102FEDh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
78h ~ 7Ch (102FF0h ~ 102FF9h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[7:0]	7:0	F1 status read out for debug.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[15:8]	7:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7E_F1[7:0]	7:0	F1 status read out for debug.	

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SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7E_F1[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[7:0]	7:0	F1 status read out for debug.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[15:8]	7:0	See description of '102FFEh'.	

IPOL Register (Bank = 102F, Sub-bank = 13)

IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F05h)	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Ch)	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Ou.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0		
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Dh)	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F43h)	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F48h)	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F49h)	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F50h)	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Dh)	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	

T3D Register (Bank = 102F, Sub-bank = 15)

T3D Register (Bank = 102F, Sub-bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 02h	**-**	**7:0**	**Default : -**	**Access : -**

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T3D Register (Bank = 102F, Sub-bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F02h ~ 102F05h)	-	-	Reserved.	
05h ~ 27h (102F0Ah ~ 102F4Eh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
28h ~ 2Bh (102F50h ~ 102F57h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h ~ 43h (102F60h ~ 102F87h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
54h ~ 61h (102FA8h ~ 102FC2h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
62h (102FC4h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
63h ~ 6Dh (102FC6h ~ 102FDBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
70h ~ 7Fh (102FE0h ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

ACE Register (Bank = 102F, Sub-bank = 18)

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_FCC_8T_EN	7	Main window FCC region 8 enable.	

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_FCC_7T_EN	6	Main window FCC region 7 enable.	
	MAIN_FCC_6T_EN	5	Main window FCC region 6 enable.	
	MAIN_FCC_5T_EN	4	Main window FCC region 5 enable.	
	MAIN_FCC_4T_EN	3	Main window FCC region 4 enable.	
	MAIN_FCC_3T_EN	2	Main window FCC region 3 enable.	
	MAIN_FCC_2T_EN	1	Main window FCC region 2 enable.	
	MAIN_FCC_1T_EN	0	Main window FCC region 1 enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FCC_DITHER_EN	6	FCC dither bit enable.	
	FCC_RESERVED_1[4:0]	5:1	Reserved.	
	MAIN_FCC_9T_EN	0	Main window FCC window 9 enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_FCC_8T_EN	7	Sub window FCC region 8 enable.	
	SUB_FCC_7T_EN	6	Sub window FCC region 7 enable.	
	SUB_FCC_6T_EN	5	Sub window FCC region 6 enable.	
	SUB_FCC_5T_EN	4	Sub window FCC region 5 enable.	
	SUB_FCC_4T_EN	3	Sub window FCC region 4 enable.	
	SUB_FCC_3T_EN	2	Sub window FCC region 3 enable.	
	SUB_FCC_2T_EN	1	Sub window FCC region 2 enable.	
	SUB_FCC_1T_EN	0	Sub window FCC region 1 enable.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SUB_FCC_9T_EN	0	Sub window FCC region 9 enable.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T1[7:0]	7:0	FCC region 1 cb target.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T1[7:0]	7:0	FCC region 1 cr target.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T2[7:0]	7:0	FCC region 2 cb target.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T2[7:0]	7:0	FCC region 2 cr target.	
1Ah	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F34h)	FCC_CB_T3[7:0]	7:0	FCC region 3 cb target.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T3[7:0]	7:0	FCC region 3 cr target.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T4[7:0]	7:0	FCC region 4 cb target.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T4[7:0]	7:0	FCC region 4 cr target.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T5[7:0]	7:0	FCC region 5 cb target.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T5[7:0]	7:0	FCC region 5 cr target.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T6[7:0]	7:0	FCC region 6 cb target.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T6[7:0]	7:0	FCC region 6 cr target.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T7[7:0]	7:0	FCC region 7 cb target.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T7[7:0]	7:0	FCC region 7 cr target.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T8[7:0]	7:0	FCC region 8 cb target.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T8[7:0]	7:0	FCC region 8 cr target.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_2T[3:0]	7:4	FCC region 2 strength.	
	FCC_K_1T[3:0]	3:0	FCC region 1 strength.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_4T[3:0]	7:4	FCC region 4 strength.	
	FCC_K_3T[3:0]	3:0	FCC region 3 strength.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_6T[3:0]	7:4	FCC region 6 strength.	
	FCC_K_5T[3:0]	3:0	FCC region 5 strength.	
21h	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F43h)	FCC_K_8T[3:0]	7:4	FCC region 8 strength.	
	FCC_K_7T[3:0]	3:0	FCC region 7 strength.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FCC_K_9T[3:0]	3:0	FCC region 9 strength.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN1_CB_UP[1:0]	7:6	FCC region 1 target cb up distance.	
	FCC_WIN1_CB_DOWN[1:0]	5:4	FCC region 1 target cb down distance.	
	FCC_WIN1_CR_UP[1:0]	3:2	FCC region 1 target cr up distance.	
	FCC_WIN1_CR_DOWN[1:0]	1:0	FCC region 1 target cr down distance.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN2_CB_UP[1:0]	7:6	FCC region 2 target cb up distance.	
	FCC_WIN2_CB_DOWN[1:0]	5:4	FCC region 2 target cb down distance.	
	FCC_WIN2_CR_UP[1:0]	3:2	FCC region 2 target cr up distance.	
	FCC_WIN2_CR_DOWN[1:0]	1:0	FCC region 2 target cr down distance.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN3_CB_UP[1:0]	7:6	FCC region 3 target cb up distance.	
	FCC_WIN3_CB_DOWN[1:0]	5:4	FCC region 3 target cb down distance.	
	FCC_WIN3_CR_UP[1:0]	3:2	FCC region 3 target cr up distance.	
	FCC_WIN3_CR_DOWN[1:0]	1:0	FCC region 3 target cr down distance.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN4_CB_UP[1:0]	7:6	FCC region 4 target cb up distance.	
	FCC_WIN4_CB_DOWN[1:0]	5:4	FCC region 4 target cb down distance.	
	FCC_WIN4_CR_UP[1:0]	3:2	FCC region 4 target cr up distance.	
	FCC_WIN4_CR_DOWN[1:0]	1:0	FCC region 4 target cr down distance.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN5_CB_UP[1:0]	7:6	FCC region 5 target cb up distance.	
	FCC_WIN5_CB_DOWN[1:0]	5:4	FCC region 5 target cb down distance.	
	FCC_WIN5_CR_UP[1:0]	3:2	FCC region 5 target cr up distance.	
	FCC_WIN5_CR_DOWN[1:0]	1:0	FCC region 5 target cr down distance.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN6_CB_UP[1:0]	7:6	FCC region 6 target cb up distance.	
	FCC_WIN6_CB_DOWN[1:0]	5:4	FCC region 6 target cb down distance.	

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_WIN6_CR_UP[1:0]	3:2	FCC region 6 target cr up distance.	
	FCC_WIN6_CR_DOWN[1:0]	1:0	FCC region 6 target cr down distance.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN7_CB_UP[1:0]	7:6	FCC region 7 target cb up distance.	
	FCC_WIN7_CB_DOWN[1:0]	5:4	FCC region 7 target cb down distance.	
	FCC_WIN7_CR_UP[1:0]	3:2	FCC region 7 target cr up distance.	
	FCC_WIN7_CR_DOWN[1:0]	1:0	FCC region 7 target cr down distance.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN8_CB_UP[1:0]	7:6	FCC region 8 target cb up distance.	
	FCC_WIN8_CB_DOWN[1:0]	5:4	FCC region 8 target cb down distance.	
	FCC_WIN8_CR_UP[1:0]	3:2	FCC region 8 target cr up distance.	
	FCC_WIN8_CR_DOWN[1:0]	1:0	FCC region 8 target cr down distance.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FCC_WIN9_CB[2:0]	5:3	FCC region 9 target cb distance.	
	FCC_WIN9_CR[2:0]	2:0	FCC region 9 target cr distance.	
28h (102F51h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:3	Reserved.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	-	1:0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_R[3:0]	7:4	Sub window ICC saturation adjustment of R.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_G[3:0]	7:4	Sub window ICC saturation adjustment of G.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_B[3:0]	7:4	Sub window ICC saturation adjustment of B.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_C[3:0]	7:4	Sub window ICC saturation adjustment of C.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_M[3:0]	7:4	Sub window ICC saturation adjustment of M.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_Y[3:0]	7:4	Sub window ICC saturation adjustment of Y.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_F[3:0]	7:4	Sub window ICC saturation adjustment of F.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation, [0]: Other_color. [1]: Red. [2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation, [0]: Other_color. [1]: Red. [2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Dh)	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_SA_USER_NC[3:0]	7:4	Sub window ICC saturation adjustment of Other color.	
	-	3:0	Reserved.	
38h (102F70h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
39h ~ 3Bh (102F72h ~ 102F77h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	White peak limit threshold.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	
	SUB_IBC_EN	6	Sub window IBC enable.	
	-	5:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h	**REG102F87**	**7:0**	**Default : 0x20**	**Access : R/W**

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F87h)	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YR_ADJ[5:0]	5:0	Sub window IBC Y adjustment of R.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YG_ADJ[5:0]	5:0	Sub window IBC Y adjustment of G.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YB_ADJ[5:0]	5:0	Sub window IBC Y adjustment of B.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YC_ADJ[5:0]	5:0	Sub window IBC Y adjustment of C.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YM_ADJ[5:0]	5:0	Sub window IBC Y adjustment of M.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YY_ADJ[5:0]	5:0	Sub window IBC Y adjustment of Y.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YF_ADJ[5:0]	5:0	Sub window IBC Y adjustment of F.	
48h (102F91h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_HIGH_PASS_EN	7	Main window Y H_coring as high pass filter.	
	MAIN_Y_TABLE_STEP[2:0]	6:4	Main window Y H_coring LUT step.	
	MAIN_PC_MODE	3	Main window PC mode.	
	-	2	Reserved.	

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_BAND2_H_CORING_EN	1	Main window Y band2 H_coring enable.	
	MAIN_Y_BAND1_H_CORING_EN	0	Main window Y band1 H_coring enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_HIGH_PASS_EN	7	Main window C H_coring as high pass filter.	
	MAIN_C_TABLE_STEP[2:0]	6:4	Main window C H_coring LUT step.	
	MAIN_WHITE_PEAK_LIMIT_EN	3	Main window white peak limit enable.	
	-	2	Reserved.	
	MAIN_C_BAND2_H_CORING_EN	1	Main window C band2 H_coring enable.	
	MAIN_C_BAND1_H_CORING_EN	0	Main window C band1 H_coring enable.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE1[7:0]	7:0	Main window Y gain table 1.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE2[7:0]	7:0	Main window Y gain table 2.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE3[7:0]	7:0	Main window Y gain table 3.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE4[7:0]	7:0	Main window Y gain table 4.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE1[7:0]	7:0	Main window C gain table 1.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE2[7:0]	7:0	Main window C gain table 2.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE3[7:0]	7:0	Main window C gain table 3.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE4[7:0]	7:0	Main window C gain table 4.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_NOISE_MASKING_EN	7	Main window horizontal Y NMR enable.	
	MAIN_Y_COLOR_NOISE_MASKING_EN	6	Main window horizontal Y NMR color adaptive enable.	
	MAIN_Y_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal Y NMR gain (xxxx.xx).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_Y_NM_MIN_THRD[3:0]	7:4	Main window Y mosquito noise removemin value threshold.	

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_NM_MAX_THRD[3:0]	3:0	Main window Y mosquito noise remove max value threshold.	
57h (102FAEh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_COLOR_NM_STEP[1:0]	1:0	Sub window color noise_masking step.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_TABLE_STEP[2:0]	6:4	Sub window Y H_coring LUT step.	
	-	3:0	Reserved.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_C_TABLE_STEP[2:0]	6:4	Sub window C H_coring LUT step.	
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.	
	-	2:0	Reserved.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE1[7:0]	7:0	Sub window Y gain table 1.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE2[7:0]	7:0	Sub window Y gain table 2.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE3[7:0]	7:0	Sub window Y gain table 3.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE4[7:0]	7:0	Sub window Y gain table 4.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE1[7:0]	7:0	Sub window C gain table 1.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE2[7:0]	7:0	Sub window C gain table 2.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE3[7:0]	7:0	Sub window C gain table 3.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE4[7:0]	7:0	Sub window C gain table 4.	
5Dh	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FBAh)	SUB_Y_NOISE_MASKING_EN	7	Sub window horizontal Y NMR enable.	
	SUB_Y_COLOR_NOISE_MASKING_EN	6	Sub window horizontal Y NMR color adaptive enable.	
	SUB_Y_NOISE_MASK_GAIN[5:0]	5:0	Sub window horizontal Y noise-masking gain (xxxx.xx).	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SUB_Y_NM_MIN_THRD[3:0]	7:4	Sub window Y noise_masking min value threshold.	
	SUB_Y_NM_MAX_THRD[3:0]	3:0	Sub window Y noise_masking max value threshold.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_DITHER_EN	6	Sub window horizontal Y NMR dither enable.	
	-	5	Reserved.	
	MAIN_Y_DITHER_EN	4	Main window horizontal Y NMR dither enable.	
	-	3:0	Reserved.	
5Fh (102FBFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:0	Reserved.	
60h (102FC1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_R[6:0]	6:0	Sub window IHC hue adjustment of R.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_G[6:0]	6:0	Sub window IHC hue adjustment of G.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_B[6:0]	6:0	Sub window IHC hue adjustment of B.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_C[6:0]	6:0	Sub window IHC hue adjustment of C.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_M[6:0]	6:0	Sub window IHC hue adjustment of M.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_Y[6:0]	6:0	Sub window IHC hue adjustment of Y.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_F[6:0]	6:0	Sub window IHC hue adjustment of F.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	

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ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	
6Eh (102FDDh)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	SUB_R2Y_EQ_SEL[2:0]	6:4	Sub window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	
	-	3	Reserved.	
	MAIN_R2Y_EQ_SEL[2:0]	2:0	Main window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	

PEAKING Register (Bank = 102F, Sub-bank = 19)

PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	

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PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.	
	-	3:1	Reserved.	
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND4_COEF_STEP[1:0]	7:6	Sub window band4 coefficient step.	
	SUB_BAND3_COEF_STEP[1:0]	5:4	Sub window band3 coefficient step.	
	SUB_BAND2_COEF_STEP[1:0]	3:2	Sub window band2 coefficient step.	
	SUB_BAND1_COEF_STEP[1:0]	1:0	Sub window band1 coefficient step.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.	
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.	

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PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_OVERSHOOT_LIMIT[7:0]	7:0	Main window band1 overshoot limit.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_OVERSHOOT_LIMIT[7:0]	7:0	Main window band2 overshoot limit.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_OVERSHOOT_LIMIT[7:0]	7:0	Main window band3 overshoot limit.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_OVERSHOOT_LIMIT[7:0]	7:0	Main window band4 overshoot limit.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band1 undershoot limit.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band2 undershoot limit.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band3 undershoot limit.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band4 undershoot limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_PEAKING_EN	7	Main window color adaptive peaking enable.	
	MAIN_COLOR_FACTOR_LPF_EN	6	Main window color factor LPF enable.	
	-	5:0	Reserved.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	-	3:2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
31h ~ 32h (102F62h ~ 102F64h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
37h ~ 37h (102F6Eh ~ 102F6Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CR_DELAY_NUM	6	Sub window cr delay number. #0: no delay. #1: delay 1T.	
	-	5	Reserved.	

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PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_CR_DELAY_NUM	4	Main window cr delay number. #0: no delay. #1: delay 1T.	
	-	3:2	Reserved.	
	SUB_YC_DELAY_EN	1	Sub window yc delay enable.	
	MAIN_YC_DELAY_EN	0	Main window yc delay enable.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CB_DELAY_NUM	6	Sub window cb delay number. #0: no delay. #1: delay 1T.	
	-	5	Reserved.	
	SUB_Y_DELAY_NUM	4	Sub window y delay number. #0: no delay. #1: delay 1T.	
	-	3	Reserved.	
	MAIN_CB_DELAY_NUM	2	Main window cb delay number. #0: no delay. #1: delay 1T.	
	-	1	Reserved.	
	MAIN_Y_DELAY_NUM	0	Main window y delay number. #0: no delay. #1: delay 1T.	
40h ~ 47h (102F80h ~ 102F8Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_COLOR_PK_WIN4_EN	7	Sub window color adaptive win4 enable.	
	SUB_COLOR_PK_WIN3_EN	6	Sub window color adaptive win3 enable.	
	SUB_COLOR_PK_WIN2_EN	5	Sub window color adaptive win2 enable.	
	SUB_COLOR_PK_WIN1_EN	4	Sub window color adaptive win1 enable.	
	MAIN_COLOR_PK_WIN4_EN	3	Main window color adaptive win4 enable.	
	MAIN_COLOR_PK_WIN3_EN	2	Main window color adaptive win3 enable.	
	MAIN_COLOR_PK_WIN2_EN	1	Main window color adaptive win2 enable.	

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PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_COLOR_PK_WIN1_EN	0	Main window color adaptive win1 enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_TRANSITION_STEP[1:0]	7:6	Color adaptive win4 transition step.	
	COLOR_PK_WIN3_TRANSITION_STEP[1:0]	5:4	Color adaptive win3 transition step.	
	COLOR_PK_WIN2_TRANSITION_STEP[1:0]	3:2	Color adaptive win2 transition step.	
	COLOR_PK_WIN1_TRANSITION_STEP[1:0]	1:0	Color adaptive win1 transition step.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_ENTRY_VALUE[3:0]	7:4	Color adaptive win2 strength.	
	COLOR_PK_WIN1_ENTRY_VALUE[3:0]	3:0	Color adaptive win1 strength.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_ENTRY_VALUE[3:0]	7:4	Color adaptive win4 strength.	
	COLOR_PK_WIN3_ENTRY_VALUE[3:0]	3:0	Color adaptive win3 strength.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	COLOR_PK_TEST_EN[3:0]	3:0	Color adaptive test mode enable.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_PK_ADP_Y_STEP[1:0]	5:4	Main window peaking adaptive y alpha step.	
	-	3:2	Reserved.	
	MAIN_PK_ADP_Y_ALPHA_LPF_EN	1	Main window peaking adaptive y alpha low pass filter enable.	
	MAIN_PK_ADP_Y_EN	0	Main window peaking adaptive y enable.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PK_Y_LOW_THRD[7:0]	7:0	Main window peaking adaptive y low threshold.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_1[3:0]	7:4	Main window peaking adaptive y alpha LUT 1.	
	MAIN_PK_ADP_Y_ALPHA_LUT_0[3:0]	3:0	Main window peaking adaptive y alpha LUT 0, format is x.xxx, range is 0~F.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x76**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_3[3:0]	7:4	Main window peaking adaptive y alpha LUT 3.	
	MAIN_PK_ADP_Y_ALPHA_LUT_2[3:0]	3:0	Main window peaking adaptive y alpha LUT 2.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_5[3:0]	7:4	Main window peaking adaptive y alpha LUT 5.	

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PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_PK_ADP_Y_ALPHA_LUT_4[3:0]	3:0	Main window peaking adaptive y alpha LUT 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_7[3:0]	7:4	Main window peaking adaptive y alpha LUT 7.	
	MAIN_PK_ADP_Y_ALPHA_LUT_6[3:0]	3:0	Main window peaking adaptive y alpha LUT 6.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_UP[7:0]	7:0	Color adaptive win1 cb up.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CR_UP[7:0]	7:0	Color adaptive win1 cr up.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_DOWN[7:0]	7:0	Color adaptive win1 cb down.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CR_DOWN[7:0]	7:0	Color adaptive win1 cr down.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CB_UP[7:0]	7:0	Color adaptive win2 cb up.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CR_UP[7:0]	7:0	Color adaptive win2 cr up.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CB_DOWN[7:0]	7:0	Color adaptive win2 cb down.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CR_DOWN[7:0]	7:0	Color adaptive win2 cr down.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CB_UP[7:0]	7:0	Color adaptive win3 cb up.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CR_UP[7:0]	7:0	Color adaptive win3 cr up.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CB_DOWN[7:0]	7:0	Color adaptive win3 cb down.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CR_DOWN[7:0]	7:0	Color adaptive win3 cr down.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_CB_UP[7:0]	7:0	Color adaptive win4 cb up.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_CR_UP[7:0]	7:0	Color adaptive win4 cr up.	
5Fh	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**

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PEAKING Register (Bank = 102F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FBEh)	COLOR_PK_WIN4_CB_DOWN[7:0]	7:0	Color adaptive win4 cb down.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_CR_DOWN[7:0]	7:0	Color adaptive win4 cr down.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_PK_ADP_Y_STEP[1:0]	5:4	Sub window peaking adaptive y alpha step.	
	-	3:2	Reserved.	
	SUB_PK_ADP_Y_ALPHA_LPF_EN	1	Sub window peaking adaptive y alpha low pass filter enable.	
	SUB_PK_ADP_Y_EN	0	Sub window peaking adaptive y enable.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PK_Y_LOW_THRD[7:0]	7:0	Sub window peaking adaptive y low threshold.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x54**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_1[3:0]	7:4	Sub window peaking adaptive y alpha LUT 1.	
	SUB_PK_ADP_Y_ALPHA_LUT_0[3:0]	3:0	Sub window peaking adaptive y alpha LUT 0.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x76**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_3[3:0]	7:4	Sub window peaking adaptive y alpha LUT 3.	
	SUB_PK_ADP_Y_ALPHA_LUT_2[3:0]	3:0	Sub window peaking adaptive y alpha LUT 2.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_5[3:0]	7:4	Sub window peaking adaptive y alpha LUT 5.	
	SUB_PK_ADP_Y_ALPHA_LUT_4[3:0]	3:0	Sub window peaking adaptive y alpha LUT 4.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_7[3:0]	7:4	Sub window peaking adaptive y alpha LUT 7.	
	SUB_PK_ADP_Y_ALPHA_LUT_6[3:0]	3:0	Sub window peaking adaptive y alpha LUT 6.	

DLC Register (Bank = 102F, Sub-bank = 1A)

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 01h (102F02h ~ 102F03h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PRE_Y_GAIN_LSB[3:0]	7:4	Main window pre Y gain LSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
	MAIN_Y_GAIN_LSB[3:0]	3:0	Main window Y gain LSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PRE_Y_GAIN_LSB[3:0]	7:4	Sub window pre Y gain LSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
	SUB_Y_GAIN_LSB[3:0]	3:0	Sub window Y gain LSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
03h ~ 04h (102F06h ~ 102F09h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
06h ~ 08h (102F0Ch ~ 102F10h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	UVC_DITHER_EN	7	UV compensate dither enable.	
	-	6	Reserved.	
	SUB_UVC_LOCATE	5	Sub window UV compensate reference location. //0: after ble/wle. //1: after curve fit.	
	SUB_UVC_EN	4	Sub window UV compensate enable.	
	-	3:2	Reserved.	
	MAIN_UVC_LOCATE	1	Main window UV compensate reference location. //0: after ble/wle. //1: after curve fit0.	
	MAIN_UVC_EN	0	Main window UV compensate enable.	
09h ~ 0Ah (102F12h ~ 102F15h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximun pixel.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximun pixel.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimun pixel.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	MAIN_Y_GAIN[6:0]	6:0	Main window Y gain MSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_GAIN[6:0]	6:0	Sub window Y gain MSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PRE_Y_GAIN[6:0]	6:0	Main window pre- Y gain MSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	SUB_PRE_Y_GAIN[6:0]	6:0	Sub window pre- Y gain MSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_POST_BRI_ADJUST_LSB[1:0]	1:0	Main window post Y adjust low bit (2's complement).	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_POST_BRI_ADJUST_LSB[1:0]	1:0	Sub window post Y adjust low bit (2's complement).	
18h	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F30h)	MAIN_POST_BRI_ADJUST[7:0]	7:0	Main window post Y adjust.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_POST_BRI_ADJUST[7:0]	7:0	Sub window post Y adjust.	
1Ah ~ 1Bh (102F34h ~ 102F37h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h ~ 27h (102F40h ~ 102F4Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x18**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x28**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x38**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x48**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x58**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x68**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x78**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x98**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0xA8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Bh)	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0xC8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0xE8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x08**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_0[7:0]	7:0	Sub window curve table 0.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x18**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_1[7:0]	7:0	Sub window curve table 1.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x28**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_2[7:0]	7:0	Sub window curve table 2.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x38**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_3[7:0]	7:0	Sub window curve table 3.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x48**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_4[7:0]	7:0	Sub window curve table 4.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x58**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_5[7:0]	7:0	Sub window curve table 5.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x68**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_6[7:0]	7:0	Sub window curve table 6.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x78**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_7[7:0]	7:0	Sub window curve table 7.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_8[7:0]	7:0	Sub window curve table 8.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x98**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_9[7:0]	7:0	Sub window curve table 9.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0xA8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_10[7:0]	7:0	Sub window curve table 10.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_11[7:0]	7:0	Sub window curve table 11.	

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0xC8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_12[7:0]	7:0	Sub window curve table 12.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_13[7:0]	7:0	Sub window curve table 13.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0xE8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_14[7:0]	7:0	Sub window curve table 14.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_15[7:0]	7:0	Sub window curve table 15.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[15:8]	7:0	See description of '102F8Ah'.	
46h	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F8Ch)	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[15:8]	7:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[15:8]	7:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[15:8]	7:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	
56h	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FADh)	TOTAL_32_22[15:8]	7:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[15:8]	7:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[15:8]	7:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[15:8]	7:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[15:8]	7:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[15:8]	7:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[15:8]	7:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[15:8]	7:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[15:8]	7:0	See description of '102FBCh'.	

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[15:8]	7:0	See description of '102FBEh'.	
63h ~ 63h (102FC6h ~ 102FC7h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x60**	**Access : R/W**
	MAIN_UVC_GAIN_HIGH_LIMIT[7:0]	7:0	Main window UV compensate gain up limit (format is 4.8).	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_HIGH_LIMIT[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAIN_UVC_GAIN_LOW_LIMIT[7:0]	7:0	Main window UV compensate gain down limit (format is 4.8).	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_LOW_LIMIT[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x60**	**Access : R/W**
	SUB_UVC_GAIN_HIGH_LIMIT[7:0]	7:0	Sub window UV compensate gain up limit (format is 4.8).	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_UVC_GAIN_HIGH_LIMIT[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SUB_UVC_GAIN_LOW_LIMIT[7:0]	7:0	Sub window UV compensate gain down limit (format is 4.8).	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_UVC_GAIN_LOW_LIMIT[11:8]	3:0	See description of '102FCEh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point.	

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DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '102FEEh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x08**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_N0[7:0]	7:0	Sub window curve table left point, MSB is sign bit.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SUB_CURVE_FIT_TABLE_N0[8]	0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x08**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_16[7:0]	7:0	Sub window curve table 16.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SUB_CURVE_FIT_TABLE_16[8]	0	See description of '102FFEh'.	

D3D Register (Bank = 102F, Sub-bank = 1D)

D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_0[7:0]	7:0		
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_0[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_1[7:0]	7:0		
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_1[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_2[7:0]	7:0		

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_3[7:0]	7:0		
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_3[15:8]	7:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_4[7:0]	7:0		
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_4[15:8]	7:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_5[7:0]	7:0		
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_5[15:8]	7:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_6[7:0]	7:0		
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_6[15:8]	7:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_7[7:0]	7:0		
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_7[15:8]	7:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_8[7:0]	7:0		
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_8[15:8]	7:0	See description of '102F30h'.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_9[7:0]	7:0		
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_9[15:8]	7:0	See description of '102F32h'.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_10[7:0]	7:0		
1Ah	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F35h)	LEFT_TOP_LEVEL_10[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_11[7:0]	7:0		
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_11[15:8]	7:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_12[7:0]	7:0		
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_12[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_13[7:0]	7:0		
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_13[15:8]	7:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_14[7:0]	7:0		
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_14[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_15[7:0]	7:0		
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_15[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_16[7:0]	7:0		
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_16[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_17[7:0]	7:0		
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_17[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_18[7:0]	7:0		
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_18[15:8]	7:0	See description of '102F44h'.	

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_19[7:0]	7:0		
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_19[15:8]	7:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_20[7:0]	7:0		
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_20[15:8]	7:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_21[7:0]	7:0		
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_21[15:8]	7:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_22[7:0]	7:0		
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_22[15:8]	7:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_23[7:0]	7:0		
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_23[15:8]	7:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_24[7:0]	7:0		
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_24[15:8]	7:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_25[7:0]	7:0		
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_25[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_26[7:0]	7:0		
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_26[15:8]	7:0	See description of '102F54h'.	
2Bh	**REG102F56**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F56h)	LEFT_TOP_LEVEL_27[7:0]	7:0		
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_27[15:8]	7:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_28[7:0]	7:0		
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_28[15:8]	7:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_29[7:0]	7:0		
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_29[15:8]	7:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_30[7:0]	7:0		
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_30[15:8]	7:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_31[7:0]	7:0		
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_31[15:8]	7:0	See description of '102F5Eh'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_0[7:0]	7:0		
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_0[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_1[7:0]	7:0		
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_1[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_2[7:0]	7:0		
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_2[15:8]	7:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_3[7:0]	7:0		

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_3[15:8]	7:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_4[7:0]	7:0		
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_4[15:8]	7:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_5[7:0]	7:0		
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_5[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_6[7:0]	7:0		
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_6[15:8]	7:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_7[7:0]	7:0		
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_7[15:8]	7:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_8[7:0]	7:0		
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_8[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_9[7:0]	7:0		
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_9[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_10[7:0]	7:0		
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_10[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_11[7:0]	7:0		
3Bh	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F77h)	RIGHT_BOTTOM_LEVEL_11[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_12[7:0]	7:0		
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_12[15:8]	7:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_13[7:0]	7:0		
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_13[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_14[7:0]	7:0		
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_14[15:8]	7:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_15[7:0]	7:0		
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_15[15:8]	7:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_16[7:0]	7:0		
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_16[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_17[7:0]	7:0		
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_17[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_18[7:0]	7:0		
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_18[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_19[7:0]	7:0		
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_19[15:8]	7:0	See description of '102F86h'.	

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_20[7:0]	7:0		
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_20[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_21[7:0]	7:0		
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_21[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_22[7:0]	7:0		
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_22[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_23[7:0]	7:0		
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_23[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_24[7:0]	7:0		
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_24[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_25[7:0]	7:0		
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_25[15:8]	7:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_26[7:0]	7:0		
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_26[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_27[7:0]	7:0		
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_27[15:8]	7:0	See description of '102F96h'.	
4Ch	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F98h)	RIGHT_BOTTOM_LEVEL_28[7:0]	7:0		
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_28[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_29[7:0]	7:0		
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_29[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_30[7:0]	7:0		
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_30[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_31[7:0]	7:0		
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_31[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RESULT_READY	7		
	-	6:3	Reserved.	
	VSYNC_LOW_ACT	2	0: Vsync pulse is high active 1: vsync pulse is low active.	
	DETECT_MODE	1	0: Side-by-side detection 1: top-bottom detection.	
	TRIGGER_START_WPULSE	0	Trigger start write pulse when 1 for side-by-side or top-bottom detection.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	THRESHOLD[7:0]	7:0	THRESHOLD value of 3D checkboard detection.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	WINDOW_SIZE[1:0]	1:0	3D checkborad detection window size: 2'b00: window size = 5, 2'b01: window size = 7, 2'b10: WINDOW_SIZE = 9, 2'b11: WINDOW_SIZE = 11 (default).	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	CKBOARD_RES[7:0]	7:0		
53h	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, Sub-bank = 1D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FA7h)	CKBOARD_RES[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOUNDARY_H_TB[7:0]	7:0	Horizontal value of boundary for not detection in top-bottom mode.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOUNDARY_V_TB[7:0]	7:0	Vertical value of boundary for not detection in top-bottom mode.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOUNDARY_H_SBYS[7:0]	7:0	Horizontal value of boundary for not detection in side-by-side mode.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOUNDARY_V_SBYS[7:0]	7:0	Vertical value of boundary for not detection in side-by-side mode.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[7:0]	7:0	The number of menuload data (0: disable menuload).	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_REQ_LEN[7:0]	7:0	Length of menuload DMA's request (0: disable menuload).	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_EN	7	Menuload enable (SC0).	
	-	6:3	Reserved.	
	MLOAD_REQ_LEN[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[7:0]	7:0	Base address of allocated memory for menuload.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[15:8]	7:0	See description of '102F06h'.	
04h	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**

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DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F08h)	MLOAD_BASE_ADR[23:16]	7:0	See description of '102F06h'.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MLOAD_BASE_ADR[26:24]	2:0	See description of '102F06h'.	
08h ~ 0Bh (102F10h ~ 102F17h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_REQ_LEN[3:0]	7:4	Length of dynamic scaling DMA's request (0: disable dynamic scaling).	
	DS_REQ_TH[3:0]	3:0	Threshold for one dynamic scaling DMA request.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_IPM2MI_SEL	7	Main IP dynamic scaling miu selection.	
	DS_IPS2MI_SEL	6	Sub IP dynamic scaling miu selection.	
	DS_OP2MI_SEL	5	OP dynamic scaling miu selection.	
	DS_RIU_WE	4	Enable write register through RIU.	
	IPM_DS_EN	3	Enable main IP2 dynamic scaling.	
	IPS_DS_EN	2	Enable sub IP2 dynamic scaling.	
	OP_DS_EN	1	Enable OP dynamic scaling.	
	DS_REQ_PRI	0	User specified priority of MIU.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[7:0]	7:0	Base address of allocated memory for dynamic scaling.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[23:16]	7:0	See description of '102F22h'.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DS_BASE_ADR[26:24]	2:0	See description of '102F22h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_IDX_DEPTH[7:0]	7:0	The number of dynamic scaling data per index (0: disable dynamic scaling).	
13h	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**

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DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F27h)	-	7:2	Reserved.	
	SC_INDEX_F2_SEL	1	F2 dynamic scaling index select. 0: From main. 1: From sub.	
	SC_INDEX_F1_SEL	0	F1 dynamic scaling index select. 0: From main. 1: From sub.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DS_OP_IDX_SEL	4	Dyn_scl idx selection for OP (SC0). (only active when reg_new_idx_mode_en = 1). 0: F2(main). 1: F1(sub).	
	NEW_IDX_MODE_EN	3	Enable new MIU idx mode. 0: OP-SC1, IP, OP. 1: IPS, OP-SC1, IPM, OP.	
	-	2:0	Reserved.	
15h ~ 16h (102F2Ah ~ 102F2Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	DS_MREQ_ALWAYS_ACTIVE	2	Set mreq_dyn_scl always active.	
	DS_RIU_BE[1:0]	1:0	Byte enable for DS RIU interface.	
18h ~ 1Bh (102F30h ~ 102F37h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h	**REG102F20**	**7:0**	**Default : 0x01**	**Access : R/W**

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F20h)	PIP_DISABLE	7	Disable PIP Function.	
	-	6	Reserved.	
	SC2LB_EN	5	Enable HD side by side line buffer mode.	
	-	4:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the scree.	
	MAIN_EN	0	Enable main window shown on the scree.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	
	FBL_SEL	4	Select FBL source. #b0: Source F2 is FBL. #b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x70**	**Access : R/W**
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x07**	**Access : R/W**
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the extra_y to half.	
	-	4:3	Reserved.	

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. #h0: 16 pixel. #h1: 32 pixel. #h2: 64 pixel. #h3: 128 pixel. #h4: (overlap length) / 8. #h5: (overlap length) / 4. #h6: (overlap length) / 2. #h7: (overlap length).	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F1[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F2[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F1[11:8]	3:0	See description of '102F2Ch'.	
17h	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Eh)	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.	
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x02**	**Access : R/W**
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).	
	EXTRA_FETCH_LINE[3:0]	3:0	How many line will be fetched by extra request. Minimum is 1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_F2_EN	1	Force F1 use F2's register setting.	
	ATP_EN	0	Manual tune parameter.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xB8**	**Access : R/W**
	SEL_DS	7	Select the source to trigger dynamic scaling. h0: Falling edge of Vsync. h1: Delay line set by REG_DS_TRIG_DLY.	
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. #0: vsync of SC_TOP. #1: delay one line of vfde.	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. #h0: down_eq7. #h1: down_eq8. #h2: down_eq9. #h3: delay lines set by reg_disp_trig_dly.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. #h0: Falling edge of vsync. #h1: Nearly raising edge of vsync. #h2: delay line set by reg_atp_trig_dly. #h3: Manual trig by set reg_atp_en.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. #h0: Falling edge of vfde. #h1: Raising edge of vsync. #h2: Reserved. #h3: Reserved.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEL_MLOAD[1:0]	5:4	Select the source to trigger menuload. h0: Falling edge of VFDE. h1: Rising edge of VSync. h2: Falling edge of VSync. h3: Delay line set by REG_MLOAD_TRIG_DLY.	
	-	3:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x03**	**Access : R/W**
	ATP_TRIG_DLY[7:0]	7:0	Generate train_trig_p from delayed line of vsync.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x05**	**Access : R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate disp_trig_p from delayed line of vsync.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. Extra_eq will be disabled when overlapped length less then this threshold.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra request.	
1Fh	**REG102F3E**	**7:0**	**Default : 0xC2**	**Access : R/W**

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Eh)	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. #h0: 2 pixel. #h1: 4 pixel. #h2: 8 pixel. #h3: 16 pixel.	
	DISP_START_MODE	5	Select the display line buffer start mode. #0: start at advance 1 display line. #1: start at faling edge of vsync_init.	
	DISP_LB_MODE	4	Select the trig mode. #0: Line base. #1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. #h0: before 8 pixel. #h1: before 16 pixel. #h2: before 32 pixel. #h3: before 64 pixel.	
	DISP_RLN_MODE[1:0]	1:0	Select the under_run value of display level. #h0: update by hsync (not optimum performance). #h1: update when session done(may error). #h2: update when line done(reg_disp_trig_mode = 1'b0). #h3: Reserved.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_UNDER_MODE	3	Select the under_run value of display level. #0: 16'h0000. #1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of op1_disp.	
	DISP_LB_WEZ	1	Disable wen of display line buffer.	
	DISP_TRIG_MODE	0	Select the trig mode. #0: Trigged by self_counter. #1: Trigged by op2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x07**	**Access : R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x01**	**Access : R/W**
	DS_TRIG_DLY[7:0]	7:0	Generate DS_TRIG_P from delayed line of Vsync.	

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	DS_TRIG_DLY[11:8]	3:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x01**	**Access : R/W**
	MLOAD_TRIG_DLY[7:0]	7:0	Generate MLOAD_TRIG_P from delayed line of Vsync.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MLOAD_TRIG_DLY[11:8]	3:0	See description of '102F44h'.	
24h (102F48h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:3	Reserved.	
	FLAG_BB_ADR_INI	2	Status of cnt_bb_adr_ini, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	FLAG_BO_END_LN	1	Status of line_base_bot, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	-	0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BO_END_LN[7:0]	7:0	Software mode to set the line_base_bot for extra request.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	SW_BO_END_LN[11:8]	3:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the cnt_bb_adr_ini.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	SW_BB_ADR_INI[11:8]	3:0	See description of '102F64h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.	

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line cnt of first display position.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line cnt of minimum display level occure.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '102F88h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_LEN[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_LEN[11:8]	3:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_LEN[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1A[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.	

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1B[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_LENGTH_RD[7:0]	7:0	Read bo_length.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '102FBEh'.	

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_LEN[11:8]	3:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	
66h	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : RO**

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OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FCDh)	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '102FCEh'.	

ELA Register (Bank = 102F, Sub-bank = 21)

ELA Register (Bank = 102F, Sub-bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 02h (102F02h ~ 102F04h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ch ~ 0Fh (102F18h ~ 102F1Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	
11h ~ 12h (102F22h ~ 102F24h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
13h (102F26h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
14h (102F28h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
15h ~ 17h	**-**	**7:0**	**Default : -**	**Access : -**

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ELA Register (Bank = 102F, Sub-bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Ah ~ 102F2Eh)	-	-	Reserved.	
30h ~ 31h	**-**	**7:0**	**Default : -**	**Access : -**
(102F60h ~ 102F63h)	-	-	Reserved.	
70h ~ 71h	**-**	**7:0**	**Default : -**	**Access : -**
(102FE0h ~ 102FE2h)	-	-	Reserved.	
72h ~ 72h	**-**	**7:0**	**Default : -**	**Access : -**
(102FE4h ~ 102FE5h)	-	-	Reserved.	
7Fh ~ 7Fh	**-**	**7:0**	**Default : -**	**Access : -**
(102FFEh ~ 102FFFh)	-	-	Reserved.	

MADI Register (Bank = 102F, Sub-bank = 22)

MADI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x80**	**Access : R/W**
	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. #0: disable C ratio filter. #1: enable C ratio filter.	

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MADI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RATIO_C_LOWBOUND_F2	6	Main window C ratio lower bound enable.	
	RSV_02_2_F2[1:0]	5:4	Reserved.	
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. #0: Enable. #1: Disable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x86**	**Access : R/W**
	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	HIS_RATIO_OFFSET_F2[3:0]	3:0	Main Window history ratio offset.	
0Ch	**REG102F18**	**7:0**	**Default : 0x07**	**Access : R/W**

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MADI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F18h)	RSV_STAT_0_F2[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F2	5	Main window ratio statistics: ratio incremental mode.	
	STAT_SEL_C_F2	4	Main window ratio statistics: ratio selection.	
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: coring threshold.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: motion status.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[23:16]	7:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.	
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.	
	-	5	Reserved.	
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F2[3:0]	3:0	Main window DFK manual weighting.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.	

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MADI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	SST_EN_F2	7	Main window SST enable.	
	-	6:0	Reserved.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.	
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.	
	-	5:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x22**	**Access : R/W**
	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.	
20h ~ 25h (102F40h ~ 102F4Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F1	7	Sub window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F1[2:0]	2:0	Sub window ratio divide mode when Y/C separate.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F1[2:0]	5:3	Sub window ratio divide mode.	
	RATIO_MD_F1[2:0]	2:0	Sub window ratio filter mode.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x80**	**Access : R/W**
	RATIO_C_INDEP_F1	7	Sub window C ratio independent mode. #0: disable C ratio filter. #1: enable C ratio filter.	
	RATIO_C_LOWBOUND_F1	6	Sub window C ratio lower bound enable.	
	-	5:4	Reserved.	
	RATIO_C_MIN_F1[3:0]	3:0	Sub window C minimum ratio in independent mode.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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MADI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RATIO_C_YMAX_DIS_F1	0	Sub window C ratio takes Y ratio mode disable. #0: Enable. #1: Disable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:6	Reserved.	
	PRE_MOT_OFFSET_F1[5:0]	5:0	Sub Window pre-memory motion offset for motion calculation.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_MOT_GAIN_F1[3:0]	3:0	Sub Window pre-memory motion gain for motion calculation.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F1[5:0]	5:0	Sub Window post-memory motion offset for motion calculation.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F1[3:0]	7:4	Sub Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F1[3:0]	3:0	Sub Window post-memory motion gain for C motion calculation.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x86**	**Access : R/W**
	POST_MOT_YMAX_EN_F1	7	Sub Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F1[2:0]	2:0	Sub Window history weighting.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	HIS_RATIO_OFFSET_F1[3:0]	3:0	Sub Window history ratio offset.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F1	7	Sub window adaptive DFK enable.	
	WEGT_MED_EN_F1	6	Sub window weighted DFK enable.	
	-	5	Reserved.	
	MED_MANUAL_EN_F1	4	Sub window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F1[3:0]	3:0	Sub window DFK manual weighting.	

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MADI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F1[4:0]	4:0	Sub window weighted DFK low-frequency begin.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F1[3:0]	3:0	Sub window weighted DFK low-frequency slope adjustment.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F1[4:0]	4:0	Sub window weighted DFK high-frequency begin.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F1[3:0]	3:0	Sub window weighted DFK high-frequency slope adjustment.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F1[5:0]	5:0	Sub window adaptive DFK motion threshold.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	SST_EN_F1	7	Sub window SST enable.	
	-	6:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SST_POSTLPF_EN_F1	7	Sub window SST post-LPF enable.	
	SST_POSTLPF_MAX_F1	6	Sub window SST post-LPF maximum function enable.	
	-	5:0	Reserved.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SST_STATIC_CORE_TH_F1[5:0]	5:0	Sub window SST static motion coring threshold.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x22**	**Access : R/W**
	SST_STATIC_SGAIN_F1[3:0]	7:4	Sub window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F1[3:0]	3:0	Sub window SST static motion temporal difference gain.	
50h ~ 50h (102FA0h ~ 102FA1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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MADI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h ~ 71h (102FE0h ~ 102FE2h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
72h (102FE4h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:2	Reserved.	
	FBASE_LVL_STATUS[1:0]	1:0	Frame-based level status.	
78h ~ 79h (102FF0h ~ 102FF3h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
7Ah (102FF5h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
7Ch ~ 7Fh (102FF8h ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	

HVSP Register (Bank = 102F , Sub-bank = 23)

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '102F02h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F07h)	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '102F06h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '102F0Ah'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '102F0Eh'.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '102F12h'.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F2	7	Main window data format is 422.	
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CR_LOAD_INI_F2	5	Main Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F2[3:0]	3:0	Main window horizontal de-ringing threshold0.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F2	7	Main window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F2[2:0]	6:4	Main window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F2[3:0]	3:0	Main window horizontal de-ringing threshold2.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F2[7:0]	7:0	Main window horizontal de-ringing offset.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F2[7:0]	7:0	Main window horizontal de-ringing offset2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F2	7	Main window vertical Y de-ringing enable.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VSP_DE_RING_TH1_F2[2:0]	6:4	Main window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F2[3:0]	3:0	Main window vertical de-ringing threshold0.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F2	7	Main window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F2[2:0]	6:4	Main window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F2[3:0]	3:0	Main window vertical de-ringing threshold2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F2[7:0]	7:0	Main window vertical de-ringing offset.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F2[7:0]	7:0	Main window vertical de-ringing offset2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F2	7	Main window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	
1Bh (102F36h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO[7:0]	7:0	Dynamic horizontal scaling factor.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_HO[23:16]	7:0	See description of '102F38h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE[7:0]	7:0	Dynamic vertical scaling factor.	
1Eh	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Dh)	DY_FACTOR_VE[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_VE[23:16]	7:0	See description of '102F3Ch'.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_SELECT	7	Dynamic scaling factor usage. 0: For main window. 1: For sub window.	
	-	6:0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal initial factor.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F1[19:16]	3:0	See description of '102F42h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[7:0]	7:0	Sub window vertical initial factor 1.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[15:8]	7:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[23:16]	7:0	See description of '102F46h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[7:0]	7:0	Sub window vertical initial factor 2.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[15:8]	7:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[23:16]	7:0	See description of '102F4Ah'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal scaling factor.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[15:8]	7:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[23:16]	7:0	See description of '102F4Eh'.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F1	0	Sub window horizontal scaling enable.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[7:0]	7:0	Sub window vertical scaling factor.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[23:16]	7:0	See description of '102F52h'.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F1	7	Sub window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F1	0	Sub window vertical scaling enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F1	7	Sub window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F1	6	Sub window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F1	5	Sub window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F1	4	Sub window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F1[2:0]	3:1	Sub window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F1	0	Sub window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Bh	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F57h)	Y_RAM_SEL_VE_F1	7	Sub window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F1	6	Sub window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F1	5	Sub window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F1	4	Sub window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F1[2:0]	3:1	Sub window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F1	0	Sub window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F1	7	Sub window data format is 422.	
	422_INTP_F1	6	Sub window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F1	5	Sub Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F1	1	Sub window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F1	0	Sub window dithering enable for horizontal scaling process.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F1	3	Sub window vertical Y coring enable.	
	VSP_CORING_EN_C_F1	2	Sub window vertical C coring enable.	
	HSP_CORING_EN_Y_F1	1	Sub window horizontal Y coring enable.	
	HSP_CORING_EN_C_F1	0	Sub window horizontal C coring enable.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F1[7:0]	7:0	Sub window horizontal C coring threshold.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F1[7:0]	7:0	Sub window horizontal Y coring threshold.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F1[7:0]	7:0	Sub window vertical C coring threshold.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F1[7:0]	7:0	Sub window vertical Y coring threshold.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F1	7	Sub window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F1[2:0]	6:4	Sub window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F1[3:0]	3:0	Sub window horizontal de-ringing threshold0.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F1	7	Sub window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F1[2:0]	6:4	Sub window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F1[3:0]	3:0	Sub window horizontal de-ringing threshold2.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F1[7:0]	7:0	Sub window horizontal de-ringing offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F1[7:0]	7:0	Sub window horizontal de-ringing offset2.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F1	7	Sub window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F1[2:0]	6:4	Sub window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F1[3:0]	3:0	Sub window vertical de-ringing threshold0.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F1	7	Sub window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F1[2:0]	6:4	Sub window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F1[3:0]	3:0	Sub window vertical de-ringing threshold2.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F1[7:0]	7:0	Sub window vertical de-ringing offset.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F1[7:0]	7:0	Sub window vertical de-ringing offset2.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F1	7	Sub window vertical nonlinear scaling enable.	
	H_NL_EN_F1	6	Sub window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F1	3	Sub window pre-V down scaling boundary mode.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OP_FIELD_SEL_F1	2	Sub window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F1	1	Sub window field polarity switch.	
	2_INIFAC_MD_F1	0	Sub window two initial factors mode.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F1	7	Sub window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F1	6	Sub window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F1	5	Sub window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F1	4	Sub window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F1	2	Sub window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F1	1	Sub window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F1	0	Sub window horizontal nonlinear scaling width0 LSB.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width0.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width1.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width2.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F1	7	Sub window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F1[6:0]	6:0	Sub window horizontal nonlinear scaling initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 0.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 1.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F1[7:0]	7:0	Sub window vertical nonlinear scaling width0.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F1[7:0]	7:0	Sub window vertical nonlinear scaling width1.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F1[7:0]	7:0	Sub window vertical nonlinear scaling width2.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F1	7	Sub window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F1[6:0]	6:0	Sub window vertical nonlinear scaling initial value.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 0.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 1.	
3Bh (102F76h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CRAM_RW_EN	1	C SRAM read/write enable.	
	YRAM_RW_EN	0	Y SRAM read/write enable.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RAM_R_PULSE	1	SRAM read data pulse.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_ADDR[7:0]	7:0	SRAM read/write address. 0: Address 0~127. 1: Address 128~255.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[7:0]	7:0	SRAM write data.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[23:16]	7:0	See description of '102F86h'.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[31:24]	7:0	See description of '102F86h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[39:32]	7:0	See description of '102F86h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[7:0]	7:0	SRAM read data.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[23:16]	7:0	See description of '102F8Ch'.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[31:24]	7:0	See description of '102F8Ch'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[39:32]	7:0	See description of '102F8Ch'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x41**	**Access : R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.	
	-	6:0	Reserved.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x08**	**Access : R/W**
	3DLR_SIDE2LINE_EN	7	3D LR side-by-side to line-to-line enable.	
	-	6:0	Reserved.	
58h ~ 5Fh (102FB0h ~ 102FBFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F2[1:0]	7:6	Main window CTI step.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:3	Reserved.	
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CTI_STEP_F2[2]	0	See description of '102FC0h'.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F2	7	Main window CTI enable.	
	-	6:0	Reserved.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F2[3:0]	3:0	Main window CTI mutual threshold.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F2[2:0]	2:0	Main window CTI mutual step.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F2[1:0]	1:0	Main window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F2[4:0]	4:0	Main window CTI mutual level patch threshold.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F2[5:0]	5:0	Main window CTI mutual trans level slope gain.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F2[4:0]	4:0	Main window CTI mutual C low freq threshold.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F2[5:0]	5:0	Main window CTI mutual C low freq slope gain.	
66h	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FCCh)	-	7:2	Reserved.	
	CTI_CLFP_STEP_F2[1:0]	1:0	Main window CTI mutual C low freq step.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F1[1:0]	7:6	Sub window CTI step.	
	-	5:3	Reserved.	
	CTI_LPF_COEF_F1[2:0]	2:0	Sub window CTI LPF coefficients.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CTI_STEP_F1[2]	0	See description of '102FE0h'.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F1	7	Sub window CTI enable.	
	-	6:0	Reserved.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F1[3:0]	3:0	Sub window CTI mutual threshold.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F1[2:0]	2:0	Sub window CTI mutual step.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F1[1:0]	1:0	Sub window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F1[4:0]	4:0	Sub window CTI mutual level patch threshold.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F1[5:0]	5:0	Sub window CTI mutual trans level slope gain.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F1[4:0]	4:0	Sub window CTI mutual C low freq threshold.	

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HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F1[5:0]	5:0	Sub window CTI mutual C low freq slope gain.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_CLFP_STEP_F1[1:0]	1:0	Sub window CTI mutual C low freq step.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EXTRA_FACTOR_EN	0	Extra horizontal initial factor enable.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_1[7:0]	7:0	Extra horizontal initial factor 1.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_2[7:0]	7:0	Extra horizontal initial factor 2.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_3[7:0]	7:0	Extra horizontal initial factor 3.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_4[7:0]	7:0	Extra horizontal initial factor 4.	

PAFRC Register (Bank = 102F, Sub-bank = 24)

PAFRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:6	Reserved.	
	POL_TYPE	5	Pol type setting.	
	PAFRC_TAIL_CUT	4	Pafrc tail cut funtion. 0: Lsb use ori lsb. 1: Lsb use 0tailcut enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Enable. 1: Disable.	
	DITH_BITS	2	Dithering bits. 0: 2-bits. 1: 4-bits.	

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PAFRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TCON_OFF_EN	1	Tcon frc_gamma function off signal enable. 1: Gamma/dither function turn off by tcon frc_gamma_offTCON FRC_GAMMA function off signal enable.	
	FRC_ON	0	PAFRC enable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x23**	**Access : R/W**
	BOX_ROTATE_EN	7	Box A/B/C/D relation rotation enable.	
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.	
	TOP_BOX_FREEZE	4	Top box freeze.	
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.	
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].	
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.	
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.	
	B_D_SWAP	4	Blue channel diagonal swap.	
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotate.	
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotate.	
	BOX8X8_ROT_UNIT	1	0: Rotate step under per A, B, C or D. 1: Rotate step between A/B/C/D.	
	BOX_FREEZE	0	Box local rotation freeze.	
41h	**REG102F82**	**7:0**	**Default : 0xF3**	**Access : R/W**

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PAFRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F82h)	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x3C**	**Access : R/W**
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	

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PAFRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0xC9**	**Access : R/W**
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x9C**	**Access : R/W**
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0xC9**	**Access : R/W**
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4th 4 frame rotation step.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x9C**	**Access : R/W**
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3rd 4 frame rotation step.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0xAA**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0xAA**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x50**	**Access : R/W**
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Counterwise. 1: Back.	
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Counterwise. 1: Back.	
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Counterwise. 1: Back.	

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PAFRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Counterwise. 1: Back.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x22**	**Access : R/W**
	BOX8X8_ROT_00[1:0]	7:6	Box8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box8x8 entity 11 rotation step by reference.	
	BOX8X8_ROT_10[1:0]	1:0	Box8x8 entity 10 rotation step by reference.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0xD8**	**Access : R/W**
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.	
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.	
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.	
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.	
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.	
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.	
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x72**	**Access : R/W**
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.	
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.	
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.	
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x72**	**Access : R/W**
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.	
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.	
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.	
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x8D**	**Access : R/W**
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.	
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.	
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.	

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PAFRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x8D**	**Access : R/W**
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.	
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.	
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.	
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x27**	**Access : R/W**
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.	
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.	
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.	
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0xD8**	**Access : R/W**
	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.	
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.	
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.	
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x72**	**Access : R/W**
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.	
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.	
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.	
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x8D**	**Access : R/W**
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.	
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.	
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.	
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.	

XVYCC Register (Bank = 102F, Sub-bank = 25)

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	-	3:0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post r channel offset.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post g channel offset.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post b channel offset.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post r channel gain.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post g channel gain.	
25h	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**

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XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Bh)	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post b channel gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post r channel offset.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_BRI_OFFSET[7:0]	7:0	Sub window post g channel offset.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_BRI_OFFSET[7:0]	7:0	Sub window post b channel offset.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post r channel gain.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post g channel gain.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '102F56h'.	
2Ch	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**

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XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F58h)	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post b channel gain.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '102F58h'.	

DMS Register (Bank = 102F, Sub-bank = 26)

DMS Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x44**	**Access : R/W**
	-	7:6	Reserved.	
	V_C_LPF_EN_F1	5	Vertical C Low Pass Filter Enable F1.	
	SPIKE_NR_EN_F1	4	Spike NR Enable F1.	
	SPIKE_NR_MR_EN	3	Spike NR motion ratio enable.	
	-	2	Reserved.	
	V_C_LPF_EN_F2	1	Vertical C Low Pass Filter Enable F2.	
	SPIKE_NR_EN_F2	0	Spike NR Enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SPIKE_NR_COEF[3:0]	3:0	Spike NR Coefficient.	
51h (102FA2h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	P_THRD_1[4:0]	4:0	Spike NR P threshold 1.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_2[7:0]	7:0	Spike NR P threshold 2.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_3[7:0]	7:0	Spike NR P threshold 3.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	D_31_STEP[2:0]	6:4	Spike NR D31 Step.	
	-	3	Reserved.	

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DMS Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	D_11_21_STEP[2:0]	2:0	Spike NR D11_21 Step.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YP_22_STEP[2:0]	2:0	Spike NR YP22 Step.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPK_MR_LPF_EN_F1	4	Spike NRmotion ratio low pass filter enable F1 (lpf is 3x3 mask).	
	-	3:1	Reserved.	
	SPK_MR_LPF_EN_F2	0	Spike NR motion ratio low pass filter enable F2 (lpf is 3x3 mask).	
54h (102FA9h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_0[7:0]	7:0	Spike NR motion ratio look-up-table 0.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x32**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_1[7:0]	7:0	Spike NR motion ratio look-up-table 1.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_2[7:0]	7:0	Spike NR motion ratio look-up-table 2.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x76**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_3[7:0]	7:0	Spike NR motion ratio look-up-table 3.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x98**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_4[7:0]	7:0	Spike NR motion ratio look-up-table 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_5[7:0]	7:0	Spike NR motion ratio look-up-table 5.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_6[7:0]	7:0	Spike NR motion ratio look-up-table 6.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_7[7:0]	7:0	Spike NR motion ratio look-up-table 7.	

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ACE2 Register (Bank = 102F, Sub-bank = 27)

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CURVE_FIT_CF_LPF_EN	5	Sub window color factor low pass filter enable for luma curve [1 2 1].	
	SUB_COLOR_CURVE_FIT_EN	4	Sub window color adaptive enable for luma curve.	
	-	3:2	Reserved.	
	MAIN_CURVE_FIT_CF_LPF_EN	1	Main window color factor low pass filter enable for luma curve [1 2 1].	
	MAIN_COLOR_CURVE_FIT_EN	0	Main window color adaptive enable for luma curve.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	COLOR_PK_WIN1_CF_ENTRY_VALUE[3:0]	3:0	Flesh color adaptive noise masking strength (x.xxx), color define from peaking, format is x.xxx, range is 4'h0~4'h8.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:1	Reserved.	
	MAIN_CTI_EN	0	Main window CTI enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_CTI_STEP[2:0]	6:4	Main window CTI step.	
	-	3:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CTI_STEP[2:0]	6:4	Sub window CTI step.	

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ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:0	Reserved.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CTI_CORING_THRD[3:0]	3:0	Sub window CTI coring threshold.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_BAND_COEF[5:0]	5:0	Sub window CTI band pass filter coefficient.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_GRAY_THRD[3:0]	3:0	Main window CTI grap patch threshold.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CTI_GRAY_THRD[3:0]	3:0	Sub window CTI grap patch threshold threshold.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VIP_FUN_BYPASS_EN	0	Vip all function bypass enable.	

VOP2_RP Register (Bank = 102F, Sub-bank = 2D)

VOP2_RP Register (Bank = 102F, Sub-bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 02h (102F02h ~ 102F04h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
03h ~ 04h (102F06h ~ 102F08h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
05h ~ 06h (102F0Ah ~ 102F0Ch)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP2_RP Register (Bank = 102F, Sub-bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F20h)	OSD_HS_ST[7:0]	7:0	For osd reference hs start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_NEW_REF	7	Osd new reference hs/vfde enable.	
	-	6:5	Reserved.	
	OSD_HS_ST[12:8]	4:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_END[7:0]	7:0	For osd reference hs end.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OSD_HS_END[12:8]	4:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_ST[7:0]	7:0	For osd reference vfde start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_VFDE_ST[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_END[7:0]	7:0	For osd reference vfde end.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_VFDE_END[11:8]	3:0	See description of '102F26h'.	

DIP Register (Bank = 102F, Sub-bank = 34)

DIP Register (Bank = 102F, Sub-bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DIP_VS_INV	2	Dip vsync invert.	
	-	1:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x42**	**Access : R/W**
	-	7	Reserved.	
	DIP_OSD_VS_INV	6	Osd vsync inverse.	

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DIP Register (Bank = 102F, Sub-bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DIP_OSD_ALPHA_SEL[1:0]	5:4	Osd alpha selection, 0: gop alpha, 1: invert gop_alpha, 2: reg_dip_osd_alpha.	
	DIP_OSD_HS_SEL	3	Osd hsync selection.	
	DIP_OSD_FOREGND	2	Osd on foreground.	
	DIP_OSD_DE_MODE	1	De mode for gop to dip.	
	DIP_OSD_EN	0	De mode for gop to dip.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	DIP_OSD_ALPHA[5:0]	5:0	Osd alpha.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	DIP_ALIGN_EN	1	Pixel align enable.	
	DIP_CLIP_EN	0	Clipping enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_CLIP_H_ST[7:0]	7:0	Horizontal clipping start.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIP_CLIP_H_ST[11:8]	3:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_CLIP_H_END[7:0]	7:0	Horizontal clipping end.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIP_CLIP_H_END[11:8]	3:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_CLIP_V_ST[7:0]	7:0	Vertical clipping start.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIP_CLIP_V_ST[11:8]	3:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_CLIP_V_END[7:0]	7:0	Vertical clipping end.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIP_CLIP_V_END[11:8]	3:0	See description of '102F48h'.	

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DIP Register (Bank = 102F, Sub-bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x1E**	**Access : R/W**
	-	7:6	Reserved.	
	DIP_ALIGN_NUM[4:0]	5:1	Pixel align number.	
	DIP_ALIGN_NUM_SEL	0	Pixel align enable.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DIP_PDW_SRC_422	5	Dip_pdw source data select.	
	DIP_C_SEL	4	C data selection from cb or cr.	
	DIP_CBCR_SWAP	3	C filter mode.	
	DIP_C_FILTER[1:0]	2:1	C filter mode.	
	DIP_F422EN	0	444 to 422 enable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DIP_FRC_FAC[5:0]	5:0	Frc factor, 0: bypass.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	DIP_FRC_RST_P	0	Frc factor reset pulse.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_DUMMY[7:0]	7:0	Dummy register.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_DUMMY[15:8]	7:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	DB_EN	0	Double buffer enable.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RST	0	Software reset.	

DIPW Register (Bank = 102F, Sub-bank = 36)

DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**

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DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F02h)	DIP_WBE_MASK	7	Write byte enable mask.	
	DIP_DWIN_EN	6	Dwin enable.	
	DIP_FORMAT[1:0]	5:4	Dip data format (00: yc422 01: rgb565 10: argb8888 11: yc420).	
	DIP_INTLAC_W	3	Dip interlace write (two field in one frame).	
	DIP_FRAME_BUF_NUM[2:0]	2:0	Number of frame buffer.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_INTLAC_SRC	7	Dip interlace source.	
	DIP_NO_COLOR	6	Dip 420c force no color.	
	DIP_PROG_420C_SEL	5	Dip 420c selection for progressive source.	
	DIP_422TO420_RATIO[4:0]	4:0	Dip 422 to 420 c blending ratio.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_ARGB_ALPHA[7:0]	7:0	Alpha for format ARGB.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x04**	**Access : R/W**
	DIP_YC_SWAP	7	Dip y c swap.	
	DIP_CBCR_SWAP	6	Dip cb cr swap.	
	DIPW_PDW2MI_SEL	5	Miu select.	
	DIP_FORCE_WREQ_THRD	4	Force wreq thrd equal to reg_dip_wreq_thrd.	
	DIP_PDW_DITH_EN	3	Dip pdw dither enable.	
	DIP_PDW_OFF	2	Dip pdw off.	
	DIP_PDW_SRC_SEL[1:0]	1:0	Dip pdw source select.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DIP_HI_PRI_NUM[4:0]	4:0	High priority threshold for write request.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BLK_TILE	7	Block tile format.	
	-	6:3	Reserved.	
	DIP_LB_FULL_CLEAN	2	Riu read lb full clean.	
	DIP_DWIN_WT_ONCE_TRIG	1	Dwin write once trigger.	
	DIP_DWIN_WT_ONCE	0	Dwin write once.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_STATUS0[7:0]	7:0	Dipw status {lb_full, frame_index, din_rdy, pdw2dnr_ack, pdw2mi_wrdy, mi2pdw_wrdy}.	

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DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_STATUS1[7:0]	7:0	Fetch count to miu request.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_FIELD	7	Dipw field (top field: 0 bot field:1).	
	-	6:2	Reserved.	
	DIPW_STATUS1[9:8]	1:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_STATUS2[7:0]	7:0	Vcnt to miu request.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DIPW_STATUS2[11:8]	3:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	PDW_CHK_SUM_VCNT[3:0]	4:1	Check sum vcnt.	
	PDW_CHK_SUM_EN	0	Check sum enable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPW_IRQ_MASK[7:0]	7:0	Interrupt mask.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPW_IRQ_FORCE[7:0]	7:0	Interrupt force.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPW_IRQ_CLR[7:0]	7:0	Interrupt clear.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_IRQ_FINAL_STATUS[7:0]	7:0	Interrupt final status on CPU side.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_IRQ_RAW_STATUS[7:0]	7:0	Interrupt raw status on IP side.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x80**	**Access : R/W**
	DIP_MIU_GATE_EN	7	Dip miu clk gate enable.	
	DIP_ALIGN_EN	6	Dip align enable.	
	DIP_ALIGN_NUM_SEL	5	Select align number: 0-> hsize 1->reg_dip_align_num.	
	DIP_ALIGN_NUM[4:0]	4:0	Align number 1-31.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DIP_MIU_GATE_INV	0	Miu gate inverse.	

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DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_STATUS3[7:0]	7:0	Dipw check sum (high).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_STATUS3[15:8]	7:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_STATUS4[7:0]	7:0	Dipw check sum (low).	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : RO**
	DIPW_STATUS4[15:8]	7:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR0[7:0]	7:0	Frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR0[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR0[23:16]	7:0	See description of '102F20h'.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DIP_BASE_ADR0[26:24]	2:0	See description of '102F20h'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR2[7:0]	7:0	Frame buffer base address 2 (for yuvi 420 mode).	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR2[15:8]	7:0	See description of '102F30h'.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR2[23:16]	7:0	See description of '102F30h'.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DIP_BASE_ADR2[26:24]	2:0	See description of '102F30h'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_FETCH_NUM[7:0]	7:0	Fetch number of one line.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIP_FETCH_NUM[11:8]	3:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR1[7:0]	7:0	Frame buffer base address 1.	

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DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR1[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_BASE_ADR1[23:16]	7:0	See description of '102F40h'.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DIP_BASE_ADR1[26:24]	2:0	See description of '102F40h'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPR_FETCH_NUM[7:0]	7:0	Fetch number of one line for dipr.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIPR_FETCH_NUM[11:8]	3:0	See description of '102F4Eh'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_VCNT_NUM[7:0]	7:0	Line count number of one frame.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIP_VCNT_NUM[11:8]	3:0	See description of '102F5Eh'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_W_LIMIT_ADR[7:0]	7:0	Write limit address.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_W_LIMIT_ADR[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_W_LIMIT_ADR[23:16]	7:0	See description of '102F60h'.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_W_LIMIT_EN	7	Write limit enable.	
	-	6:3	Reserved.	
	DIP_W_LIMIT_ADR[26:24]	2:0	See description of '102F60h'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_LN_OFFSET[7:0]	7:0	Frame buffer line offset.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIP_LN_OFFSET[11:8]	3:0	See description of '102F7Eh'.	
40h	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**

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DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F80h)	DIP_C_BASE_W_LIMIT_ADR[7:0]	7:0	Write limit address for c base.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_C_BASE_W_LIMIT_ADR[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_C_BASE_W_LIMIT_ADR[23:16]	7:0	See description of '102F80h'.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DIP_C_BASE_W_LIMIT_ADR[26:24]	2:0	See description of '102F80h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_FRM_OFFSET[7:0]	7:0	Frame offset.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_FRM_OFFSET[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_FRM_OFFSET[23:16]	7:0	See description of '102FA0h'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_C_BASE_FRM_OFFSET[7:0]	7:0	Frame offset of c frame buffer.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_C_BASE_FRM_OFFSET[15:8]	7:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_C_BASE_FRM_OFFSET[23:16]	7:0	See description of '102FC0h'.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DIP_WREQ_THRD[5:0]	5:0	Wlb threshold for write request.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DIP_WREQ_MAX[6:0]	6:0	Write request maximum number.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PDW_ARB_MAX_REQ_NUM[7:0]	7:0	Rw arbiter max. Request number.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	PDW_ARB_SW_RST	4	Rw arbiter software reset.	
	PDW_ARB_BYPASS_EN	3	Rw arbiter bypass function enable.	

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DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDW_ARB_THD_HIT_LAST_EN	2	Rw arbiter gen. Last when thrd hit.	
	PDW_ARB_FLOW_CTRL_EN	1	Rw arbiter flow control enable.	
	PDW_ARB_RDY1_FIRST	0	Rw arbiter client 1 having higher priority than client 0.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x04**	**Access : R/W**
	PDW_ARB_RDY0_THD[7:0]	7:0	Thrd of flow control of client 0.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x04**	**Access : R/W**
	PDW_ARB_RDY1_THD[7:0]	7:0	Thrd of flow control of client 1.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPR_BASE_ADR0[7:0]	7:0	Dip frame buffer base address 0.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPR_BASE_ADR0[15:8]	7:0	See description of '102FF0h'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPR_BASE_ADR0[23:16]	7:0	See description of '102FF0h'.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DIPR_BASE_ADR0[26:24]	2:0	See description of '102FF0h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPR_FORMAT[1:0]	7:6	Read format.	
	DIPR_REQ_THRD[5:0]	5:0	Rlb empty count threshold for read request.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPR_PDW2MI_SEL	7	Miu select.	
	DIPR_EN	6	Dip read enable.	
	DIPR_FORCE_RREQ_THRD	5	Force rreq thrd equal to reg_dipr_req_thrd.	
	DIPR_HI_PRI_NUM[4:0]	4:0	High priority threshold for read request.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIP_YUVI_FORCE_BASE	7	Yuvi 420 mode force base adr form reg.	
	DIP_TILE_REQ_NUM[6:0]	6:0	Request number once for tile format.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPW2MI_I64	7	I64 mode.	
	DIP_YUVI_LINEAR	6	Yuvi 420 mode.	
	DIP_RGB_SWAP	5	Rgb swap rgb / bgr.	
	DIP_CLIP_EN	4	Clip enable.	

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DIPW Register (Bank = 102F, Sub-bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DIP_Y2R_EN	3	Yuv to rgb enable.	
	CR_LOAD_INI	2	Cr load ini for 422 to 444.	
	422TO444_MD[1:0]	1:0	422 to 444 mode 0:disable, 1:dup, 2:center, 3:co-located.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DIPR_TILE_REQ_NUM[6:0]	6:0	Request number once for tile format (dipr).	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIPR_INTLAC_R	7	Dip interlace read (two fields in one frame).	
	DIPR_REQ_MAX[6:0]	6:0	Read request maximum number.	

GOP_INT Register (Bank = 102F, Sub-bank = 40)

GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102F00h)	**REG102F00**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler.	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]: SWRST1[4]: IP, include F1 and F2. SWRST1[3]: OP include OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F06h)	GATED_MCLK_ON	7	Clk_miu enable.	
	-	6:2	Reserved.	
	PDMD[1:0]	1:0	PowerDown mode: 01: IDCLK. Others: IDCLK and ODCLK.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x10**	**Access : R/W**
	GCLK_MD[7:0]	7:0	PowerDown control: [1]: Live Fclk gated enable. [4]: Fclk gated control.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.	
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Dh)	COP_EN	7	Enable cop for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F26h)	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
16h	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Dh)	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	

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GOP_INT Register (Bank = 102F, Sub-bank = 40)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '102F48h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0xE1**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

IP1_M Register (Bank = 102F, Sub-bank = 41)

IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F06h)	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F18h)	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0		
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. #0: Left result. #1: right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. #0: Not clear. #1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. #0: Update every frame. #1: Keep the history value.	
	JITTER	3	JITTER function Result. #0: No JITTER. #1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. #0: Update every frame. #1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. #0: Result not ready. #1: Result ready.	
	ATS_EN	0	Auto position function Enable. #0: Disable. #1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F21h)	THOLD[3:0]	7:4	Auto position Valid Data Value. #0000: Valid if data >= 0000 0000. #0001: Valid if data >= 0001 0000. #0010: Valid if data >= 0010 0000. .. #1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Positoin Force Pixel Mode. #0 : DE or Pixel decide by the Source. #1 : Force Pixel Mode.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Aoto Gain Value. (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Bh)	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Bh)	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F42h)	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ah)	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x01**	**Access : R/W**
	_	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. #0: Can gate the GOP clock. #1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. #0: Don't gate the idclk. #1: Can gate the idclk.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:3	Reserved.	
	ATS_B_SKIP	2	Auto search ignore B data.	
	ATS_G_SKIP	1	Auto search ignore G data.	
	ATS_R_SKIP	0	Auto search ignore R data.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DE_BYPASS_MODE	7	Use input DE to replace SPRange_H as output DE.	
	-	6:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Ah)	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Atuto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	
40h ~ 43h (102F80h ~ 102F86h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F93h)	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	
	FDET_STATUS_INTLAC_DET0	0	Mode detect result 0.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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IP1_M Register (Bank = 102F, Sub-bank = 41)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	
60h ~ 60h (102FC0h ~ 102FC1h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
70h ~ 70h (102FE0h ~ 102FE1h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
71h (102FE3h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 42)

IP2_M Register (Bank = 102F, Sub-bank = 42)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Bh)	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	PREV_DOWN_3D	4	PREV_DOWN_3D.	
	-	3:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x08**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	
	YDELAY_EN	4	Y delay enable.	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	44TO42_DITH_EN	0	444 to 422 filter dith enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FILL_BLACK_NUM[5:0]	5:0	Fill black number.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILL_BLACK_ACT	7	FILL_BLACK_ACT.	
	FILL_BLACK_CLR	6	Clear fill_black register manually.	
	-	5:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OSD_HSK_MD	5	Ip2 osd handshaking mode.	
	FORCE_OSD_HSK	4	Force ip2 to osd in handshaking mode.	
	-	3	Reserved.	
	IP2_VS_SEL	2	1: Use mvop_vs to generate vs to opvs 0:use ip1_vs to generate vs to opvs.	
	FORCE_PRE2LAST	1	1: Use vsd last valid as pre align 0: use original pre align.	
	MVOP_DIN_EN	0	1: Data is form mvop 0: form yc delay.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RANDOM_SEL[1:0]	5:4	//random mode 0:1 1:3/4 2:1/2 3:1/4 rdy.	
	ALTIVE_LINE	3	//1: use chessboard data 0:use non line altive data;	
	CHESS_EN	2	//1: use chessboard data 0:use nomo data;	
	PAT_DATA_SEL	1	//1: use patgen data 0:use input data;	
	PAT_TIMING_SEL	0	//1: use patgen timing 1:use input timing;	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0xD0**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen h total.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0xE0**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen v total.	

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x40**	**Access : R/W**
	H_BLOCK[7:0]	7:0	Patgen h block.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen v block.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	V_BLOCK[9:8]	1:0	See description of '102F28h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xF2**	**Access : R/W**
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x1F**	**Access : R/W**
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x5E**	**Access : R/W**
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xF4**	**Access : R/W**
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x0C**	**Access : R/W**
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x5A**	**Access : R/W**
	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x37**	**Access : R/W**
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0xF5**	**Access : R/W**
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y0. Format: S7 of 2's complement (-15 <= Y0 <= 15).	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 127).	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x17**	**Access : R/W**
	HSD_CT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_CT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x0B**	**Access : R/W**
	HSD_CT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_CT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x29**	**Access : R/W**
	HSD_CT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C3. Format: Fix 8 (0 <= C3 <= 255).	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x01**	**Access : R/W**
	HSD_CT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C4. Format: S7 of 2's complement (-63 <= C4 <= + 63).	
28h	**REG102F50**	**7:0**	**Default : 0x04**	**Access : R/W**

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F50h)	HSD_CT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x3C**	**Access : R/W**
	HSD_CT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C2. Format: Fix 8 (0 <= C2 <= 127).	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:0	Reserved.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IP2DIP_SEL	0	IP2 to DIP source select: 1'b0: before HSD/VSD. 1'b1: after HSD/VSD.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IP2VE_VS_SEL	2	IP to VE vsync selection. 1'b0: IP1 vsync. 1'b1: original vsync.	
	IP2VE_CAP_EN	1	IP to VE cap enable.	
	IP2VE_PATH_EN	0	IP to VE enable.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2VE_HBLANK[3:0]	7:4	IP to VE H-blanking length.	
	IP2VE_RATE[3:0]	3:0	IP to VE flow control.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIN_CTRL_EN	7	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	6	IP2 VSD input line count number setting enable.	
	-	5	Reserved.	
	VSD_IN_NUM_USR[12:8]	4:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VOUT_CTRL_EN	7	IP2 VSD output line count control enable.	

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:5	Reserved.	
	VSD_OUT_NUMBER[12:8]	4:0	See description of '102F6Eh'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_HSD_OUT_CNT[12:8]	4:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_VSD_OUT_CNT[12:8]	4:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PREFLT_ALPHA_EN	7	IP2 Pre-Filter alpha blending enable.	
	-	6:5	Reserved.	
	PREFLT_ALPHA[4:0]	4:0	IP2 Pre-Filter alpha blending for original and filter.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_Y_TAP0[3:0]	3:0	IP2 Pre-Filter coefficient 0 [s.3] (T8).	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_FILTER_EN	7	IP2 Pre-Filter enable.	
	FIR_DITH_EN	6	IP2 Pre-Filter dith enable.	
	-	5:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP1[6:0]	6:0	IP2 Pre-Filter coefficient 1 [s.6] (T8).	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PRE_Y_TAP2[6:0]	6:0	IP2 Pre-Filter coefficient 2 [s.6] (T8).	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP3[7:0]	7:0	IP2 Pre-Filter coefficient 3 [s.7] (T8).	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP4[7:0]	7:0	IP2 Pre-Filter coefficient 4 [s.8] (T8).	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PRE_Y_TAP4[8]	0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP5[7:0]	7:0	IP2 Pre-Filter coefficient 5 [s.9] (T8).	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP5[9:8]	1:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP6[7:0]	7:0	IP2 Pre-Filter coefficient 6 [0.10] (T8).	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP6[9:8]	1:0	See description of '102F9Ch'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FLT_MODE	0	In advance mode 0:use 4 phase blending 1: use 8 phase blending.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT3_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x0D**	**Access : R/W**
	HSD_YT3_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x5C**	**Access : R/W**
	HSD_YT3_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x23**	**Access : R/W**
	HSD_YT3_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT3_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x03**	**Access : R/W**
	HSD_YT3_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_YT4_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x3B**	**Access : R/W**
	HSD_YT4_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT4_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_YT4_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable bpseudo blanking.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x08**	**Access : R/W**
	LB_SPLIT_BLANK[7:0]	7:0	LB pseudo blank cycle.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0xC0**	**Access : R/W**
	LB_AUTO	7	LB_AUTO.	
	VSD_FAC_AUTO_RST_EN	6	VSD 3d auto factor reset mode enable.	

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IP2_M Register (Bank = 102F, Sub-bank = 42)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:0	Reserved.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable dat_adj to src force ready.	
	-	0	Reserved.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[7:0]	7:0	Debug.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_DIFF[7:0]	7:0	Number of fifo.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_CLR[7:0]	7:0	DUMMY_CLR.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_CLR[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[7:0]	7:0	DUMMY_SET.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[15:8]	7:0	See description of '102FFEh'.	

IP1_S Register (Bank = 102F, Sub-bank = 43)

IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F06h)	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:5	Reserved.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Ou.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F18h)	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0		
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. #0: Left result. #1: right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. #0: Not clear. #1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. #0: Update every frame. #1: Keep the history value.	
	JITTER	3	JITTER function Result. #0: No JITTER. #1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. #0: Update every frame. #1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. #0: Result not ready. #1: Result ready.	
	ATS_EN	0	Auto position function Enable. #0: Disable. #1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F21h)	THOLD[3:0]	7:4	Auto position Valid Data Value. #0000: Valid if data >= 0000 0000. #0001: Valid if data >= 0001 0000. #0010: Valid if data >= 0010 0000. .. #1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Positoin Force Pixel Mode. #0 : DE or Pixel decide by the Source. #1 : Force Pixel Mode.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Aoto Gain Value. (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Bh)	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Bh)	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F42h)	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ah)	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. #0: Can gate the GOP clock. #1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. #0: Don't gate the idclk. #1: Can gate the idclk.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATS_B_SKIP	2	Auto search ignore B data.	
	ATS_G_SKIP	1	Auto search ignore G data.	
	ATS_R_SKIP	0	Auto search ignore R data.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DE_BYPASS_MODE	7	Use input DE to replace SPRange_H as output DE.	
	-	6:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Ah)	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Atuto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	
40h ~ 43h (102F80h ~ 102F86h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F93h)	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	
	FDET_STATUS_INTLAC_DET0	0	Mode detect result 0.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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IP1_S Register (Bank = 102F, Sub-bank = 43)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	

IP2_S Register (Bank = 102F, Sub-bank = 44)

IP2_S Register (Bank = 102F, Sub-bank = 44)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	

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IP2_S Register (Bank = 102F, Sub-bank = 44)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	-	6:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_S Register (Bank = 102F, Sub-bank = 44)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Fh)	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	-	4:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x08**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	
	YDELAY_EN	4	Y delay enable.	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	44TO42_DITH_EN	0	444 to 422 filter dith enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FILL_BLACK_NUM[5:0]	5:0	Fill black number.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILL_BLACK_ACT	7	FILL_BLACK_ACT.	
	FILL_BLACK_CLR	6	Clear fill_black register manually.	
	-	5:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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IP2_S Register (Bank = 102F, Sub-bank = 44)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_HSK_MD	5	Ip2 osd handshaking mode.	
	FORCE_OSD_HSK	4	Force ip2 to osd in handshaking mode.	
	IP2_MVOP_DAT_SEL	3	0: IP_f1 connect to DC1 IP_f2 connect to DC0 1:IP1_f1 connect to DC0 IP2_f2 connect to DC1.	
	IP2_VS_SEL	2	1: Use mvop_vs to generate vs to opvs 0:use ip1_vs to generate vs to opvs.	
	FORCE_PRE2LAST	1	1: Use vsd last valid as pre align 0: use original pre align.	
	MVOP_DIN_EN	0	1: Data is form mvop 0: form yc delay.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RANDOM_SEL[1:0]	5:4	//random mode 0:1 1:3/4 2:1/2 3:1/4 rdy.	
	-	3:2	Reserved.	
	PAT_DATA_SEL	1	//1: use patgen data 0:use input data;	
	PAT_TIMING_SEL	0	//1: use patgen timing 1:use input timing;	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0xD0**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen h total.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0xE0**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen v total.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x40**	**Access : R/W**
	H_BLOCK[7:0]	7:0	Patgen h block.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen v block.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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IP2_S Register (Bank = 102F, Sub-bank = 44)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	V_BLOCK[9:8]	1:0	See description of '102F28h'.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:0	Reserved.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IP2DIP_SEL	0	IP2 to DIP source select: 1'b0: before HSD/VSD. 1'b1: after HSD/VSD.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IP2VE_VS_SEL	2	IP to VE vsync selection. 1'b0: IP1 vsync. 1'b1: original vsync.	
	IP2VE_CAP_EN	1	IP to VE cap enable.	
	IP2VE_PATH_EN	0	IP to VE enable.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIN_CTRL_EN	7	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	6	IP2 VSD input line count number setting enable.	
	-	5	Reserved.	
	VSD_IN_NUM_USR[12:8]	4:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VOUT_CTRL_EN	7	IP2 VSD output line count control enable.	
	-	6:5	Reserved.	
	VSD_OUT_NUMBER[12:8]	4:0	See description of '102F6Eh'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_HSD_OUT_CNT[12:8]	4:0	See description of '102F7Ch'.	

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IP2_S Register (Bank = 102F, Sub-bank = 44)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_VSD_OUT_CNT[12:8]	4:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable bpseudo blanking.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x08**	**Access : R/W**
	SPLIT_BLANK[7:0]	7:0	Pseudo blank cycle.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable dat_adj to src force ready.	
	ADJ_AUTO	0	ADJ_AUTO.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[7:0]	7:0	Debug.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_DIFF[7:0]	7:0	Number of fifo.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_CLR[7:0]	7:0	DUMMY_CLR.	
7Eh	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_S Register (Bank = 102F, Sub-bank = 44)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FFDh)	DUMMY_CLR[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[7:0]	7:0	DUMMY_SET.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[15:8]	7:0	See description of '102FFEh'.	

PNR Register (Bank = 102F, Sub-bank = 45)

PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F1	7	Sub Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F1	6	Sub Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F1	5	Sub Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F1	4	Sub Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F1	3	Sub Window Post Noise Reduction for Y.	
	PNR_ENC_F1	2	Sub Window Post Noise Reduction for C.	
	RATIOYC_F1[1:0]	1:0	Sub Wimdow Motion Ratio.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F1	0	Sub Window select next field inverter for noc_sel.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F1	7	Sub Window DHD 3f mode enable.	
	PCCS_3F_EN_F1	6	Sub Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F1	4	Sub Window PCCS dither enable.	
	DHD_DITHER_EN_F1	3	Sub Window DHD dither enable.	
	PNR_BYPASS_F1	2	Sub Window PNR function bypass enable.	
	NR_EN_F1	1	Sub Window Post NR enable.	
	PCCS_EN_F1	0	Sub Window Post CCS enable.	
02h	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**

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PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F05h)	-	7	Reserved.	
	PAL_EN_F1	6	Sub Window PAL enable.	
	-	5:0	Reserved.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F1[2:0]	7:5	Sub Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F1[2:0]	4:2	Sub Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F1	1	Sub Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F1	0	Sub Window user-defined Y motion threshold enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	NR_Y_ROUND_F1	6	Sub Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F1	5	Sub Window enable select max motion for c.	
	YMOT_MAX_SEL_F1	4	Sub Window enable select max motion for y.	
	CMOT_DIV_MODE_F1[1:0]	3:2	Sub Window C motion divide mode.	
	YMOT_DIV_MODE_F1[1:0]	1:0	Sub Window Y motion divide mode.	
0Bh (102F16h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:3	Reserved.	
	DITHER_FRAME_RST_CNT[1:0]	2:1	Dither frame reset count.	
	DITHER_FRAME_RST_EN	0	Dither frame reset enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_F2[1:0]	1:0	Main Wimdow Motion Ratio.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:1	Reserved.	

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PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for noc_sel.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F2	7	Main Window DHD 3f mode enable.	
	PCCS_3F_EN_F2	6	Main Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F2	4	Main Window PCCS dither enable.	
	DHD_DITHER_EN_F2	3	Main Window DHD dither enable.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PAL_EN_F2	6	Main Window PAL enable.	
	-	5:0	Reserved.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F2	5	Main Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F2	4	Main Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F2	3	Main Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F2	2	Main Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F2	1	Main Window DHD YMR02 enable.	

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PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_EN_F2	0	Main Window DHD enable.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F1	5	Sub Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F1	4	Sub Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F1	3	Sub Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F1	2	Sub Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F1	1	Sub Window DHD YMR02 enable.	
	DHD_EN_F1	0	Sub Window DHD enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR02_TH[5:0]	5:0	DHD YMR02 threshold.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR02_GAIN[2:0]	2:0	DHD YMR02 gain.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR04_TH[5:0]	5:0	DHD YMR04 threshold.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR04_GAIN[2:0]	2:0	DHD YMR04 gain.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_CVAL_GAIN[7:0]	7:0	DHD C value gain.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_DIFFPIX_GAIN[3:0]	3:0	DHD pixel diff gain.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR02_TH[5:0]	5:0	DHD C motion02 threshold.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR02_GAIN[2:0]	2:0	DHD C motion02 gain.	
25h	**REG102F4A**	**7:0**	**Default : 0x10**	**Access : R/W**

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PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ah)	-	7:6	Reserved.	
	DHD_CMR04_TH[5:0]	5:0	DHD C motion04 threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR04_GAIN[2:0]	2:0	DHD C motion04 gain.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x30**	**Access : R/W**
	DHD_CEDGE_GAIN[7:0]	7:0	DHD C edge gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_YEDGE_GAIN[7:0]	7:0	DHD Y edge gain.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_DEBUG0_EN	7	DHD debug0 enable.	
	DHD_DEBUG1_EN	6	DHD debug1 enable.	
	-	5:0	Reserved.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_YMR_IIR_ALPHA[2:0]	6:4	DHD YMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_YMR_IIR_STEP[1:0]	1:0	DHD YMR IIR step.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_CMR_IIR_ALPHA[2:0]	6:4	DHD CMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_CMR_IIR_STEP[1:0]	1:0	DHD CMR IIR step.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_CEDGE_TH[3:0]	3:0	DHD C edge threshold.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YEDGE_TH[5:0]	5:0	DHD Y edge threshold.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_CVAL_TH[3:0]	3:0	DHD C value threshold.	
4Ch	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**

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PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F98h)	-	7	Reserved.	
	INV_SAT_OFFSET[6:0]	6:0	PCCS invert saturation offset.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INV_SAT_POWNUM[2:0]	6:4	PCCS invert saturation pownum.	
	INV_SAT_W[3:0]	3:0	PCCS invert saturation weight.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TDELTA_C_POWNUM[3:0]	7:4	PCCS inv-saturation delta pownum.	
	TDELTA_C_W[3:0]	3:0	PCCS inv-saturation delta weight.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS Y Fn Fn-2 coring threshold.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS Y Fn Fn-2 pre wieght.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS Y Fn Fn-2 post pownum.	
	-	3	Reserved.	
	YDIFF_FNFN2_POST_W[2:0]	2:0	PCCS Y Fn Fn-2 post wieght.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-2 coring threshold.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS C Fn Fn-2 pre wieght.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-2 post pownum.	
	-	3	Reserved.	
	CDIFF_FNFN2_POST_W[2:0]	2:0	PCCS C Fn Fn-2 post wieght.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RC_EV_POWNUM[2:0]	6:4	PCCS real color edge value pownum.	
	RC_EV_W[3:0]	3:0	PCCS real color edge value weight.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCMODIFYFAC_POWNUM[3:0]	7:4	PCCS cross color edge value pownum.	
	CCMODIFYFAC_W[3:0]	3:0	PCCS cross color edge value weight.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	YEDGEFAC_UP_OFFSET[7:0]	7:0	PCCS Y edge offset.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YEDGEFAC_POWNUM[2:0]	6:4	PCCS Y edge pownum.	
	YEDGEFAC_W[3:0]	3:0	PCCS Y edge weight.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BLEND_LPF_TURN_OFF	1	PCCS factor low-pass filter off.	
	MEDIAN_TURN_OFF	0	PCCS factor median filter off.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INV_CDIFF_FNFN2_POWNUM[3:0]	7:4	PCCS invert C Fn Fn-2 diff pownum.	
	INV_CDIFF_FNFN2_W[3:0]	3:0	PCCS invert C Fn Fn-2 diff weight.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-4 diff threshold.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN4_PRE_W[2:0]	2:0	PCCS C Fn Fn-4 diff pre weight.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-4 diff post pownu,	
	-	3	Reserved.	
	CDIFF_FNFN4_POST_W[2:0]	2:0	PCCS C Fn Fn-4 diff post weight.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_3F_POST_POWNUM[2:0]	6:4	PCCS Y 3F diff post pownum.	
	-	3	Reserved.	

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PNR Register (Bank = 102F, Sub-bank = 45)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	YDIFF_3F_POST_W[2:0]	2:0	PCCS Y 3F diff post weight.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[7:0]	7:0	PCCS Table.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[15:8]	7:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[23:16]	7:0	See description of '102FC0h'.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[31:24]	7:0	See description of '102FC0h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[39:32]	7:0	See description of '102FC0h'.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[47:40]	7:0	See description of '102FC0h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[55:48]	7:0	See description of '102FC0h'.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[63:56]	7:0	See description of '102FC0h'.	
78h ~ 78h (102FF0h ~ 102FF1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DNR Register (Bank = 102F, Sub-bank = 46)

DNR Register (Bank = 102F, sub-bank = 46)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F1_DNR_CORE_EN	1	F1 DNR CORE FUNCTION EN.	
	F1_DNR_EN	0	F1 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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DNR Register (Bank = 102F, sub-bank = 46)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F1_NR_TABLE_SEL_C	1	F1 DNR Table C Mapping Select. #0 : non-linear. #1 : linear.	
	F1_NR_TABLE_SEL_Y	0	F1 DNR Table Y Mapping Select. #0 : non-linear. #1 : linear.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F1_ROUND_MODE_C[1:0]	3:2	F1 DNR C blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
	F1_ROUND_MODE_Y[1:0]	1:0	F1 DNR Y blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F1_MAX_MOT_ENABLE_C	3	F1_MAX_MOT_ENABLE_C.	
	F1_MAX_MOT_ENABLE_Y	2	F1_MAX_MOT_ENABLE_Y.	
	F1_DNR_FILTER_EN_C	1	F1_DNR_FILTER_EN_C.	
	F1_DNR_FILTER_EN_Y	0	F1_DNR_FILTER_EN_Y.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_FILTER_DIV0_C[2:0]	7:5	F1_DNR_FILTER_DIV0_C.	
	F1_DNR_FILTER_DIV0_Y[2:0]	4:2	F1_DNR_FILTER_DIV0_Y.	
	-	1:0	Reserved.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_FILTER_MODE_C[1:0]	7:6	F1_DNR_FILTER_MODE_C.	
	F1_DNR_FILTER_MODE_Y[1:0]	5:4	F1_DNR_FILTER_MODE_Y.	
	F1_DNR_FILTER_DIV1_C[1:0]	3:2	F1_DNR_FILTER_DIV1_C.	
	F1_DNR_FILTER_DIV1_Y[1:0]	1:0	F1_DNR_FILTER_DIV1_Y.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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DNR Register (Bank = 102F, sub-bank = 46)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. #0 : non-linear. #1 : linear.	
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. #0 : non-linear. #1 : linear.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.	
	SNR_EN	0	F2 SNR FUNCTION EN.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.	
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.	
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	

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DNR Register (Bank = 102F, sub-bank = 46)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_SHARP_LEVEL[3:0]	3:0	SNR sharpness level.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0xBD**	**Access : R/W**
	F1_DNR_TABLEY_0[7:0]	7:0	F1 DNR TABLEY_0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x79**	**Access : R/W**
	F1_DNR_TABLEY_0[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x56**	**Access : R/W**
	F1_DNR_TABLEY_1[7:0]	7:0	F1 DNR TABLEY_1.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x34**	**Access : R/W**
	F1_DNR_TABLEY_1[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x12**	**Access : R/W**
	F1_DNR_TABLEY_2[7:0]	7:0	F1 DNR TABLEY_2.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_2[15:8]	7:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_3[7:0]	7:0	F1 DNR TABLEY_3.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_3[15:8]	7:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0xBD**	**Access : R/W**
	F1_DNR_TABLEC_0[7:0]	7:0	F1 DNR TABLEC_0.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x79**	**Access : R/W**
	F1_DNR_TABLEC_0[15:8]	7:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x56**	**Access : R/W**
	F1_DNR_TABLEC_1[7:0]	7:0	F1 DNR TABLEC_1.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x34**	**Access : R/W**
	F1_DNR_TABLEC_1[15:8]	7:0	See description of '102F6Ah'.	

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DNR Register (Bank = 102F, sub-bank = 46)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x12**	**Access : R/W**
	F1_DNR_TABLEC_2[7:0]	7:0	F1 DNR TABLEC_2.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_2[15:8]	7:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_3[7:0]	7:0	F1 DNR TABLEC_3.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_3[15:8]	7:0	See description of '102F6Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h	**REG102F8C**	**7:0**	**Default : 0x12**	**Access : R/W**

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DNR Register (Bank = 102F, sub-bank = 46)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F8Ch)	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	F2_WIN_EN	0	F2 DNR/SNR active window enable.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_XSTART[7:0]	7:0	F2 DNR/SNR active window start X.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XSTART[10:8]	2:0	See description of '102FE8h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_YSTART[7:0]	7:0	F2 DNR/SNR active window start Y.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YSTART[10:8]	2:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x68**	**Access : R/W**
	F2_WIN_XEND[7:0]	7:0	F2 DNR/SNR active window end X.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XEND[10:8]	2:0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0xF0**	**Access : R/W**
	F2_WIN_YEND[7:0]	7:0	F2 DNR/SNR active window end Y.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YEND[10:8]	2:0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F1[7:0]	7:0	F1 hcnt for debug.	
78h	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : RO**

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DNR Register (Bank = 102F, sub-bank = 46)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FF1h)	-	7:3	Reserved.	
	STATUS_HCNT_F1[10:8]	2:0	See description of '102FF0h'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F1[7:0]	7:0	F1 vcnt for debug.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F1	7	F1 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F1[10:8]	2:0	See description of '102FF2h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F2[7:0]	7:0	F2 hcnt for debug.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	STATUS_HCNT_F2[10:8]	2:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F2[7:0]	7:0	F2 vcnt for debug.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F2	7	F2 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F2[10:8]	2:0	See description of '102FF6h'.	

FILM Register (Bank = 102F, Sub-bank = 4A)

FILM Register (Bank = 102F, sub-bank = 4A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7	Reserved.	
	DET_FIELD_SEL_LC	6	DET_FIELD_SEL_LC.	
	-	5	Reserved.	
	DIFF_TH[12:8]	4:0	Difference threshold.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_CUR_ERROR_TH_F2[7:0]	7:0	32 current error threshold.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_PRE_ERROR_TH_F2[15:8]	7:0	32 previous error threshold.	

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FILM Register (Bank = 102F, sub-bank = 4A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_CUR_ERROR_TH_F2[7:0]	7:0	22 current error threshold.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_PRE_ERROR_TH_F2[15:8]	7:0	22 previous error threshold.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	32_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	32 total error max th.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x7F**	**Access : R/W**
	32_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	32 total error sum th.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x08**	**Access : R/W**
	22_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	22 total error max th.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x7F**	**Access : R/W**
	22_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	22 total error sum th.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	FIX_DIFF_TH[12:8]	4:0	Cur error sum th.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[7:0]	7:0	F2 counter 1 threshold.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[7:0]	7:0	F2 counter 3 threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[7:0]	7:0	F2 counter fix threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[15:8]	7:0	See description of '102F1Ch'.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x30**	**Access : R/W**
	FILM32_EN_F2	7	F2 32 film mode enable.	
	FILM22_EN_F2	6	F2 22 film mode enable.	
	-	5:4	Reserved.	
	PRE32_F2	3	F2 pre32.	
	-	2:0	Reserved.	

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FILM Register (Bank = 102F, sub-bank = 4A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xEE**	**Access : R/W**
	MOT_TH_PATCH_F2[7:4]	7:4	F2 patch motion threshold.	
	FM_MOT_PIXTH_F2[3:0]	3:0	F2 motion ratio threshold.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x14**	**Access : R/W**
	FM_MOT_CNTTH_F2[15:8]	7:0	F2 unmatch threshold.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FILM32_N1_EN_F2	7	F2 N1 film32 enable.	
	FILM22_N1_EN_F2	6	F2 N1 film22 enable.	
	-	5:0	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[7:0]	7:0	F2 read status.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[15:8]	7:0	See description of '102F30h'.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[7:0]	7:0	F2 patch read status.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[15:8]	7:0	See description of '102F34h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x50**	**Access : R/W**
	MULT_COEF_F2[7:4]	7:4	F2 multiplicant ratio.	
	-	3:1	Reserved.	
	RELATIVE_FM_EN_F2	0	F2 relative film mode frame diff enable.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x05**	**Access : R/W**
	LOWER_BOUND_FM_32_F2[15:8]	7:0	F2 frame diff lower bound.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[7:0]	7:0	F2 frame diff upper bound.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x03**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x0F**	**Access : R/W**
	CHECK_SEQ_F2[7:0]	7:0	F2 lock threshold to enter 22.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x44**	**Access : R/W**
	SPEEDUP_STEP_F2[7:4]	7:4	F2 speedup step.	
	SPEEDUP_SHIFT_F2[3:0]	3:0	F2 speedup shift value.	
23h	**REG102F47**	**7:0**	**Default : 0x80**	**Access : R/W**

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FILM Register (Bank = 102F, sub-bank = 4A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(102F47h)	SPEEDUP_EN_F2	7	F2 speedup enable.
	-	6:0	Reserved.

S_VOP Register (Bank = 102F, Sub-bank = 4F)

S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO_BO[3:0]	7:4	Main windowborder outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	
	-	3:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND[11:8]	3:0	See description of '102F14h'.	
0Bh	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F16h)	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	S_VDEST_3RD[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F3Ch'.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Bh)	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SMEN	7	SVM Main window Enable.	
	SMTE	6	SVM Main window Tap Enable.	
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
	SSWEN	3	SVM Sub window Enable.	
	SSWETE	2	SVM Sub window Tap Enable.	
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
27h	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Eh)	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.	
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.	
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data. 11: Y with tap filter.	
	SCORING[3:0]	3:0	SVM Coring.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	-	4:2	Reserved.	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TO_MISC_NON_MAIN_WIN_SEL_PRE[1:0]	1:0	OSD blending window select. 2'b00 select main window as OSD window. 2'b01 select sub window as OSD window. others: Select main and sub window as OSD window.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_CHECK_ALPHA_PRE	7	Check pre osd blending alpha value. 1: Enable. 0: Disable.	
	OSD_CHECK_ALPHA	6	Check osd blending alpha value. 1: Enable. 0: Disable.	
	-	5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	
	-	5:4	Reserved.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	RESERVED[1:0]	6:5	RESERVED.	
	-	4:0	Reserved.	
30h	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F60h)	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '102F6Ah'.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (bri_function) for main window R.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (bri_function) for main window G.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (bri_function) for main window B.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_R[7:0]	7:0	Brightness offset (bri_function) for sub window R.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (bri_function) for sub window G.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (bri_function) for sub window B.	
3Bh	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F77h)	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '102F80h'.	
41h	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F82h)	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '102F82h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CAP_STAGE[1:0]	5:4	Capture stage selection. 0: Before osd. 1: After osd. 2: VIP output.	
	-	3:0	Reserved.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '102F94h'.	
4Bh	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F96h)	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FREEZ_VCNT_VALUE[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when REG_NEW_LOCK_POINT is set high.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LOCK_VCNT_VALUE[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_VS_EN	6	Enable pseudo vsync for freeze region.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select insert_end point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_MAIN_R_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_R_MIN_LIMIT. REG_MAIN_R_MIN_SIGN = 0: MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_MAIN_G_MIN_SIGN = 1: MAIN_G_MIN = -MAIN_G_MIN_LIMIT. REG_MAIN_G_MIN_SIGN = 0: MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '102FB6h'.	
5Ch	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB8h)	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_MAIN_B_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_B_MIN_LIMIT. REG_MAIN_B_MIN_SIGN = 0: MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value , s.12 format sign bit is bit-12. REG_SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. REG_SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_SUB_G_MIN_SIGN = 1: MAIN_G_MIN = -SUB_G_MIN_LIMIT. REG_SUB_G_MIN_SIGN = 0: MAIN_G_MIN = SUB_G_MIN_LIMIT.	

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_SUB_B_MIN_SIGN = 1: MAIN_R_MIN = -SUB_B_MIN_LIMIT. REG_SUB_B_MIN_SIGN = 0: MAIN_R_MIN = SUB_B_MIN_LIMIT.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '102FC6h'.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[7:0]	7:0	New add function for RGB_compression.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[15:8]	7:0	See description of '102FD8h'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FWC_SUB_EN	4		
	-	3:2	Reserved.	
	FWC_DITHER_EN	1		
	FWC_MAIN_EN	0		
70h	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FE1h)	-	7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0		
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FWC_SLOPE[5:0]	5:0		
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	FWC_CTH[7:0]	7:0		
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[7:0]	7:0		
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '102FE4h'.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '102FE4h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '102FE4h'.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[47:40]	7:0	See description of '102FE4h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '102FE4h'.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '102FE4h'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '102FE4h'.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '102FE4h'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '102FE4h'.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '102FE4h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[7:0]	7:0		

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S_VOP Register (Bank = 102F, sub-bank = 4F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '102FF4h'.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '102FF4h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '102FF4h'.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '102FF4h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '102FF4h'.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '102FF4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '102FF4h'.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '102FF4h'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '102FF4h'.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '102FF4h'.	

VOP Register (Bank = 102F, Sub-bank = 50)

VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated when DB_MASK and DB_LOAD.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSST1[7:0]	7:0	Output VSYNC start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VSST	4	Output VSYNC D[11]start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST1[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS=1). 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSEND[11:8]	3:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHST[7:0]	7:0	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHST[12:8]	4:0	See description of '102F08h'.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHEND[7:0]	7:0	Output DE Horizontal END. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHEND[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVEND[7:0]	7:0	Output DE Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SIHST[12:8]	4:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SIHEND[12:8]	4:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVEND[7:0]	7:0	Scaling Image window Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVEND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HDTOT[12:8]	4:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VDTOT[11:8]	3:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x4C**	**Access : R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).	
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.	
	-	5:4	Reserved.	
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels. 1: Disable, Output H Total is always odd pixels.	
	MOD2	2	Mode 2. 0: Disable. 1: Enable.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLLMD0	7	Frame PLL Mode 0.	
	SL_TUNE_EN	6	Short line tune enable.	
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.	
	-	4:2	Reserved.	
	SSC_SHIFT	1	0: Enable. 1: Disable.	
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x20**	**Access : R/W**
	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x08**	**Access : R/W**
	LCK_TH[15:8]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP Register Enable.	
	-	1	Reserved.	
	NOISY_GEN	0	Noise Generator.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT1[7:0]	7:0	Frame PLL Limit.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT0[7:0]	7:0	Frame PLL Limit.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT[7:0]	7:0	Frame PLL Limit.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : RO**
	INTLX_VS_OFFSET[7:0]	7:0	The interlace vsync offset.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLX_VS_EN	5	Interlace vsync enable.	
	INTLX_VS_OFFSET[12:8]	4:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	BY_STAGE_VIP[3:0]	7:4	Vip report point stage.	
	BY_STAGE_OP2[3:0]	3:0	Report point stage.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	REP_RD_TRID	0	Report SW read trigger.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SWBLBK	6	Sub window Blue screen color. 0: Black color. 1: Blue color.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SWBLUE	5	Sub window Blue screen control. 0: Off. 1: On.	
	-	4:3	Reserved.	
	MBD_EN	2	Main window Border Enable.	
	MBLK	1	Main window Black screen control. 0: Off. 1: On.	
	NOSC_EN	0	No Signal Color Enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_G[7:0]	7:0	Frame Color - Green.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_B[7:0]	7:0	Frame Color - Blue.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_E_4_FRAME	7	Reset noise generator by frames enable.	
	NDMD	6	Noise Dithering Method.	
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.	
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.	
	DT3	3	Dither Type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.	
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F39h)	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma Write.	
	-	3:1	Reserved.	
	OUTFRR_EN0	0	Output Free-run Enable.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x07**	**Access : R/W**
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	-	6:0	Reserved.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_MD1	7	FPLL Mode 1.	
	FPLL_DIS	6	FPLL Stop.	
	-	5:3	Reserved.	
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.	
	-	1:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.	
	WHTS	5	White Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.	
	-	2:0	Reserved.	
22h	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F45h)	FBLALL_SET	7	Frame buffer less all set.	
	-	6:0	Reserved.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCHBLEND	7	OSD Character Blending mode.	
	-	6	Reserved.	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4	Reserved.	
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0%% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	MNS_COL[7:0]	7:0	Main Window No Signal Color.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	-	6:0	Reserved.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ch)	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CM31[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FTPS_PRE	7	Front-TPSCR. For pre_osd_blending. 0: Disable. 1: Enable.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255.1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F5Fh)	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : RO**
	OVSSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error less than 29h/2Ah.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	OVERDESTAT	6	Output Vertical DE Status.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : RO**
	OHTSTAT1[7:0]	7:0	Output H Total Status.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	FRACST1[7:0]	7:0	Fraction Status.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FRACST2[2:0]	2:0	Fraction Status.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FRACST3[2:0]	2:0	Fraction Status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	HTTMGN[7:0]	7:0	H Total Margin.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSCMGN[7:0]	7:0	SSC Margin.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSTVALUE0[7:0]	7:0	Read Start initial value.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	RSTVALUE1[7:0]	7:0	Read Start Value.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read Start initial value.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read Start Value.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	INP8	7	This bit with REG_INE_DRV3 to enable G replace R and B for gamma mapping.	
	ONE_DRV3	6	Gamma use G replace R and B for gamma mapping.	
	GABYP	5	By pass gamma function.	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTDATA[7:0]	7:0	Reserved.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.	
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	TFRACN[7:0]	7:0	Target Fraction Number. / Frame PLL limit RK[7:0].	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	PDP_MASK_EN	6	Reserved.	
	-	5	Reserved.	
	FX_PROT	4	Frame Change Protect.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x40**	**Access : R/W**
	TSTMD_REG_EN	7	Test Mode Register Enable. 0: Disable. 1: Enable.	
	-	6	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEE_DEBUG_SEL[2:0]	5:3	See Debug bus output byte enable, bit0=DI[7:0], bit1=DI[15:8], bit2=DI[23:16].	
	-	2:0	Reserved.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CLK_MODE	7	0: Disable. 1: Enable.	
	-	6	Reserved.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	TEST_MD[3:0]	3:0	Reserved.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	BOND_STS[7:0]	7:0	Reserved.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x44**	**Access : R/W**
	LP_SET0[7:0]	7:0	Output PLL Set.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x55**	**Access : R/W**
	LP_SET0[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	LP_SET1[7:0]	7:0	Output PLL Set.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBN10	7	10-bit Bus enable.	
	DITHER_MINUS	6	1: Enable.	
	-	5	Reserved.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	ODCLK_GATE_ST_SEL[2:0]	6:4		
	-	3:2	Reserved.	
	SEL_ORI_GATE	1		
	ODCLK_GATE_EN	0		
53h	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FA6h)	ODCLK_GATE_END_DLY[7:0]	7:0		
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ODCLK_GATE_END_DLY[11:8]	3:0	See description of '102FA6h'.	
56h (102FAChh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field created method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: Vsync end.	
	-	4:0	Reserved.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	REM[7:0]	7:0	Htoal REMainder value.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	REM[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PWM5DIV[8]	0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduce, only active when REG_TRACE_PHASE_EN is set to 1.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduce.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	T3D_PATH_SEL	2	1: T3d before pre_con_bri and after bri. 0: T3d before gamma and after pre_gamma_osd_blend.	
	-	1:0	Reserved.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x07**	**Access : R/W**
	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_0_REG[7:0]	7:0		
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_1_REG[7:0]	7:0		
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_2_REG[7:0]	7:0		
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_3_REG[7:0]	7:0		
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_4_REG[7:0]	7:0		
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_5_REG[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[7:0]	7:0	Input VDE PRD value.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[15:8]	7:0	See description of '102FD0h'.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[7:0]	7:0	Input Vtt PRD value.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC RANdom noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	
	-	4:0	Reserved.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:0	Reserved.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_R[7:0]	7:0	Data write to R LUT SRAM.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	See description of '102FDCh'.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FDFh)	-	7:4	Reserved.	
	WR_G[11:8]	3:0	See description of '102FDEh'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_B[7:0]	7:0	Data write to B LUT SRAM.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_B[11:8]	3:0	See description of '102FE0h'.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	See description of '102FE2h'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '102FEAh'.	
76h	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FECh)	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '102FEAh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '102FEEh'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 50)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	B_MAX_BASE0[11:8]	3:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	See description of '102FFEh'.	

SCMI Register (Bank = 102F, Sub-bank = 52)

SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data config from mode 5 change to mode 4.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force madi off.	
	MADI_FORCE_ON_F2	4	F2 force madi on.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	-	2	Reserved.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	OPM_LINEAR_BASE_SEL_F2	6	F2 linear mode base address selection.	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	IPM_LINEAR_EN_F2	4	F2 IP linear address enable.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	Y8_M4_ONLY_MODE_F2	3	F2 FB store Y8/M4 only mode.	
	Y8_ONLY_MODE_F2	2	F2 FB store Y-8bits only.	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	DUMMY04_14_14	6	F2 FB store Y-8bits only.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_BYPASS_INTERLACE_FILM_F2	4	Film-supported bypass interlace mode.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F2	7	F2 memysnc write bank reset.	
	IPM_WREQ_HPRI_SEL_F2	6	F2 ipm wreq high priority selection: 1'b0: ipm local priority. 1'b1: ip2_adj priority.	
	FRC_FREEMD_F2	5	F2 Force output odd/even toggle when 2DDi for interlace input.	
	MIU_SELECT_F2	4	F2 access MIU0 or MIU1 select.	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x02**	**Access : R/W**
	DUMMY05_10_15[5:0]	7:2		
	OPM_F1_EN	1	Enable OPM F1 register.	
	BK_FIELD_SEL_F2	0	F2 memysnc fd selection.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WBANK_ALIGN_USR_F2[1:0]	3:2	[0] wbank align user mode. [1] wbank force align.	
	-	1:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RW_BANK_MAP_MSB_F2	7	F2 msb bit of read/write bank mapping mode.	
	OPM_RBANK_SEL_MSB_F2	6	F2 OP force read bank select msb.	
	-	5:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x88**	**Access : R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x40**	**Access : R/W**
	RW_BANK_MAP_F2[2:0]	7:5	F2 read/write bank mapping mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IPM_BASE_ADDR0_F2[26:24]	2:0	See description of '102F10h'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_OFFSET_F2[12:8]	4:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_FETCH_NUM_F2[12:8]	4:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F20h'.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR0_F2[26:24]	2:0	See description of '102F20h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR1_F2[26:24]	2:0	See description of '102F24h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F2[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_EN_F2	7	F2 IP line count limit enable.	
	-	6:5	Reserved.	
	IPM_VCNT_LIMIT_NUM_F2[12:8]	4:0	See description of '102F30h'.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FORCE_MUTE_IPW_ENABLE_F2	5	Force IPM enable at av-mute case.	
	FIELD_NUM_F2[4:0]	4:0	F2 field number.	
19h	**REG102F33**	**7:0**	**Default : 0x10**	**Access : R/W**

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F33h)	OPM_FIELD_NUM_DEFINE_F2	7	Enable OPM F2 field number define.	
	OPM_FIELD_NUM_F2[4:0]	6:2	OPM F2 field number.	
	OPM_8READ_EN_F2	1	F2 opm 8read mode enable.	
	OPM_6READ_EN_F2	0	F2 opm 6read mode enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_EN_F2	7	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	6	F2 IP write limit flag 0: maximum 1: minimum.	
	-	5:3	Reserved.	
	IPM_W_LIMIT_ADR_F2[26:24]	2:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_EN_F2	7	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[14:8]	6:0	See description of '102F38h'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h	**REG102F46**	**7:0**	**Default : 0x10**	**Access : R/W**

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F46h)	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_FLOW_CTRL_CNT[7:0]	7:0	OPW request flow control count.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x88**	**Access : R/W**
	OPW_VP_CNT_CLR	7	OPW write mask field count clear.	
	OPW_MASK_MODE[2:0]	6:4	OPW write mask number by field.	
	OPW_STATUS_CLR	3	OPW status clear enable.	
	OPW_REQ_RST	2	OPW write request reset.	
	-	1	Reserved.	
	OPW_WREQ_OFF_F2	0	OPW write request disable.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_THRD[7:0]	7:0	OPW FIFO threshold for read request.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_HPRI[7:0]	7:0	OPW high priority threshold for read request.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPW_WREQ_MAX[7:0]	7:0	OPW read request max number.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x22**	**Access : R/W**
	OPW_WFIFO_DEPTH[7:0]	7:0	OPW line buffer length for memory data write.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_PRE_DELTA_0_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at real line case.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at real line case.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPM_3D_SBS_FORCE_EN_F2	1	F2 IPM 3D side by side input enable.	
	IPM_3D_EN_F2	0	F2 IPM 3D input enable.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY34_7_7	7	HDMI 3D OPM side by side read using PIP.	
	-	6:0	Reserved.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[15:8]	7:0	See description of '102F6Ah'.	
36h	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Ch)	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[15:8]	7:0	See description of '102F6Ch'.	
37h ~ 37h (102F6Eh ~ 102F6Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[15:8]	7:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[15:8]	7:0	See description of '102F7Ch'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x18**	**Access : R/W**
	DUMMY40_5_15[2:0]	7:5		
	OPM_LB_CEN_MODE	4	OP Line buffer power ctrl.	
	UPDATE_MEM_CONFIG_EN	3	Update memory format enable.	
	-	2	Reserved.	
	IPM_REG_DBF_EN_F2	1	F2 Register latch with input V sync enable.	
	OPM_REG_DBF_EN	0	Register latch with output V sync enable.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY40_5_15[10:3]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY41_7_6[1:0]	7:6		
	-	5:0	Reserved.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MADI_FORCE_OFF_F1	5	F1 force madi off.	
	MADI_FORCE_ON_F1	4	F1 force madi on.	
	-	3:0	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_LINEAR_EN_F1	4	F1 IP linear address enable.	
	OPM_4READ_EN_F1	3	F1 OP read 4 fields enable.	
	OPM_3READ_EN_F1	2	F1 OP read 3 fields enable.	
	OPM_2READ_EN_F1	1	F1 OP read 2 fields enable.	
	OPM_1READ_EN_F1	0	F1 OP read 1 field enable.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	FILM_HIGH_PRI_F1	3	F1 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F1	2	F1 OP film dot line data select.	
	DOT_LN_PON_SEL_F1	1	F1 OP MADi dot line data select.	
	-	0	Reserved.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DUMMY44_2_3[1:0]	3:2		
	-	1:0	Reserved.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F1	7	F1 memysnc write bank reset.	
	IPM_WREQ_HPRI_SEL_F1	6	F1 ipm wreq high priority selection: 1'b0: ipm local priority. 1'b1: ip2_adj priority.	
	-	5:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY45_9_15[6:0]	7:1		
	BK_FIELD_SEL_F1	0	F2 memysnc fd selection.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY46_4_7[3:0]	7:4		
	WBANK_ALIGN_USR_F1[1:0]	3:2	[0] wbank align user mode. [1] wbank force align.	
	-	1	Reserved.	
	WBANK_SRC_SEL_F1	0	F1 Wbank src selection: 1'b0: original. 1'b1: from sc1.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[7:0]	7:0	F1 OP frame buffer base address 0.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[23:16]	7:0	See description of '102FA0h'.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR0_F1[26:24]	2:0	See description of '102FA0h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[7:0]	7:0	F1 OP frame buffer base address 1.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[15:8]	7:0	See description of '102FA4h'.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[23:16]	7:0	See description of '102FA4h'.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR1_F1[26:24]	2:0	See description of '102FA4h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MWE_OFFSET_F1[7:0]	7:0	F1 OP demo mode pixel offset (pixel unit).	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_MWE_OFFSET_F1[11:8]	3:0	See description of '102FA8h'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F1[7:0]	7:0	F1 OP frame buffer line offset (pixel unit).	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F1[12:8]	4:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F1[7:0]	7:0	F1 OP fetch pixel number of one line.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F1[11:8]	3:0	See description of '102FAEh'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FORCE_MUTE_IPW_ENABLE_F1	5	Force IPS enable at av-mute case.	
	-	4:0	Reserved.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:2	Reserved.	
	OPM_8READ_EN_F1	1	F1 opm 8read mode enable.	
	OPM_6READ_EN_F1	0	F1 opm 6read mode enable.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[7:0]	7:0	OPW write limit address.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[15:8]	7:0	See description of '102FBCh'.	
5Fh	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FBEh)	OPW_W_LIMIT_ADR[23:16]	7:0	See description of '102FBCh'.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_EN	7	OPW write limit enable.	
	OPW_W_LIMIT_MIN	6	OPW write limit flag 0: maximum 1: minimum.	
	-	5:3	Reserved.	
	OPW_W_LIMIT_ADR[26:24]	2:0	See description of '102FBCh'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_0	4	SCM first arbiter bypass function enable.	
	SCM_ARB_SW_RST_0	3	SCM first arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_0	2	SCM first arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_0	1	SCM first arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_0	0	SCM first arbiter client 1 having higher priority than client 0.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM_0[7:0]	7:0	SCM first arbiter maximum request number for each last.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY0_THD_0[7:0]	7:0	SCM first arbiter threshold number of flow control of client 0.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_0[7:0]	7:0	SCM first arbiter threshold number of flow control of client 1.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY66_13_15[2:0]	7:5		
	-	4:0	Reserved.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FD_MASK_READ_F1	5	F1 fd mask read back.	
	FD_MASK_READ_F2	4	F2 fd mask read back.	
	-	3:2	Reserved.	
	OPW_WREQ_OFF_ALL	1	All OPW write request disable.	
	OPW_WREQ_OFF_F1	0	F1 OPW write request disable.	

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY67_8_15[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_1	4	SCM second arbiter bypass function enable.	
	SCM_ARB_SW_RST_1	3	SCM second arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_1	2	SCM second arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_1	1	SCM second arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_1	0	SCM second arbiter client 1 having higher priority than client 0.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM_1[7:0]	7:0	SCM second arbiter maximum request number for each last.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY0_THD_1[7:0]	7:0	SCM second arbiter threshold number of flow control of client 0.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_1[7:0]	7:0	SCM second arbiter threshold number of flow control of client 1.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_2	4	SCM third arbiter bypass function enable.	
	SCM_ARB_SW_RST_2	3	SCM third arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_2	2	SCM third arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_2	1	SCM third arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_2	0	SCM third arbiter client 1 having higher priority than client 0.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x0C**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM_2[7:0]	7:0	SCM third arbiter maximum request number for each last.	
6Bh	**REG102FD6**	**7:0**	**Default : 0x08**	**Access : R/W**

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FD6h)	SCM_ARB_RDY0_THD_2[7:0]	7:0	SCM third arbiter threshold number of flow control of client 0.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_2[7:0]	7:0	SCM third arbiter threshold number of flow control of client 1.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at real line case.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at real line case.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[7:0]	7:0	F1 status read out for debug.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[15:8]	7:0	See description of '102FFAh'.	
7Eh	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : RO**

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SCMI Register (Bank = 102F, sub-bank = 52)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FFCh)	STATUS_READ_7E_F1[7:0]	7:0	F1 status read out for debug.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7E_F1[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[7:0]	7:0	F1 status read out for debug.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[15:8]	7:0	See description of '102FFEh'.	

IPOL Register (Bank = 102F, Sub-bank = 53)

IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F05h)	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Ch)	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Ou.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0		
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Dh)	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F43h)	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F48h)	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F49h)	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F50h)	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 53)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Dh)	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	

OP1_TOP Register (Bank = 102F, Sub-bank = 60)

OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x01**	**Access : R/W**
	PIP_DISABLE	7	Disable PIP Function.	
	-	6	Reserved.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SC2LB_EN	5	Enable HD side by side line buffer mode.	
	-	4:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the screen.	
	MAIN_EN	0	Enable main window shown on the screen.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	
	FBL_SEL	4	Select FBL source. #b0: Source F2 is FBL. #b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x70**	**Access : R/W**
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x07**	**Access : R/W**
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the extra_y to half.	
	-	4:3	Reserved.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. #h0: 16 pixel. #h1: 32 pixel. #h2: 64 pixel. #h3: 128 pixel. #h4: (overlap length) / 8. #h5: (overlap length) / 4. #h6: (overlap length) / 2. #h7: (overlap length).	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F1[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F2[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F1[11:8]	3:0	See description of '102F2Ch'.	
17h	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Eh)	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.	
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x02**	**Access : R/W**
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).	
	EXTRA_FETCH_LINE[3:0]	3:0	How many line will be fetched by extra request. Minimum is 1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_F2_EN	1	Force F1 use F2's register setting.	
	ATP_EN	0	Manual tune parameter.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xB8**	**Access : R/W**
	SEL_DS	7	Select the source to trigger dynamic scaling. h0: Falling edge of Vsync. h1: Delay line set by REG_DS_TRIG_DLY.	
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. #0: vsync of SC_TOP. #1: delay one line of vfde.	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. #h0: down_eq7. #h1: down_eq8. #h2: down_eq9. #h3: delay lines set by reg_disp_trig_dly.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. #h0: Falling edge of vsync. #h1: Nearly raising edge of vsync. #h2: delay line set by reg_atp_trig_dly. #h3: Manual trig by set reg_atp_en.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. #h0: Falling edge of vfde. #h1: Raising edge of vsync. #h2: Reserved. #h3: Reserved.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEL_MLOAD[1:0]	5:4	Select the source to trigger menuload. h0: Falling edge of VFDE. h1: Rising edge of VSync. h2: Falling edge of VSync. h3: Delay line set by REG_MLOAD_TRIG_DLY.	
	-	3:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x03**	**Access : R/W**
	ATP_TRIG_DLY[7:0]	7:0	Generate train_trig_p from delayed line of vsync.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x05**	**Access : R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate disp_trig_p from delayed line of vsync.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. Extra_eq will be disabled when overlapped length less then this threshold.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra request.	
1Fh	**REG102F3E**	**7:0**	**Default : 0xC2**	**Access : R/W**

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Eh)	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. #h0: 2 pixel. #h1: 4 pixel. #h2: 8 pixel. #h3: 16 pixel.	
	DISP_START_MODE	5	Select the display line buffer start mode. #0: start at advance 1 display line. #1: start at faling edge of vsync_init.	
	DISP_LB_MODE	4	Select the trig mode. #0: Line base. #1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. #h0: before 8 pixel. #h1: before 16 pixel. #h2: before 32 pixel. #h3: before 64 pixel.	
	DISP_RLN_MODE[1:0]	1:0	Select the under_run value of display level. #h0: update by hsync (not optimum performance). #h1: update when session done(may error). #h2: update when line done(reg_disp_trig_mode = 1'b0). #h3: Reserved.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_UNDER_MODE	3	Select the under_run value of display level. #0: 16'h0000. #1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of op1_disp.	
	DISP_LB_WEZ	1	Disable wen of display line buffer.	
	DISP_TRIG_MODE	0	Select the trig mode. #0: Trigged by self_counter. #1: Trigged by op2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x07**	**Access : R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x01**	**Access : R/W**
	DS_TRIG_DLY[7:0]	7:0	Generate DS_TRIG_P from delayed line of Vsync.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	DS_TRIG_DLY[11:8]	3:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x01**	**Access : R/W**
	MLOAD_TRIG_DLY[7:0]	7:0	Generate MLOAD_TRIG_P from delayed line of Vsync.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MLOAD_TRIG_DLY[11:8]	3:0	See description of '102F44h'.	
24h (102F48h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:3	Reserved.	
	FLAG_BB_ADR_INI	2	Status of cnt_bb_adr_ini, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	FLAG_BO_END_LN	1	Status of line_base_bot, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	-	0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BO_END_LN[7:0]	7:0	Software mode to set the line_base_bot for extra request.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	SW_BO_END_LN[11:8]	3:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the cnt_bb_adr_ini.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	SW_BB_ADR_INI[11:8]	3:0	See description of '102F64h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line cnt of first display position.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line cnt of minimum display level occure.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '102F88h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_LEN[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_LEN[11:8]	3:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_LEN[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1A[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1B[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_LENGTH_RD[7:0]	7:0	Read bo_length.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '102FBEh'.	

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_LEN[11:8]	3:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	
66h	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : RO**

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OP1_TOP Register (Bank = 102F, sub-bank = 60)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FCDh)	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '102FCEh'.	

ELA Register (Bank = 102F, Sub-bank = 61)

ELA Register (Bank = 102F, sub-bank = 61)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	

MADI Register (Bank = 102F, Sub-bank = 62)

MADI Register (Bank = 102F, sub-bank = 62)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h	**REG102F04**	**7:0**	**Default : 0x80**	**Access : R/W**

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MADI Register (Bank = 102F, sub-bank = 62)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F04h)	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. #0: disable C ratio filter. #1: enable C ratio filter.	
	RATIO_C_LOWBOUND_F2	6	Main window C ratio lower bound enable.	
	RSV_02_2_F2[1:0]	5:4	Reserved.	
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. #0: Enable. #1: Disable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x86**	**Access : R/W**
	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	

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MADI Register (Bank = 102F, sub-bank = 62)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HIS_RATIO_OFFSET_F2[3:0]	3:0	Main Window history ratio offset.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x07**	**Access : R/W**
	RSV_STAT_0_F2[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F2	5	Main window ratio statistics: ratio incremental mode.	
	STAT_SEL_C_F2	4	Main window ratio statistics: ratio selection.	
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: coring threshold.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: motion status.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[23:16]	7:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.	
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.	
	-	5	Reserved.	
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F2[3:0]	3:0	Main window DFK manual weighting.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x08**	**Access : R/W**
	_	7:5	Reserved.	
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x04**	**Access : R/W**
	_	7:4	Reserved.	
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x14**	**Access : R/W**
	_	7:5	Reserved.	
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x04**	**Access : R/W**
	_	7:4	Reserved.	
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.	
13h	**REG102F26**	**7:0**	**Default : 0x30**	**Access : R/W**

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MADI Register (Bank = 102F, sub-bank = 62)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F26h)	-	7:6	Reserved.	
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	SST_EN_F2	7	Main window SST enable.	
	-	6:0	Reserved.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.	
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.	
	-	5:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x22**	**Access : R/W**
	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F1	7	Sub window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F1[2:0]	2:0	Sub window ratio divide mode when Y/C separate.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F1[2:0]	5:3	Sub window ratio divide mode.	
	RATIO_MD_F1[2:0]	2:0	Sub window ratio filter mode.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x80**	**Access : R/W**
	RATIO_C_INDEP_F1	7	Sub window C ratio independent mode. #0: disable C ratio filter. #1: enable C ratio filter.	
	RATIO_C_LOWBOUND_F1	6	Sub window C ratio lower bound enable.	
	-	5:4	Reserved.	
	RATIO_C_MIN_F1[3:0]	3:0	Sub window C minimum ratio in independent mode.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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MADI Register (Bank = 102F, sub-bank = 62)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RATIO_C_YMAX_DIS_F1	0	Sub window C ratio takes Y ratio mode disable. #0: Enable. #1: Disable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:6	Reserved.	
	PRE_MOT_OFFSET_F1[5:0]	5:0	Sub Window pre-memory motion offset for motion calculation.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_MOT_GAIN_F1[3:0]	3:0	Sub Window pre-memory motion gain for motion calculation.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F1[5:0]	5:0	Sub Window post-memory motion offset for motion calculation.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F1[3:0]	7:4	Sub Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F1[3:0]	3:0	Sub Window post-memory motion gain for C motion calculation.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x86**	**Access : R/W**
	POST_MOT_YMAX_EN_F1	7	Sub Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F1[2:0]	2:0	Sub Window history weighting.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	HIS_RATIO_OFFSET_F1[3:0]	3:0	Sub Window history ratio offset.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F1	7	Sub window adaptive DFK enable.	
	WEGT_MED_EN_F1	6	Sub window weighted DFK enable.	
	-	5	Reserved.	
	MED_MANUAL_EN_F1	4	Sub window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F1[3:0]	3:0	Sub window DFK manual weighting.	

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MADI Register (Bank = 102F, sub-bank = 62)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F1[4:0]	4:0	Sub window weighted DFK low-frequency begin.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F1[3:0]	3:0	Sub window weighted DFK low-frequency slope adjustment.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F1[4:0]	4:0	Sub window weighted DFK high-frequency begin.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F1[3:0]	3:0	Sub window weighted DFK high-frequency slope adjustment.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F1[5:0]	5:0	Sub window adaptive DFK motion threshold.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	SST_EN_F1	7	Sub window SST enable.	
	-	6:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SST_POSTLPF_EN_F1	7	Sub window SST post-LPF enable.	
	SST_POSTLPF_MAX_F1	6	Sub window SST post-LPF maximum function enable.	
	-	5:0	Reserved.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SST_STATIC_CORE_TH_F1[5:0]	5:0	Sub window SST static motion coring threshold.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x22**	**Access : R/W**
	SST_STATIC_SGAIN_F1[3:0]	7:4	Sub window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F1[3:0]	3:0	Sub window SST static motion temporal difference gain.	

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HVSP Register (Bank = 102F, Sub-bank = 63)

HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '102F02h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '102F06h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '102F0Ah'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '102F0Eh'.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '102F12h'.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '102F12h'.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F2	7	Main window data format is 422.	
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F2	5	Main Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSP_DE_RING_TH0_F2[3:0]	3:0	Main window horizontal de-ringing threshold0.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F2	7	Main window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F2[2:0]	6:4	Main window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F2[3:0]	3:0	Main window horizontal de-ringing threshold2.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F2[7:0]	7:0	Main window horizontal de-ringing offset.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F2[7:0]	7:0	Main window horizontal de-ringing offset2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F2	7	Main window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F2[2:0]	6:4	Main window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F2[3:0]	3:0	Main window vertical de-ringing threshold0.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F2	7	Main window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F2[2:0]	6:4	Main window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F2[3:0]	3:0	Main window vertical de-ringing threshold2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F2[7:0]	7:0	Main window vertical de-ringing offset.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F2[7:0]	7:0	Main window vertical de-ringing offset2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F2	7	Main window vertical 3tap scaling enable.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Bh (102F36h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO[7:0]	7:0	Dynamic horizontal scaling factor.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_HO[23:16]	7:0	See description of '102F38h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE[7:0]	7:0	Dynamic vertical scaling factor.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_VE[23:16]	7:0	See description of '102F3Ch'.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_SELECT	7	Dynamic scaling factor usage. 0: For main window. 1: For sub window.	
	-	6:0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal initial factor.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F1[19:16]	3:0	See description of '102F42h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[7:0]	7:0	Sub window vertical initial factor 1.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[15:8]	7:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[23:16]	7:0	See description of '102F46h'.	
25h	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ah)	INI_FACTOR2_VE_F1[7:0]	7:0	Sub window vertical initial factor 2.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[15:8]	7:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[23:16]	7:0	See description of '102F4Ah'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal scaling factor.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[15:8]	7:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[23:16]	7:0	See description of '102F4Eh'.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F1	0	Sub window horizontal scaling enable.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[7:0]	7:0	Sub window vertical scaling factor.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[23:16]	7:0	See description of '102F52h'.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F1	7	Sub window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F1	0	Sub window vertical scaling enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F1	7	Sub window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F1	6	Sub window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F1	5	Sub window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	C_RAM_EN_HO_F1	4	Sub window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F1[2:0]	3:1	Sub window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F1	0	Sub window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F1	7	Sub window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F1	6	Sub window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F1	5	Sub window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F1	4	Sub window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F1[2:0]	3:1	Sub window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F1	0	Sub window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F1	7	Sub window data format is 422.	
	422_INTP_F1	6	Sub window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F1	5	Sub Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F1	1	Sub window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F1	0	Sub window dithering enable for horizontal scaling process.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F1	3	Sub window vertical Y coring enable.	
	VSP_CORING_EN_C_F1	2	Sub window vertical C coring enable.	
	HSP_CORING_EN_Y_F1	1	Sub window horizontal Y coring enable.	
	HSP_CORING_EN_C_F1	0	Sub window horizontal C coring enable.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F1[7:0]	7:0	Sub window horizontal C coring threshold.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F1[7:0]	7:0	Sub window horizontal Y coring threshold.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F1[7:0]	7:0	Sub window vertical C coring threshold.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F1[7:0]	7:0	Sub window vertical Y coring threshold.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F1	7	Sub window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F1[2:0]	6:4	Sub window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F1[3:0]	3:0	Sub window horizontal de-ringing threshold0.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F1	7	Sub window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F1[2:0]	6:4	Sub window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F1[3:0]	3:0	Sub window horizontal de-ringing threshold2.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F1[7:0]	7:0	Sub window horizontal de-ringing offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F1[7:0]	7:0	Sub window horizontal de-ringing offset2.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F1	7	Sub window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F1[2:0]	6:4	Sub window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F1[3:0]	3:0	Sub window vertical de-ringing threshold0.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F1	7	Sub window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F1[2:0]	6:4	Sub window vertical de-ringing threshold3.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VSP_DE_RING_TH2_F1[3:0]	3:0	Sub window vertical de-ringing threshold2.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F1[7:0]	7:0	Sub window vertical de-ringing offset.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F1[7:0]	7:0	Sub window vertical de-ringing offset2.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F1	7	Sub window vertical nonlinear scaling enable.	
	H_NL_EN_F1	6	Sub window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F1	3	Sub window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F1	2	Sub window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F1	1	Sub window field polarity switch.	
	2_INIFAC_MD_F1	0	Sub window two initial factors mode.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F1	7	Sub window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F1	6	Sub window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F1	5	Sub window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F1	4	Sub window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F1	2	Sub window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F1	1	Sub window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F1	0	Sub window horizontal nonlinear scaling width0 LSB.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width0.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width1.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width2.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F1	7	Sub window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F1[6:0]	6:0	Sub window horizontal nonlinear scaling initial value.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 0.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 1.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F1[7:0]	7:0	Sub window vertical nonlinear scaling width0.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F1[7:0]	7:0	Sub window vertical nonlinear scaling width1.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F1[7:0]	7:0	Sub window vertical nonlinear scaling width2.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F1	7	Sub window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F1[6:0]	6:0	Sub window vertical nonlinear scaling initial value.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 0.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 1.	
3Bh (102F76h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CRAM_RW_EN	1	C SRAM read/write enable.	
	YRAM_RW_EN	0	Y SRAM read/write enable.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RAM_R_PULSE	1	SRAM read data pulse.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_ADDR[7:0]	7:0	SRAM read/write address. 0: Address 0~127. 1: Address 128~255.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[7:0]	7:0	SRAM write data.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[23:16]	7:0	See description of '102F86h'.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[31:24]	7:0	See description of '102F86h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[39:32]	7:0	See description of '102F86h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[7:0]	7:0	SRAM read data.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[23:16]	7:0	See description of '102F8Ch'.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[31:24]	7:0	See description of '102F8Ch'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[39:32]	7:0	See description of '102F8Ch'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x41**	**Access : R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:0	Reserved.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x08**	**Access : R/W**
	3DLR_SIDE2LINE_EN	7	3D LR side-by-side to line-to-line enable.	
	-	6:0	Reserved.	
58h ~ 5Fh (102FB0h ~ 102FBFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F2[1:0]	7:6	Main window CTI step.	
	-	5:3	Reserved.	
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CTI_STEP_F2[2]	0	See description of '102FC0h'.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F2	7	Main window CTI enable.	
	-	6:0	Reserved.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F2[3:0]	3:0	Main window CTI mutual threshold.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F2[2:0]	2:0	Main window CTI mutual step.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F2[1:0]	1:0	Main window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F2[4:0]	4:0	Main window CTI mutual level patch threshold.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F2[5:0]	5:0	Main window CTI mutual trans level slope gain.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F2[4:0]	4:0	Main window CTI mutual C low freq threshold.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F2[5:0]	5:0	Main window CTI mutual C low freq slope gain.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_CLFP_STEP_F2[1:0]	1:0	Main window CTI mutual C low freq step.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F1[1:0]	7:6	Sub window CTI step.	
	-	5:3	Reserved.	
	CTI_LPF_COEF_F1[2:0]	2:0	Sub window CTI LPF coefficients.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CTI_STEP_F1[2]	0	See description of '102FE0h'.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F1	7	Sub window CTI enable.	
	-	6:0	Reserved.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F1[3:0]	3:0	Sub window CTI mutual threshold.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F1[2:0]	2:0	Sub window CTI mutual step.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	

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HVSP Register (Bank = 102F, sub-bank = 63)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CTI_PATCH_MODE_F1[1:0]	1:0	Sub window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F1[4:0]	4:0	Sub window CTI mutual level patch threshold.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F1[5:0]	5:0	Sub window CTI mutual trans level slope gain.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F1[4:0]	4:0	Sub window CTI mutual C low freq threshold.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F1[5:0]	5:0	Sub window CTI mutual C low freq slope gain.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_CLFP_STEP_F1[1:0]	1:0	Sub window CTI mutual C low freq step.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EXTRA_FACTOR_EN	0	Extra horizontal initial factor enable.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_1[7:0]	7:0	Extra horizontal initial factor 1.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_2[7:0]	7:0	Extra horizontal initial factor 2.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_3[7:0]	7:0	Extra horizontal initial factor 3.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_4[7:0]	7:0	Extra horizontal initial factor 4.	

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XVYCC Register (Bank = 102F, Sub-bank = 65)

XVYCC Register (Bank = 102F, sub-bank = 65)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	-	3:0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post r channel offset.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post g channel offset.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post b channel offset.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post r channel gain.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F48h'.	

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XVYCC Register (Bank = 102F, sub-bank = 65)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post g channel gain.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post b channel gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post r channel offset.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_BRI_OFFSET[7:0]	7:0	Sub window post g channel offset.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_BRI_OFFSET[7:0]	7:0	Sub window post b channel offset.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post r channel gain.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post g channel gain.	
2Bh	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**

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XVYCC Register (Bank = 102F, sub-bank = 65)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F57h)	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post b channel gain.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '102F58h'.	

VOP2_RP Register (Bank = 102F, Sub-bank = 6D)

VOP2_RP Register (Bank = 102F, sub-bank = 6D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_ST[7:0]	7:0	For osd reference hs start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_NEW_REF	7	Osd new reference hs/vfde enable.	
	-	6:5	Reserved.	
	OSD_HS_ST[12:8]	4:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_END[7:0]	7:0	For osd reference hs end.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OSD_HS_END[12:8]	4:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_ST[7:0]	7:0	For osd reference vfde start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_VFDE_ST[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_END[7:0]	7:0	For osd reference vfde end.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_VFDE_END[11:8]	3:0	See description of '102F26h'.	

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GOP_INT Register (Bank = 102F, Sub-bank = 80)

GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102F00h)	**REG102F00**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler.	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]: SWRST1[4]: IP, include F1 and F2. SWRST1[3]: OP include OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_MCLK_ON	7	Clk_miu enable.	
	-	6:2	Reserved.	
	PDMD[1:0]	1:0	PowerDown mode: 01: IDCLK. Others: IDCLK and ODCLK.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x10**	**Access : R/W**
	GCLK_MD[7:0]	7:0	PowerDown control: [1]: Live Fclk gated enable. [4]: Fclk gated control.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.	

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	COP_EN	7	Enable cop for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO**

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F20h)	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
13h	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F27h)	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Eh)	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**

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GOP_INT Register (Bank = 102F, sub-bank = 80)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F47h)	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '102F48h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0xE1**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

IP1_M Register (Bank = 102F, Sub-bank = 81)

IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F1Ah)	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F1Fh)	DUMMY0F_8_15[7:0]	7:0		
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. #0: Left result. #1: right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. #0: Not clear. #1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. #0: Update every frame. #1: Keep the history value.	
	JITTER	3	JITTER function Result. #0: No JITTER. #1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. #0: Update every frame. #1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. #0: Result not ready. #1: Result ready.	
	ATS_EN	0	Auto position function Enable. #0: Disable. #1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	THOLD[3:0]	7:4	Auto position Valid Data Value. #0000: Valid if data >= 0000 0000. #0001: Valid if data >= 0001 0000. #0010: Valid if data >= 0010 0000. .. #1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Positoin Force Pixel Mode. #0 : DE or Pixel decide by the Source. #1 : Force Pixel Mode.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Aoto Gain Value. (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F35h)	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Ch)	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Eh)	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh	**REG102F5C**	**7:0**	**Default : 0x01**	**Access : R/W**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F5Ch)	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. #0: Can gate the GOP clock. #1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. #0: Don't gate the idclk. #1: Can gate the idclk.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATS_B_SKIP	2	Auto search ignore B data.	
	ATS_G_SKIP	1	Auto search ignore G data.	
	ATS_R_SKIP	0	Auto search ignore R data.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DE_BYPASS_MODE	7	Use input DE to replace SPRange_H as output DE.	
	-	6:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F65h)	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Bh)	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Atuto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	
40h ~ 43h (102F80h ~ 102F86h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FDET_STATUS_INTLAC_DET0	0	Mode detect result 0.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	

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IP1_M Register (Bank = 102F, sub-bank = 81)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	

IP2_M Register (Bank = 102F, Sub-bank = 82)

IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	PREV_DOWN_3D	4	PREV_DOWN_3D.	
	-	3:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x08**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	
	YDELAY_EN	4	Y delay enable.	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	44TO42_DITH_EN	0	444 to 422 filter dith enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FILL_BLACK_NUM[5:0]	5:0	Fill black number.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILL_BLACK_ACT	7	FILL_BLACK_ACT.	
	FILL_BLACK_CLR	6	Clear fill_black register manually.	
	-	5:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_HSK_MD	5	Ip2 osd handshaking mode.	
	FORCE_OSD_HSK	4	Force ip2 to osd in handshaking mode.	
	-	3	Reserved.	
	IP2_VS_SEL	2	1: Use mvop_vs to generate vs to opvs 0:use ip1_vs to generate vs to opvs.	
	FORCE_PRE2LAST	1	1: Use vsd last valid as pre align 0: use original pre align.	
	MVOP_DIN_EN	0	1: Data is form mvop 0: form yc delay.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RANDOM_SEL[1:0]	5:4	//random mode 0:1 1:3/4 2:1/2 3:1/4 rdy.	
	ALTIVE_LINE	3	//1: use chessboard data 0:use non line altive data;	
	CHESS_EN	2	//1: use chessboard data 0:use nomo data;	
	PAT_DATA_SEL	1	//1: use patgen data 0:use input data;	
	PAT_TIMING_SEL	0	//1: use patgen timing 1:use input timing;	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0xD0**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen h total.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0xE0**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen v total.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x40**	**Access : R/W**
	H_BLOCK[7:0]	7:0	Patgen h block.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen v block.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	V_BLOCK[9:8]	1:0	See description of '102F28h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xF2**	**Access : R/W**
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x1F**	**Access : R/W**
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x5E**	**Access : R/W**
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xF4**	**Access : R/W**
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x0C**	**Access : R/W**
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x5A**	**Access : R/W**
	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x37**	**Access : R/W**
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0xF5**	**Access : R/W**
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y0. Format: S7 of 2's complement (-15 <= Y0 <= 15).	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
21h	**REG102F42**	**7:0**	**Default : 0x4B**	**Access : R/W**

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F42h)	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 127).	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x17**	**Access : R/W**
	HSD_CT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_CT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x0B**	**Access : R/W**
	HSD_CT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_CT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x29**	**Access : R/W**
	HSD_CT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C3. Format: Fix 8 (0 <= C3 <= 255).	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x01**	**Access : R/W**
	HSD_CT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C4. Format: S7 of 2's complement (-63 <= C4 <= + 63).	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x04**	**Access : R/W**
	HSD_CT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x3C**	**Access : R/W**
	HSD_CT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C2. Format: Fix 8 (0 <= C2 <= 127).	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:0	Reserved.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IP2DIP_SEL	0	IP2 to DIP source select: 1'b0: before HSD/VSD. 1'b1: after HSD/VSD.	
2Dh	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F5Ah)	-	7:3	Reserved.	
	IP2VE_VS_SEL	2	IP to VE vsync selection. 1'b0: IP1 vsync. 1'b1: original vsync.	
	IP2VE_CAP_EN	1	IP to VE cap enable.	
	IP2VE_PATH_EN	0	IP to VE enable.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2VE_HBLANK[3:0]	7:4	IP to VE H-blanking length.	
	IP2VE_RATE[3:0]	3:0	IP to VE flow control.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIN_CTRL_EN	7	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	6	IP2 VSD input line count number setting enable.	
	-	5	Reserved.	
	VSD_IN_NUM_USR[12:8]	4:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VOUT_CTRL_EN	7	IP2 VSD output line count control enable.	
	-	6:5	Reserved.	
	VSD_OUT_NUMBER[12:8]	4:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_USR_VACT_VIDEO[7:0]	7:0	VSD user mode v_active region.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_USR_VACT_VIDEO_EN	7	VSD user mode v_active region enable.	
	-	6:5	Reserved.	
	VSD_USR_VACT_VIDEO[12:8]	4:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	VSD_VACT_VIDEO_READ[7:0]	7:0	VSD user mode v_active region.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	VSD_VACT_VIDEO_READ[12:8]	4:0	See description of '102F72h'.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_HSD_OUT_CNT[12:8]	4:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_VSD_OUT_CNT[12:8]	4:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PREFLT_ALPHA_EN	7	IP2 Pre-Filter alpha blending enable.	
	-	6:5	Reserved.	
	PREFLT_ALPHA[4:0]	4:0	IP2 Pre-Filter alpha blending for original and filter.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_Y_TAP0[3:0]	3:0	IP2 Pre-Filter coefficient 0 [s.3] (T8).	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_FILTER_EN	7	IP2 Pre-Filter enable.	
	FIR_DITH_EN	6	IP2 Pre-Filter dith enable.	
	-	5:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP1[6:0]	6:0	IP2 Pre-Filter coefficient 1 [s.6] (T8).	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP2[6:0]	6:0	IP2 Pre-Filter coefficient 2 [s.6] (T8).	
4Bh	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F96h)	PRE_Y_TAP3[7:0]	7:0	IP2 Pre-Filter coefficient 3 [s.7] (T8).	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP4[7:0]	7:0	IP2 Pre-Filter coefficient 4 [s.8] (T8).	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PRE_Y_TAP4[8]	0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP5[7:0]	7:0	IP2 Pre-Filter coefficient 5 [s.9] (T8).	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP5[9:8]	1:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP6[7:0]	7:0	IP2 Pre-Filter coefficient 6 [0.10] (T8).	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP6[9:8]	1:0	See description of '102F9Ch'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FLT_MODE	0	In advance mode 0:use 4 phase blending 1: use 8 phase blending.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT3_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x0D**	**Access : R/W**
	HSD_YT3_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x5C**	**Access : R/W**
	HSD_YT3_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x23**	**Access : R/W**
	HSD_YT3_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
55h	**REG102FAA**	**7:0**	**Default : 0xF7**	**Access : R/W**

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FAAh)	HSD_YT3_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x03**	**Access : R/W**
	HSD_YT3_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_YT4_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x3B**	**Access : R/W**
	HSD_YT4_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT4_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_YT4_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GOP_REQ_CNT[4:0]	4:0	In mvop handshake mode, gen gop needs timing.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2GOP_SRC_SEL	7	For GOPD src of ip2 0: IP2IN 1:IP2OUT.	
	-	6:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable bpseudo blanking.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x08**	**Access : R/W**
	LB_SPLIT_BLANK[7:0]	7:0	LB pseudo blank cycle.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x18**	**Access : R/W**
	PRE_ADJ_SPLIT_BLANK[7:0]	7:0	Adj pseudo blank cycle.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EXT_LR_EN	4	Enable external lr signal.	
	-	3:1	Reserved.	
	INIT_3D_STAT	0	Initialize 3d stat.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	WAIT_LEFT_FRM_INV	5	Reg_wait_right_frm.	
	WAIT_LEFT_FRM	4	WAIT_LEFT_FRM.	
	-	3:1	Reserved.	
	EXT_LR_INV	0	Inverse external lr signal.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	INI_LR_IDX	4	0: L is the first frame 1: R is the first frame.	
	-	3	Reserved.	
	ADJ_FORCE_EN	2	Adj bypass enable.	
	LR_CHG_MODE[1:0]	1:0	0: Line 1:block 2:frame.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAX_LOOP[2:0]	6:4	3d mode setting.	
	-	3:1	Reserved.	
	SPLIT_HALF	0	Split 1 frame into 2 frame.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VACT_SPC_EN[1:0]	5:4	3d mode setting.	
	-	3	Reserved.	
	MASK_EN[2:0]	2:0	3d mode setting.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GEN_VS_ACT[3:0]	7:4	Enable gen pseudo vsync in 3d.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GEN_VS_EN[3:0]	3:0	Enable gen pseudo vsync in 3d.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_VIDEO[7:0]	7:0	V_active region.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_VIDEO[12:8]	4:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_0[7:0]	7:0	V blanking between field1&field2 or field3&field4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_0[12:8]	4:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_1[7:0]	7:0	V blanking between field2&field3.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_1[12:8]	4:0	See description of '102FCEh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0xC0**	**Access : R/W**
	LB_AUTO	7	LB_AUTO.	
	VSD_FAC_AUTO_RST_EN	6	VSD 3d auto factor reset mode enable.	
	AUTO_VACT_VIDEO_RST	5	AUTO vact_video mode reset.	
	-	4:0	Reserved.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable dat_adj to src force ready.	
	ADJ_AUTO	0	ADJ_AUTO.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[7:0]	7:0	Debug.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_DIFF[7:0]	7:0	Number of fifo.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LR_ALT_LINE	2	LR_ALT_LINE.	
	LR_FST_PIX	1	LR_FST_PIX.	
	PIX_SEP_EN	0	PIX_SEP_EN.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HALF_PIX[7:0]	7:0	IP2 separation half pix number in user mode.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	HALF_PIX_USR_EN	7	IP2 separation user mode.	
	-	6:3	Reserved.	
	HALF_PIX[10:8]	2:0	See description of '102FD8h'.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSP_PH0_COEF0[7:0]	7:0	RSP_PH0_COEF0.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x80**	**Access : R/W**
	RSP_PH0_COEF1[7:0]	7:0	RSP_PH0_COEF1.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSP_PH1_COEF0[7:0]	7:0	RSP_PH1_COEF0.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x40**	**Access : R/W**
	RSP_PH1_COEF1[7:0]	7:0	RSP_PH1_COEF1.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RSP_LINE7_PH	7	RSP_LINE7_PH.	
	RSP_LINE6_PH	6	RSP_LINE6_PH.	
	RSP_LINE5_PH	5	RSP_LINE5_PH.	
	RSP_LINE4_PH	4	RSP_LINE4_PH.	
	RSP_LINE3_PH	3	RSP_LINE3_PH.	
	RSP_LINE2_PH	2	RSP_LINE2_PH.	
	RSP_LINE1_PH	1	RSP_LINE1_PH.	
	RSP_LINE0_PH	0	RSP_LINE0_PH.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RSP_FIELD_USR_EN	6	Re-sample local toggle field flag.	
	RSP_FIELD_INV	5	Re-sample field polarity invert.	

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IP2_M Register (Bank = 102F, sub-bank = 82)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RSP_FIELD_EN	4	Re-sample field mode.	
	-	3:1	Reserved.	
	RESAMP_EN	0	RESAMP_EN.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_CLR[7:0]	7:0	DUMMY_CLR.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_CLR[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[7:0]	7:0	DUMMY_SET.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[15:8]	7:0	See description of '102FFEh'.	

PNR Register (Bank = 102F, Sub-bank = 85)

PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F1	7	Sub Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F1	6	Sub Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F1	5	Sub Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F1	4	Sub Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F1	3	Sub Window Post Noise Reduction for Y.	
	PNR_ENC_F1	2	Sub Window Post Noise Reduction for C.	
	RATIOYC_F1[1:0]	1:0	Sub Window Motion Ratio.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F1	0	Sub Window select next field inverter for noc_sel.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F1	7	Sub Window DHD 3f mode enable.	
	PCCS_3F_EN_F1	6	Sub Window PCCS 3f mode enable.	
	-	5	Reserved.	

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PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PCCS_DITHER_EN_F1	4	Sub Window PCCS dither enable.	
	DHD_DITHER_EN_F1	3	Sub Window DHD dither enable.	
	PNR_BYPASS_F1	2	Sub Window PNR function bypass enable.	
	NR_EN_F1	1	Sub Window Post NR enable.	
	PCCS_EN_F1	0	Sub Window Post CCS enable.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PAL_EN_F1	6	Sub Window PAL enable.	
	-	5:0	Reserved.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F1[2:0]	7:5	Sub Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F1[2:0]	4:2	Sub Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F1	1	Sub Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F1	0	Sub Window user-defined Y motion threshold enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F1	6	Sub Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F1	5	Sub Window enable select max motion for c.	
	YMOT_MAX_SEL_F1	4	Sub Window enable select max motion for y.	
	CMOT_DIV_MODE_F1[1:0]	3:2	Sub Window C motion divide mode.	
	YMOT_DIV_MODE_F1[1:0]	1:0	Sub Window Y motion divide mode.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DITHER_FRAME_RST_CNT[1:0]	2:1	Dither frame reset count.	
	DITHER_FRAME_RST_EN	0	Dither frame reset enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	

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PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_F2[1:0]	1:0	Main Wimdow Motion Ratio.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for noc_sel.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F2	7	Main Window DHD 3f mode enable.	
	PCCS_3F_EN_F2	6	Main Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F2	4	Main Window PCCS dither enable.	
	DHD_DITHER_EN_F2	3	Main Window DHD dither enable.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PAL_EN_F2	6	Main Window PAL enable.	
	-	5:0	Reserved.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F2	5	Main Window DHD Interleaved History MR invert.	

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PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_HMR_INT_EN_F2	4	Main Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F2	3	Main Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F2	2	Main Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F2	1	Main Window DHD YMR02 enable.	
	DHD_EN_F2	0	Main Window DHD enable.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F1	5	Sub Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F1	4	Sub Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F1	3	Sub Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F1	2	Sub Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F1	1	Sub Window DHD YMR02 enable.	
	DHD_EN_F1	0	Sub Window DHD enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR02_TH[5:0]	5:0	DHD YMR02 threshold.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR02_GAIN[2:0]	2:0	DHD YMR02 gain.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR04_TH[5:0]	5:0	DHD YMR04 threshold.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR04_GAIN[2:0]	2:0	DHD YMR04 gain.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_CVAL_GAIN[7:0]	7:0	DHD C value gain.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_DIFFPIX_GAIN[3:0]	3:0	DHD pixel diff gain.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR02_TH[5:0]	5:0	DHD C motion02 threshold.	

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PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR02_GAIN[2:0]	2:0	DHD C motion02 gain.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR04_TH[5:0]	5:0	DHD C motion04 threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR04_GAIN[2:0]	2:0	DHD C motion04 gain.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x30**	**Access : R/W**
	DHD_CEDGE_GAIN[7:0]	7:0	DHD C edge gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_YEDGE_GAIN[7:0]	7:0	DHD Y edge gain.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_DEBUG0_EN	7	DHD debug0 enable.	
	DHD_DEBUG1_EN	6	DHD debug1 enable.	
	-	5:0	Reserved.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_YMR_IIR_ALPHA[2:0]	6:4	DHD YMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_YMR_IIR_STEP[1:0]	1:0	DHD YMR IIR step.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_CMR_IIR_ALPHA[2:0]	6:4	DHD CMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_CMR_IIR_STEP[1:0]	1:0	DHD CMR IIR step.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_CEDGE_TH[3:0]	3:0	DHD C edge threshold.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YEDGE_TH[5:0]	5:0	DHD Y edge threshold.	

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PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_CVAL_TH[3:0]	3:0	DHD C value threshold.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INV_SAT_OFFSET[6:0]	6:0	PCCS invert saturation offset.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INV_SAT_POWNUM[2:0]	6:4	PCCS invert saturation pownum.	
	INV_SAT_W[3:0]	3:0	PCCS invert saturation weight.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TDELTA_C_POWNUM[3:0]	7:4	PCCS inv-saturation delta pownum.	
	TDELTA_C_W[3:0]	3:0	PCCS inv-saturation delta weight.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS Y Fn Fn-2 coring threshold.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS Y Fn Fn-2 pre wieght.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS Y Fn Fn-2 post pownum.	
	-	3	Reserved.	
	YDIFF_FNFN2_POST_W[2:0]	2:0	PCCS Y Fn Fn-2 post wieght.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-2 coring threshold.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS C Fn Fn-2 pre wieght.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-2 post pownum.	

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PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3	Reserved.	
	CDIFF_FNFN2_POST_W[2:0]	2:0	PCCS C Fn Fn-2 post wieght.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RC_EV_POWNUM[2:0]	6:4	PCCS real color edge value pownum.	
	RC_EV_W[3:0]	3:0	PCCS real color edge value weight.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCMODIFYFAC_POWNUM[3:0]	7:4	PCCS cross color edge value pownum.	
	CCMODIFYFAC_W[3:0]	3:0	PCCS cross color edge value weight.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	YEDGEFAC_UP_OFFSET[7:0]	7:0	PCCS Y edge offset.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YEDGEFAC_POWNUM[2:0]	6:4	PCCS Y edge pownum.	
	YEDGEFAC_W[3:0]	3:0	PCCS Y edge weight.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BLEND_LPF_TURN_OFF	1	PCCS factor low-pass filter off.	
	MEDIAN_TURN_OFF	0	PCCS factor median filter off.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INV_CDIFF_FNFN2_POWNUM[3:0]	7:4	PCCS invert C Fn Fn-2 diff pownum.	
	INV_CDIFF_FNFN2_W[3:0]	3:0	PCCS invert C Fn Fn-2 diff weight.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-4 diff threshold.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN4_PRE_W[2:0]	2:0	PCCS C Fn Fn-4 diff pre weight.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-4 diff post pownu,	
	-	3	Reserved.	
	CDIFF_FNFN4_POST_W[2:0]	2:0	PCCS C Fn Fn-4 diff post weight.	

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PNR Register (Bank = 102F, sub-bank = 85)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDIFF_3F_POST_POWNUM[2:0]	6:4	PCCS Y 3F diff post pownum.	
	-	3	Reserved.	
	YDIFF_3F_POST_W[2:0]	2:0	PCCS Y 3F diff post weight.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[7:0]	7:0	PCCS Table.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[15:8]	7:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[23:16]	7:0	See description of '102FC0h'.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[31:24]	7:0	See description of '102FC0h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[39:32]	7:0	See description of '102FC0h'.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[47:40]	7:0	See description of '102FC0h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[55:48]	7:0	See description of '102FC0h'.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE[63:56]	7:0	See description of '102FC0h'.	

DNR Register (Bank = 102F, Sub-bank = 86)

DNR Register (Bank = 102F, sub-bank = 86)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	F2_MR_SOURCE_NRY	4	F2 Motion Source Cur Select. #0 : cur after NR. #1 : cur non-NR.	
	-	3:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	

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DNR Register (Bank = 102F, sub-bank = 86)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.	
	F2_SNR_EN	0	F2 SNR FUNCTION EN.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	F2_NR_ROUND_BIT_C	5	Set C_ROUND described as above.	
	F2_NR_ROUND_BIT_Y	4	Set Y_ROUND described as above.	
	-	3:0	Reserved.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	F2_MOTION_PRE_SHIFT_C[1:0]	6:5	F2_MOTION_PRE_SHIFT_C.	
	-	4	Reserved.	
	F2_MOTION_PRE_SHIFT_Y[1:0]	3:2	F2_MOTION_PRE_SHIFT_Y.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	F2_DNR_LPF_C_EN	6	F2_DNR_LPF_C_EN.	
	-	5	Reserved.	
	F2_DNR_LPF_Y_EN	4	F2_DNR_LPF_Y_EN.	
	-	3:0	Reserved.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	F2_SHARP_LEVEL[2:0]	2:0	F2 SNR sharpness level.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_POW_NUM[2:0]	2:0	F2 SNR power number.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h	**REG102F82**	**7:0**	**Default : 0x56**	**Access : R/W**

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DNR Register (Bank = 102F, sub-bank = 86)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F82h)	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x08**	**Access : R/W**
	RESERVED_TABLE_0[7:0]	7:0	Reserved.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x18**	**Access : R/W**
	RESERVED_TABLE_0[15:8]	7:0	See description of '102FE8h'.	

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FILM Register (Bank = 102F, Sub-bank = 8A)

FILM Register (Bank = 102F, sub-bank = 8A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7	Reserved.	
	DET_FIELD_SEL_LC	6	DET_FIELD_SEL_LC.	
	-	5	Reserved.	
	DIFF_TH[12:8]	4:0	Difference threshold.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_CUR_ERROR_TH_F2[7:0]	7:0	32 current error threshold.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_PRE_ERROR_TH_F2[15:8]	7:0	32 previous error threshold.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_CUR_ERROR_TH_F2[7:0]	7:0	22 current error threshold.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_PRE_ERROR_TH_F2[15:8]	7:0	22 previous error threshold.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	32_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	32 total error max th.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x7F**	**Access : R/W**
	32_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	32 total error sum th.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x08**	**Access : R/W**
	22_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	22 total error max th.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x7F**	**Access : R/W**
	22_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	22 total error sum th.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	FIX_DIFF_TH[12:8]	4:0	Cur error sum th.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[7:0]	7:0	F2 counter 1 threshold.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[7:0]	7:0	F2 counter 3 threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[15:8]	7:0	See description of '102F1Ah'.	

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FILM Register (Bank = 102F, sub-bank = 8A)

Index (Absolute)	Mnemonic	Bit	Description	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[7:0]	7:0	F2 counter fix threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[15:8]	7:0	See description of '102F1Ch'.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x30**	**Access : R/W**
	FILM32_EN_F2	7	F2 32 film mode enable.	
	FILM22_EN_F2	6	F2 22 film mode enable.	
	-	5:4	Reserved.	
	PRE32_F2	3	F2 pre32.	
	-	2:0	Reserved.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xEE**	**Access : R/W**
	MOT_TH_PATCH_F2[7:4]	7:4	F2 patch motion threshold.	
	FM_MOT_PIXTH_F2[3:0]	3:0	F2 motion ratio threshold.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x14**	**Access : R/W**
	FM_MOT_CNTTH_F2[15:8]	7:0	F2 unmatch threshold.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FILM32_N1_EN_F2	7	F2 N1 film32 enable.	
	FILM22_N1_EN_F2	6	F2 N1 film22 enable.	
	-	5:0	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[7:0]	7:0	F2 read status.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[15:8]	7:0	See description of '102F30h'.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[7:0]	7:0	F2 patch read status.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[15:8]	7:0	See description of '102F34h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x50**	**Access : R/W**
	MULT_COEF_F2[7:4]	7:4	F2 multiplicant ratio.	
	-	3:1	Reserved.	
	RELATIVE_FM_EN_F2	0	F2 relative film mode frame diff enable.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x05**	**Access : R/W**
	LOWER_BOUND_FM_32_F2[15:8]	7:0	F2 frame diff lower bound.	

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FILM Register (Bank = 102F, sub-bank = 8A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[7:0]	7:0	F2 frame diff upper bound.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x03**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x0F**	**Access : R/W**
	CHECK_SEQ_F2[7:0]	7:0	F2 lock threshold to enter 22.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x44**	**Access : R/W**
	SPEEDUP_STEP_F2[7:4]	7:4	F2 speedup step.	
	SPEEDUP_SHIFT_F2[3:0]	3:0	F2 speedup shift value.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x80**	**Access : R/W**
	SPEEDUP_EN_F2	7	F2 speedup enable.	
	-	6:0	Reserved.	

SNR Register (Bank = 102F, Sub-bank = 8C)

SNR Register (Bank = 102F, sub-bank = 8C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SNR_EN_F1	4	SNR enable F1.	
	-	3	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F2	2	De-blocking and SNR active threshold motion ratio enable F2.	
	SNR_MOTION_RATIO_EN_F2	1	SNR motion ratio enable F2.	
	SNR_EN_F2	0	SNR enable F2.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x48**	**Access : R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	-	4	Reserved.	
	SNR_STRENGTH_GAIN_F2[3:0]	3:0	SNR strength F2.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0xCF**	**Access : R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	

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SNR Register (Bank = 102F, sub-bank = 8C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x69**	**Access : R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x24**	**Access : R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x01**	**Access : R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_NM_DITHER_EN	7	Noise masking dither enable.	
	-	6:5	Reserved.	
	SNR_NM_FILTER_EN_F1	4	Noise masking enable F1.	
	-	3:2	Reserved.	
	SNR_NM_MOTION_RATIO_EN_F2	1	Noise masking motion ratio enable F2.	
	SNR_NM_FILTER_EN_F2	0	Noise masking enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_15[1:0]	7:6	Reserved.	
	-	5:0	Reserved.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SNR_MR_LPF_EN_F2	0	De-blocking and SNR motion ratio low pass filter enable F2 (lpf is 3x3 mask).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_9[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F2[5:0]	5:0	Noise masking gain F2.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_10[1:0]	7:6	Reserved.	

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SNR Register (Bank = 102F, sub-bank = 8C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:0	Reserved.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SNR_NM_MIN_THRD[3:0]	7:4	Noise masking min threshold bound.	
	SNR_NM_MAX_THRD[3:0]	3:0	Noise masking max threshold bound.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_01[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_01.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_23[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_23.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_45[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_45.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_67[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_67.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_89[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_89.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_AB[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_AB.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_CD[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_CD.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_EF[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_EF.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_MOTION_TABLE_01[7:0]	7:0	SNR motion ratio LUT_01.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_MOTION_TABLE_23[7:0]	7:0	SNR motion ratio LUT_23.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_MOTION_TABLE_45[7:0]	7:0	SNR motion ratio LUT_45.	

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SNR Register (Bank = 102F, sub-bank = 8C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_MOTION_TABLE_67[7:0]	7:0	SNR motion ratio LUT_67.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_MOTION_TABLE_89[7:0]	7:0	SNR motion ratio LUT_89.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_MOTION_TABLE_AB[7:0]	7:0	SNR motion ratio LUT_AB.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_MOTION_TABLE_CD[7:0]	7:0	SNR motion ratio LUT_CD.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_MOTION_TABLE_EF[7:0]	7:0	SNR motion ratio LUT_EF.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_NM_MOTION_TABLE_01[7:0]	7:0	Noise masking motion ratio LUT_01.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_NM_MOTION_TABLE_23[7:0]	7:0	Noise masking motion ratio LUT_23.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_NM_MOTION_TABLE_45[7:0]	7:0	Noise masking motion ratio LUT_45.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_NM_MOTION_TABLE_67[7:0]	7:0	Noise masking motion ratio LUT_67.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_NM_MOTION_TABLE_89[7:0]	7:0	Noise masking motion ratio LUT_89.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_NM_MOTION_TABLE_AB[7:0]	7:0	Noise masking motion ratio LUT_AB.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_NM_MOTION_TABLE_CD[7:0]	7:0	Noise masking motion ratio LUT_CD.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_NM_MOTION_TABLE_EF[7:0]	7:0	Noise masking motion ratio LUT_EF.	

HISDNR Register (Bank = 102F, Sub-bank = 8E)

HISDNR Register (Bank = 102F, sub-bank = 8E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h	**REG102F02**	**7:0**	**Default : 0xC0**	**Access : R/W**

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HISDNR Register (Bank = 102F, sub-bank = 8E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F02h)	FM_HIS_H_RANGE_EN	7	Frame Histogram Report Define H Range Enable.	
	FM_HIS_RANGE_EN	6	Frame Histogram Report Define Range Enable.	
	-	5	Reserved.	
	DNR_USE_HISDNR_EN	4	DNR Function Use Hisdnr Enable.	
	-	3:2	Reserved.	
	PSNR_EN	1	PSNR Enable.	
	HISDNR_EN	0	HISDNR enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x0D**	**Access : R/W**
	_	7:1	Reserved.	
	FM_HIS_V_RANGE_EN	0	Frame Histogram Report Define V Range Enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x2C**	**Access : R/W**
	HISDNR_MD_ADJUST_LEVEL_0123[3:0]	7:4	Motion difference adjust level 0123: 0.5 format.	
	MD_ADJUST_SHIFT	3	Motion difference adjust shift.	
	HISMATCH_BIT[2:0]	2:0	Histogram matching result shift bits(0 to 7).	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FM_HIS_STD_THRD[7:0]	7:0	Frame Histogram STD Threshold.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:2	Reserved.	
	HISDNR_HISMATCH_STEP_LEVEL_0123[1:0]	1:0	Histogram matching step 0123.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x80**	**Access : R/W**
	HISDNR_HISMATCH_THRD_LEVEL_0123[7:0]	7:0	Histogram matching threshold 0123.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HISDNR_STD_THRD_LEVEL_0123[3:0]	7:4	Standard Deviation threshold 0123.	
	-	3:2	Reserved.	
	HISDNR_STD_STEP_LEVEL_0123[1:0]	1:0	Standard Deviation step 0123.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x12**	**Access : R/W**
	_	7:6	Reserved.	
	HISDNR_STRENGTH_GAIN[5:0]	5:0	HISDNR strength gain 2.4 format.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_1[7:0]	7:0	Frame motion histogram report section 1.	

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HISDNR Register (Bank = 102F, sub-bank = 8E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_1[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_2[7:0]	7:0	Frame motion histogram report section 2.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_2[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_3[7:0]	7:0	Frame motion histogram report section 3.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_3[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_4[7:0]	7:0	Frame motion histogram report section 4.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_4[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_5[7:0]	7:0	Frame motion histogram report section 5.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_5[15:8]	7:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_6[7:0]	7:0	Frame motion histogram report section 6.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_6[15:8]	7:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_7[7:0]	7:0	Frame motion histogram report section 7.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_7[15:8]	7:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_8[7:0]	7:0	Frame motion histogram report section 8.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_8[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_9[7:0]	7:0	Frame motion histogram report section 9.	
0Dh	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : RO**

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HISDNR Register (Bank = 102F, sub-bank = 8E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F1Bh)	FM_HIS_16_9[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_31[7:0]	7:0	Frame motion histogram report section 31.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_HIS_16_31[15:8]	7:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_0[7:0]	7:0	Normalized frame motion histogram section 0.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_0[8]	0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_1[7:0]	7:0	Normalized frame motion histogram section 1.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_1[8]	0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_2[7:0]	7:0	Normalized frame motion histogram section 2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_2[8]	0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_3[7:0]	7:0	Normalized frame motion histogram section 3.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_3[8]	0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_4[7:0]	7:0	Normalized frame motion histogram section 4.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_4[8]	0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_5[7:0]	7:0	Normalized frame motion histogram section 5.	
14h	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**

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HISDNR Register (Bank = 102F, sub-bank = 8E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F29h)	-	7:1	Reserved.	
	NFM_HIS_16_5[8]	0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_6[7:0]	7:0	Normalized frame motion histogram section 6.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_6[8]	0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFM_HIS_16_7[7:0]	7:0	Normalized frame motion histogram section 7.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_7[8]	0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:6	Reserved.	
	PSNR_STRENGTH_GAIN[5:0]	5:0	PSNR strength gain: 2.4 format.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	PSNR_MH_BS[1:0]	1:0	PSNR motion history shift bits(0 to 7).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	PSNR_STD_STEP_LEVEL_0123[1:0]	1:0	PSNR Standard Deviation step 0123.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x13**	**Access : R/W**
	PSNR_STD_THRD_LEVEL_0123[7:0]	7:0	PSNR STD threshold 0123.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	FM_HIS_H_ST[7:0]	7:0	Frame Histogram Report H Range Start.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x5B**	**Access : R/W**
	FM_HIS_H_END[7:0]	7:0	Frame Histogram Report H Range End.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x01**	**Access : R/W**
	FM_HIS_V_ST[7:0]	7:0	Frame Histogram Report V Range Start.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x1D**	**Access : R/W**
	FM_HIS_V_END[7:0]	7:0	Frame Histogram Report V Range End.	
1Bh	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**

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HISDNR Register (Bank = 102F, sub-bank = 8E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F36h)	FM_LUMA_SUM[7:0]	7:0	Total luma sum for assigned window: 16MSBs of 30 bit total sum.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	FM_LUMA_SUM[15:8]	7:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_0[7:0]	7:0	Frame motion matching histogram report section 0.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_0[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_1[7:0]	7:0	Frame motion matching histogram report section 1.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_1[15:8]	7:0	See description of '102F3Ah'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_2[7:0]	7:0	Frame motion matching histogram report section 2.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_2[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_3[7:0]	7:0	Frame motion matching histogram report section 3.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_3[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_4[7:0]	7:0	Frame motion matching histogram report section 4.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_4[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_5[7:0]	7:0	Frame motion matching histogram report section 5.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_5[15:8]	7:0	See description of '102F44h'.	

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HISDNR Register (Bank = 102F, sub-bank = 8E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_6[7:0]	7:0	Frame motion matching histogram report section 6.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_6[15:8]	7:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_7[7:0]	7:0	Frame motion matching histogram report section 7.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	MAT_FM_HIS_16_7[15:8]	7:0	See description of '102F48h'.	

S_VOP Register (Bank = 102F, Sub-bank = 8F)

S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO_BO[3:0]	7:4	Main windowborder outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	
	-	3:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F13h)	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '102F1Eh'.	
10h	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F20h)	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	S_VDEEND_4TH[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
1Dh	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Bh)	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F46h'.	
24h	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F48h)	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SMEN	7	SVM Main window Enable.	
	SMTE	6	SVM Main window Tap Enable.	
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SSWEN	3	SVM Sub window Enable.	
	SSWETE	2	SVM Sub window Tap Enable.	
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.	
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.	
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data. 11: Y with tap filter.	
	SCORING[3:0]	3:0	SVM Coring.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	-	4:2	Reserved.	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	
	-	5:4	Reserved.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	RESERVED[1:0]	6:5	RESERVED.	
	-	4:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (bri_function) for main window R.	
36h	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Dh)	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (bri_function) for main window G.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (bri_function) for main window B.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_R[7:0]	7:0	Brightness offset (bri_function) for sub window R.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (bri_function) for sub window G.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (bri_function) for sub window B.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.	
3Ch	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F79h)	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '102F82h'.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h ~ 45h (102F84h ~ 102F8Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CAP_STAGE	4	Capture stage selection. 0: Before osd. 1: After osd.	
	-	3:0	Reserved.	
46h (102F8Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102FA2h'.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FREEZ_VCNT_VALUE[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when REG_NEW_LOCK_POINT is set high.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LOCK_VCNT_VALUE[11:8]	3:0	See description of '102FAAh'.	
56h	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FACh)	-	7	Reserved.	
	PSEUDO_VS_EN	6	Enable pseudo vsync for freeze region.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select insert_end point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	
58h	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB0h)	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_MAIN_R_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_R_MIN_LIMIT. REG_MAIN_R_MIN_SIGN = 0: MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_MAIN_G_MIN_SIGN = 1: MAIN_G_MIN = -MAIN_G_MIN_LIMIT. REG_MAIN_G_MIN_SIGN = 0: MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_MAIN_B_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_B_MIN_LIMIT. REG_MAIN_B_MIN_SIGN = 0: MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value , s.12 format sign bit is bit-12. REG_SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. REG_SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_SUB_G_MIN_SIGN = 1: MAIN_G_MIN = -SUB_G_MIN_LIMIT. REG_SUB_G_MIN_SIGN = 0: MAIN_G_MIN = SUB_G_MIN_LIMIT.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_SUB_B_MIN_SIGN = 1: MAIN_R_MIN = -SUB_B_MIN_LIMIT. REG_SUB_B_MIN_SIGN = 0: MAIN_R_MIN = SUB_B_MIN_LIMIT.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '102FC6h'.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[7:0]	7:0	New add function for RGB_compression.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[15:8]	7:0	See description of '102FD8h'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FWC_SUB_EN	4		
	-	3:2	Reserved.	
	FWC_DITHER_EN	1		
	FWC_MAIN_EN	0		
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0		
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FWC_SLOPE[5:0]	5:0		
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	FWC_CTH[7:0]	7:0		
72h	**REG102FE4**	**7:0**	**Default : 0x80**	**Access : R/W**

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FE4h)	FWC_DELTA_R[7:0]	7:0		
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '102FE4h'.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '102FE4h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '102FE4h'.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[47:40]	7:0	See description of '102FE4h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '102FE4h'.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '102FE4h'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '102FE4h'.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '102FE4h'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '102FE4h'.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '102FE4h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[7:0]	7:0		
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '102FF4h'.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '102FF4h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '102FF4h'.	

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S_VOP Register (Bank = 102F, sub-bank = 8F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '102FF4h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '102FF4h'.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '102FF4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '102FF4h'.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '102FF4h'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '102FF4h'.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '102FF4h'.	

VOP Register (Bank = 102F, Sub-bank = 90)

VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated when DB_MASK and DB_LOAD.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSST1[7:0]	7:0	Output VSYNC start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VSST	4	Output VSYNC D[11]start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST1[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS=1). 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSEND[11:8]	3:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHST[7:0]	7:0	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHEND[7:0]	7:0	Output DE Horizontal END. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHEND[12:8]	4:0	See description of '102F0Ah'.	
06h	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Ch)	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVEND[7:0]	7:0	Output DE Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SIHST[12:8]	4:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SIHEND[12:8]	4:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	See description of '102F14h'.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVEND[7:0]	7:0	Scaling Image window Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVEND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HDTOT[12:8]	4:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VDTOT[11:8]	3:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x4C**	**Access : R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).	
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.	
	-	5:4	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels. 1: Disable, Output H Total is always odd pixels.	
	MOD2	2	Mode 2. 0: Disable. 1: Enable.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLLMD0	7	Frame PLL Mode 0.	
	SL_TUNE_EN	6	Short line tune enable.	
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.	
	-	4:2	Reserved.	
	SSC_SHIFT	1	0: Enable. 1: Disable.	
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x20**	**Access : R/W**
	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x08**	**Access : R/W**
	LCK_TH[15:8]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP Register Enable.	
	-	1	Reserved.	
	NOISY_GEN	0	Noise Generator.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT1[7:0]	7:0	Frame PLL Limit.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT0[7:0]	7:0	Frame PLL Limit.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT[7:0]	7:0	Frame PLL Limit.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : RO**
	INTLX_VS_OFFSET[7:0]	7:0	The interlace vsync offset.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLX_VS_EN	5	Interlace vsync enable.	
	INTLX_VS_OFFSET[12:8]	4:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	BY_STAGE_VIP[3:0]	7:4	Vip report point stage.	
	BY_STAGE_OP2[3:0]	3:0	Report point stage.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	REP_RD_TRID	0	Report SW read trigger.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SWBLBK	6	Sub window Blue screen color. 0: Black color. 1: Blue color.	
	SWBLUE	5	Sub window Blue screen control. 0: Off. 1: On.	
	-	4:3	Reserved.	
	MBD_EN	2	Main window Border Enable.	
	MBLK	1	Main window Black screen control. 0: Off. 1: On.	
	NOSC_EN	0	No Signal Color Enable.	
1Ah	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F34h)	FCL_G[7:0]	7:0	Frame Color - Green.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_B[7:0]	7:0	Frame Color - Blue.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_E_4_FRAME	7	Reset noise generator by frames enable.	
	NDMD	6	Noise Dithering Method.	
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.	
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.	
	DT3	3	Dither Type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.	
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma Write.	
	-	3:1	Reserved.	
	OUTFRR_EN0	0	Output Free-run Enable.	
1Dh (102F3Ah)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x07**	**Access : R/W**
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	-	6:0	Reserved.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_MD1	7	FPLL Mode 1.	
	FPLL_DIS	6	FPLL Stop.	
	-	5:3	Reserved.	
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.	
	-	1:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.	
	WHTS	5	White Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.	
	-	2:0	Reserved.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBLALL_SET	7	Frame buffer less all set.	
	-	6:0	Reserved.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCHBLEND	7	OSD Character Blending mode.	
	-	6	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4	Reserved.	
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0%% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	MNS_COL[7:0]	7:0	Main Window No Signal Color.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	-	6:0	Reserved.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F4Ch'.	
27h	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F4Eh)	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CM32[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FTPS_PRE	7	Front-TPSCR. For pre_osd_blending. 0: Disable. 1: Enable.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255.1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : RO**
	OVSSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error less than 29h/2Ah.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	OVERDESTAT	6	Output Vertical DE Status.	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	See description of '102F64h'.	
33h	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F66h)	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : RO**
	OHTSTAT1[7:0]	7:0	Output H Total Status.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	FRACST1[7:0]	7:0	Fraction Status.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FRACST2[2:0]	2:0	Fraction Status.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FRACST3[2:0]	2:0	Fraction Status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	HTTMGN[7:0]	7:0	H Total Margin.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSCMGN[7:0]	7:0	SSC Margin.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSTVALUE0[7:0]	7:0	Read Start initial value.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	RSTVALUE1[7:0]	7:0	Read Start Value.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read Start initial value.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read Start Value.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	INP8	7	This bit with REG_INE_DRV3 to enable G replace R and B for gamma mapping.	
	ONE_DRV3	6	Gamma use G replace R and B for gamma mapping.	
	GABYP	5	By pass gamma function.	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTDATA[7:0]	7:0	Reserved.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.	
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.	
42h (102F85h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	TFRACN[7:0]	7:0	Target Fraction Number. / Frame PLL limit RK[7:0].	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	PDP_MASK_EN	6	Reserved.	
	-	5	Reserved.	
	FX_PROT	4	Frame Change Protect.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x40**	**Access : R/W**
	TSTMD_REG_EN	7	Test Mode Register Enable. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	SEE_DEBUG_SEL[2:0]	5:3	See Debug bus output byte enable, bit0=DI[7:0], bit1=DI[15:8], bit2=DI[23:16].	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	2:0	Reserved.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CLK_MODE	7	0: Disable. 1: Enable.	
	-	6	Reserved.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	TEST_MD[3:0]	3:0	Reserved.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	BOND_STS[7:0]	7:0	Reserved.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x44**	**Access : R/W**
	LP_SET0[7:0]	7:0	Output PLL Set.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x55**	**Access : R/W**
	LP_SET0[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	LP_SET1[7:0]	7:0	Output PLL Set.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBN10	7	10-bit Bus enable.	
	DITHER_MINUS	6	1: Enable.	
	-	5	Reserved.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	ODCLK_GATE_ST_SEL[2:0]	6:4		
	-	3:2	Reserved.	
	SEL_ORI_GATE	1		
	ODCLK_GATE_EN	0		
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SC1_SYNC_EN	7		

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:0	Reserved.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODCLK_GATE_END_DLY[7:0]	7:0		
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ODCLK_GATE_END_DLY[11:8]	3:0	See description of '102FA6h'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field created method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: Vsync end.	
	-	4:0	Reserved.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	REM[7:0]	7:0	Htoal REMainder value.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	REM[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PWM5DIV[8]	0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduce, only active when REG_TRACE_PHASE_EN is set to 1.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduce.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '102FB4h'.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x07**	**Access : R/W**
	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_0_REG[7:0]	7:0		
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_1_REG[7:0]	7:0		
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_2_REG[7:0]	7:0		
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_3_REG[7:0]	7:0		
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_4_REG[7:0]	7:0		
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_5_REG[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[7:0]	7:0	Input VDE PRD value.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[15:8]	7:0	See description of '102FD0h'.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[7:0]	7:0	Input Vtt PRD value.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC RANdom noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	
	-	4:0	Reserved.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:0	Reserved.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_R[7:0]	7:0	Data write to R LUT SRAM.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	See description of '102FDCh'.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_G[11:8]	3:0	See description of '102FDEh'.	
70h	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FE0h)	WR_B[7:0]	7:0	Data write to B LUT SRAM.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_B[11:8]	3:0	See description of '102FE0h'.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	See description of '102FE2h'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '102FEAh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '102FEEh'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE0[11:8]	3:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	

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VOP Register (Bank = 102F, sub-bank = 90)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	See description of '102FFEh'.	

SCMI Register (Bank = 102F, Sub-bank = 92)

SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data config from mode 5 change to mode 4.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force madi off.	
	MADI_FORCE_ON_F2	4	F2 force madi on.	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	-	2	Reserved.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	OPM_LINEAR_BASE_SEL_F2	6	F2 linear mode base address selection.	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	IPM_LINEAR_EN_F2	4	F2 IP linear address enable.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	Y8_M4_ONLY_MODE_F2	3	F2 FB store Y8/M4 only mode.	
	Y8_ONLY_MODE_F2	2	F2 FB store Y-8bits only.	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY04_14_14	6	F2 FB store Y-8bits only.	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_BYPASS_INTERLACE_FILM_F2	4	Film-supported bypass interlace mode.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F2	7	F2 memysnc write bank reset.	
	IPM_WREQ_HPRI_SEL_F2	6	F2 ipm wreq high priority selection: 1'b0: ipm local priority. 1'b1: ip2_adj priority.	
	FRC_FREEMD_F2	5	F2 Force output odd/even toggle when 2DDi for interlace input.	
	MIU_SELECT_F2	4	F2 access MIU0 or MIU1 select.	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x02**	**Access : R/W**
	DUMMY05_10_15[5:0]	7:2		
	OPM_F1_EN	1	Enable OPM F1 register.	
	BK_FIELD_SEL_F2	0	F2 memysnc fd selection.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WBANK_ALIGN_USR_F2[1:0]	3:2	[0] wbank align user mode. [1] wbank force align.	
	-	1:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RW_BANK_MAP_MSB_F2	7	F2 msb bit of read/write bank mapping mode.	
	OPM_RBANK_SEL_MSB_F2	6	F2 OP force read bank select msb.	
	-	5:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x88**	**Access : R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x40**	**Access : R/W**
	RW_BANK_MAP_F2[2:0]	7:5	F2 read/write bank mapping mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IPM_BASE_ADDR0_F2[26:24]	2:0	See description of '102F10h'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_OFFSET_F2[12:8]	4:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_FETCH_NUM_F2[12:8]	4:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F20h'.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR0_F2[26:24]	2:0	See description of '102F20h'.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR1_F2[26:24]	2:0	See description of '102F24h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F2[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_EN_F2	7	F2 IP line count limit enable.	
	-	6:5	Reserved.	
	IPM_VCNT_LIMIT_NUM_F2[12:8]	4:0	See description of '102F30h'.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FORCE_MUTE_IPW_ENABLE_F2	5	Force IPM enable at av-mute case.	
	FIELD_NUM_F2[4:0]	4:0	F2 field number.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_FIELD_NUM_DEFINE_F2	7	Enable OPM F2 field number define.	
	OPM_FIELD_NUM_F2[4:0]	6:2	OPM F2 field number.	
	OPM_8READ_EN_F2	1	F2 opm 8read mode enable.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_6READ_EN_F2	0	F2 opm 6read mode enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_EN_F2	7	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	6	F2 IP write limit flag 0: maximum 1: minimum.	
	-	5:3	Reserved.	
	IPM_W_LIMIT_ADR_F2[26:24]	2:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_EN_F2	7	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[14:8]	6:0	See description of '102F38h'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_FLOW_CTRL_CNT[7:0]	7:0	OPW request flow control count.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x88**	**Access : R/W**
	OPW_VP_CNT_CLR	7	OPW write mask field count clear.	
	OPW_MASK_MODE[2:0]	6:4	OPW write mask number by field.	
	OPW_STATUS_CLR	3	OPW status clear enable.	
	OPW_REQ_RST	2	OPW write request reset.	
	-	1	Reserved.	
	OPW_WREQ_OFF_F2	0	OPW write request disable.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_THRD[7:0]	7:0	OPW FIFO threshold for read request.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_HPRI[7:0]	7:0	OPW high priority threshold for read request.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPW_WREQ_MAX[7:0]	7:0	OPW read request max number.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x22**	**Access : R/W**
	OPW_WFIFO_DEPTH[7:0]	7:0	OPW line buffer length for memory data write.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at real line case.	
2Ch	**REG102F59**	**7:0**	**Default : 0x12**	**Access : R/W**

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F59h)	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at real line case.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPM_3D_SBS_FORCE_EN_F2	1	F2 IPM 3D side by side input enable.	
	IPM_3D_EN_F2	0	F2 IPM 3D input enable.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY34_7_7	7	HDMI 3D OPM side by side read using PIP.	
	-	6:0	Reserved.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[15:8]	7:0	See description of '102F6Ch'.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[15:8]	7:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[15:8]	7:0	See description of '102F7Ch'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x18**	**Access : R/W**
	DUMMY40_5_15[2:0]	7:5		
	OPM_LB_CEN_MODE	4	OP Line buffer power ctrl.	
	UPDATE_MEM_CONFIG_EN	3	Update memory format enable.	
	-	2	Reserved.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_REG_DBF_EN_F2	1	F2 Register latch with input V sync enable.	
	OPM_REG_DBF_EN	0	Register latch with output V sync enable.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY40_5_15[10:3]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY41_7_6[1:0]	7:6		
	-	5:0	Reserved.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MADI_FORCE_OFF_F1	5	F1 force madi off.	
	MADI_FORCE_ON_F1	4	F1 force madi on.	
	-	3:0	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_LINEAR_EN_F1	4	F1 IP linear address enable.	
	OPM_4READ_EN_F1	3	F1 OP read 4 fields enable.	
	OPM_3READ_EN_F1	2	F1 OP read 3 fields enable.	
	OPM_2READ_EN_F1	1	F1 OP read 2 fields enable.	
	OPM_1READ_EN_F1	0	F1 OP read 1 field enable.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	FILM_HIGH_PRI_F1	3	F1 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F1	2	F1 OP film dot line data select.	
	DOT_LN_PON_SEL_F1	1	F1 OP MADi dot line data select.	
	-	0	Reserved.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DUMMY44_2_3[1:0]	3:2		
	-	1:0	Reserved.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F1	7	F1 memysnc write bank reset.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_WREQ_HPRI_SEL_F1	6	F1 ipm wreq high priority selection: 1'b0: ipm local priority. 1'b1: ip2_adj priority.	
	-	5:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY45_9_15[6:0]	7:1		
	BK_FIELD_SEL_F1	0	F2 memysnc fd selection.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY46_4_7[3:0]	7:4		
	WBANK_ALIGN_USR_F1[1:0]	3:2	[0] wbank align user mode. [1] wbank force align.	
	WBANK_SRC_SEL_F1[1:0]	1:0	F1 Wbank src selection: 1'b0: original. 1'b1: from sc0 M. 1'b1: from sc0 S.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[7:0]	7:0	F1 OP frame buffer base address 0.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[23:16]	7:0	See description of '102FA0h'.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR0_F1[26:24]	2:0	See description of '102FA0h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[7:0]	7:0	F1 OP frame buffer base address 1.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[23:16]	7:0	See description of '102FA4h'.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_BASE_ADDR1_F1[26:24]	2:0	See description of '102FA4h'.	
54h	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FA8h)	OPM_MWE_OFFSET_F1[7:0]	7:0	F1 OP demo mode pixel offset (pixel unit).	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_MWE_OFFSET_F1[11:8]	3:0	See description of '102FA8h'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F1[7:0]	7:0	F1 OP frame buffer line offset (pixel unit).	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F1[12:8]	4:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F1[7:0]	7:0	F1 OP fetch pixel number of one line.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F1[11:8]	3:0	See description of '102FAEh'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FORCE_MUTE_IPW_ENABLE_F1	5	Force IPS enable at av-mute case.	
	-	4:0	Reserved.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:2	Reserved.	
	OPM_8READ_EN_F1	1	F1 opm 8read mode enable.	
	OPM_6READ_EN_F1	0	F1 opm 6read mode enable.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[7:0]	7:0	OPW write limit address.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[23:16]	7:0	See description of '102FBCh'.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_EN	7	OPW write limit enable.	
	OPW_W_LIMIT_MIN	6	OPW write limit flag 0: maximum 1: minimum.	
	-	5:3	Reserved.	
	OPW_W_LIMIT_ADR[26:24]	2:0	See description of '102FBCh'.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_0	4	SCM first arbiter bypass function enable.	
	SCM_ARB_SW_RST_0	3	SCM first arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_0	2	SCM first arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_0	1	SCM first arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_0	0	SCM first arbiter client 1 having higher priority than client 0.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM_0[7:0]	7:0	SCM first arbiter maximum request number for each last.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY0_THD_0[7:0]	7:0	SCM first arbiter threshold number of flow control of client 0.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_0[7:0]	7:0	SCM first arbiter threshold number of flow control of client 1.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY66_13_15[2:0]	7:5		
	-	4:0	Reserved.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FD_MASK_READ_F1	5	F1 fd mask read back.	
	FD_MASK_READ_F2	4	F2 fd mask read back.	
	-	3:2	Reserved.	
	OPW_WREQ_OFF_ALL	1	All OPW write request disable.	
	OPW_WREQ_OFF_F1	0	F1 OPW write request disable.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY67_8_15[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_1	4	SCM second arbiter bypass function enable.	
	SCM_ARB_SW_RST_1	3	SCM second arbiter software reset bit.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCM_ARB_THD_HIT_LAST_EN_1	2	SCM second arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_1	1	SCM second arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_1	0	SCM second arbiter client 1 having higher priority than client 0.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM_1[7:0]	7:0	SCM second arbiter maximum request number for each last.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY0_THD_1[7:0]	7:0	SCM second arbiter threshold number of flow control of client 0.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_1[7:0]	7:0	SCM second arbiter threshold number of flow control of client 1.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SCM_ARB_BYPASS_EN_2	4	SCM third arbiter bypass function enable.	
	SCM_ARB_SW_RST_2	3	SCM third arbiter software reset bit.	
	SCM_ARB_THD_HIT_LAST_EN_2	2	SCM third arbiter generate last to MIU when threshold hit or client send last.	
	SCM_ARB_FLOW_CTRL_EN_2	1	SCM third arbiter flow control enable.	
	SCM_ARB_RDY1_FIRST_2	0	SCM third arbiter client 1 having higher priority than client 0.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x0C**	**Access : R/W**
	SCM_ARB_MAX_REQ_NUM_2[7:0]	7:0	SCM third arbiter maximum request number for each last.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x08**	**Access : R/W**
	SCM_ARB_RDY0_THD_2[7:0]	7:0	SCM third arbiter threshold number of flow control of client 0.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_ARB_RDY1_THD_2[7:0]	7:0	SCM third arbiter threshold number of flow control of client 1.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	

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SCMI Register (Bank = 102F, sub-bank = 92)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_PRE_DELTA_0_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at real line case.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at real line case.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[7:0]	7:0	F1 status read out for debug.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[15:8]	7:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7E_F1[7:0]	7:0	F1 status read out for debug.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7E_F1[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[7:0]	7:0	F1 status read out for debug.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[15:8]	7:0	See description of '102FFEh'.	

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IPOL Register (Bank = 102F, Sub-bank = 93)

IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A. #10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F07h)	FRCV	7	Source Sync Enable. #1 : Display will adaptive follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F0Eh)	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Ou.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F11h)	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F16h)	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetion.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Eh	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F1Ch)	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0		
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Dh)	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Seperator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Seperator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F43h)	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F48h)	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Seperated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F49h)	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable. #1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F50h)	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**

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IPOL Register (Bank = 102F, sub-bank = 93)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Dh)	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	

ACE Register (Bank = 102F, Sub-bank = 98)

ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_FCC_8T_EN	7	Main window FCC region 8 enable.	
	MAIN_FCC_7T_EN	6	Main window FCC region 7 enable.	

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_FCC_6T_EN	5	Main window FCC region 6 enable.	
	MAIN_FCC_5T_EN	4	Main window FCC region 5 enable.	
	MAIN_FCC_4T_EN	3	Main window FCC region 4 enable.	
	MAIN_FCC_3T_EN	2	Main window FCC region 3 enable.	
	MAIN_FCC_2T_EN	1	Main window FCC region 2 enable.	
	MAIN_FCC_1T_EN	0	Main window FCC region 1 enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FCC_DITHER_EN	6	FCC dither bit enable.	
	FCC_RESERVED_1[4:0]	5:1	Reserved.	
	MAIN_FCC_9T_EN	0	Main window FCC window 9 enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_FCC_8T_EN	7	Sub window FCC region 8 enable.	
	SUB_FCC_7T_EN	6	Sub window FCC region 7 enable.	
	SUB_FCC_6T_EN	5	Sub window FCC region 6 enable.	
	SUB_FCC_5T_EN	4	Sub window FCC region 5 enable.	
	SUB_FCC_4T_EN	3	Sub window FCC region 4 enable.	
	SUB_FCC_3T_EN	2	Sub window FCC region 3 enable.	
	SUB_FCC_2T_EN	1	Sub window FCC region 2 enable.	
	SUB_FCC_1T_EN	0	Sub window FCC region 1 enable.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SUB_FCC_9T_EN	0	Sub window FCC region 9 enable.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T1[7:0]	7:0	FCC region 1 cb target.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T1[7:0]	7:0	FCC region 1 cr target.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T2[7:0]	7:0	FCC region 2 cb target.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T2[7:0]	7:0	FCC region 2 cr target.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T3[7:0]	7:0	FCC region 3 cb target.	

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T3[7:0]	7:0	FCC region 3 cr target.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T4[7:0]	7:0	FCC region 4 cb target.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T4[7:0]	7:0	FCC region 4 cr target.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T5[7:0]	7:0	FCC region 5 cb target.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T5[7:0]	7:0	FCC region 5 cr target.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T6[7:0]	7:0	FCC region 6 cb target.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T6[7:0]	7:0	FCC region 6 cr target.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T7[7:0]	7:0	FCC region 7 cb target.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T7[7:0]	7:0	FCC region 7 cr target.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T8[7:0]	7:0	FCC region 8 cb target.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T8[7:0]	7:0	FCC region 8 cr target.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_2T[3:0]	7:4	FCC region 2 strength.	
	FCC_K_1T[3:0]	3:0	FCC region 1 strength.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_4T[3:0]	7:4	FCC region 4 strength.	
	FCC_K_3T[3:0]	3:0	FCC region 3 strength.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_6T[3:0]	7:4	FCC region 6 strength.	
	FCC_K_5T[3:0]	3:0	FCC region 5 strength.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_8T[3:0]	7:4	FCC region 8 strength.	

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_K_7T[3:0]	3:0	FCC region 7 strength.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FCC_K_9T[3:0]	3:0	FCC region 9 strength.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN1_CB_UP[1:0]	7:6	FCC region 1 target cb up distance.	
	FCC_WIN1_CB_DOWN[1:0]	5:4	FCC region 1 target cb down distance.	
	FCC_WIN1_CR_UP[1:0]	3:2	FCC region 1 target cr up distance.	
	FCC_WIN1_CR_DOWN[1:0]	1:0	FCC region 1 target cr down distance.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN2_CB_UP[1:0]	7:6	FCC region 2 target cb up distance.	
	FCC_WIN2_CB_DOWN[1:0]	5:4	FCC region 2 target cb down distance.	
	FCC_WIN2_CR_UP[1:0]	3:2	FCC region 2 target cr up distance.	
	FCC_WIN2_CR_DOWN[1:0]	1:0	FCC region 2 target cr down distance.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN3_CB_UP[1:0]	7:6	FCC region 3 target cb up distance.	
	FCC_WIN3_CB_DOWN[1:0]	5:4	FCC region 3 target cb down distance.	
	FCC_WIN3_CR_UP[1:0]	3:2	FCC region 3 target cr up distance.	
	FCC_WIN3_CR_DOWN[1:0]	1:0	FCC region 3 target cr down distance.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN4_CB_UP[1:0]	7:6	FCC region 4 target cb up distance.	
	FCC_WIN4_CB_DOWN[1:0]	5:4	FCC region 4 target cb down distance.	
	FCC_WIN4_CR_UP[1:0]	3:2	FCC region 4 target cr up distance.	
	FCC_WIN4_CR_DOWN[1:0]	1:0	FCC region 4 target cr down distance.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN5_CB_UP[1:0]	7:6	FCC region 5 target cb up distance.	
	FCC_WIN5_CB_DOWN[1:0]	5:4	FCC region 5 target cb down distance.	
	FCC_WIN5_CR_UP[1:0]	3:2	FCC region 5 target cr up distance.	
	FCC_WIN5_CR_DOWN[1:0]	1:0	FCC region 5 target cr down distance.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN6_CB_UP[1:0]	7:6	FCC region 6 target cb up distance.	
	FCC_WIN6_CB_DOWN[1:0]	5:4	FCC region 6 target cb down distance.	
	FCC_WIN6_CR_UP[1:0]	3:2	FCC region 6 target cr up distance.	

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_WIN6_CR_DOWN[1:0]	1:0	FCC region 6 target cr down distance.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN7_CB_UP[1:0]	7:6	FCC region 7 target cb up distance.	
	FCC_WIN7_CB_DOWN[1:0]	5:4	FCC region 7 target cb down distance.	
	FCC_WIN7_CR_UP[1:0]	3:2	FCC region 7 target cr up distance.	
	FCC_WIN7_CR_DOWN[1:0]	1:0	FCC region 7 target cr down distance.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN8_CB_UP[1:0]	7:6	FCC region 8 target cb up distance.	
	FCC_WIN8_CB_DOWN[1:0]	5:4	FCC region 8 target cb down distance.	
	FCC_WIN8_CR_UP[1:0]	3:2	FCC region 8 target cr up distance.	
	FCC_WIN8_CR_DOWN[1:0]	1:0	FCC region 8 target cr down distance.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FCC_WIN9_CB[2:0]	5:3	FCC region 9 target cb distance.	
	FCC_WIN9_CR[2:0]	2:0	FCC region 9 target cr distance.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:3	Reserved.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	-	1:0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation, [0]: Other_color. [1]: Red. [2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation, [0]: Other_color. [1]: Red. [2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
3Ch	**REG102F78**	**7:0**	**Default : 0xFF**	**Access : R/W**

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F78h)	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	White peak limit threshold.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	
	SUB_IBC_EN	6	Sub window IBC enable.	
	-	5:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_HIGH_PASS_EN	7	Main window Y H_coring as high pass filter.	
	MAIN_Y_TABLE_STEP[2:0]	6:4	Main window Y H_coring LUT step.	
	MAIN_PC_MODE	3	Main window PC mode.	
	-	2	Reserved.	
	MAIN_Y_BAND2_H_CORING_EN	1	Main window Y band2 H_coring enable.	
	MAIN_Y_BAND1_H_CORING_EN	0	Main window Y band1 H_coring enable.	

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_HIGH_PASS_EN	7	Main window C H_coring as high pass filter.	
	MAIN_C_TABLE_STEP[2:0]	6:4	Main window C H_coring LUT step.	
	MAIN_WHITE_PEAK_LIMIT_EN	3	Main window white peak limit enable.	
	-	2	Reserved.	
	MAIN_C_BAND2_H_CORING_EN	1	Main window C band2 H_coring enable.	
	MAIN_C_BAND1_H_CORING_EN	0	Main window C band1 H_coring enable.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE1[7:0]	7:0	Main window Y gain table 1.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE2[7:0]	7:0	Main window Y gain table 2.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE3[7:0]	7:0	Main window Y gain table 3.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE4[7:0]	7:0	Main window Y gain table 4.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE1[7:0]	7:0	Main window C gain table 1.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE2[7:0]	7:0	Main window C gain table 2.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE3[7:0]	7:0	Main window C gain table 3.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE4[7:0]	7:0	Main window C gain table 4.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_NOISE_MASKING_EN	7	Main window horizontal Y NMR enable.	
	MAIN_Y_COLOR_NOISE_MASKING_EN	6	Main window horizontal Y NMR color adaptive enable.	
	MAIN_Y_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal Y NMR gain (xxxx.xx).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_Y_NM_MIN_THRD[3:0]	7:4	Main window Y mosquito noise removemin value threshold.	
	MAIN_Y_NM_MAX_THRD[3:0]	3:0	Main window Y mosquito noise remove max value threshold.	
58h	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB1h)	-	7:4	Reserved.	
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.	
	-	2:0	Reserved.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_NOISE_MASKING_EN	7	Sub window horizontal Y NMR enable.	
	SUB_Y_COLOR_NOISE_MASKING_EN	6	Sub window horizontal Y NMR color adaptive enable.	
	-	5:0	Reserved.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_DITHER_EN	6	Sub window horizontal Y NMR dither enable.	
	-	5	Reserved.	
	MAIN_Y_DITHER_EN	4	Main window horizontal Y NMR dither enable.	
	-	3:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:0	Reserved.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**

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ACE Register (Bank = 102F, sub-bank = 98)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FC7h)	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_R2Y_EQ_SEL[2:0]	6:4	Sub window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	
	-	3	Reserved.	
	MAIN_R2Y_EQ_SEL[2:0]	2:0	Main window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	

PEAKING Register (Bank = 102F, Sub-bank = 99)

PEAKING Register (Bank = 102F, sub-bank = 99)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	

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PEAKING Register (Bank = 102F, sub-bank = 99)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.	
	-	3:1	Reserved.	
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.	

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PEAKING Register (Bank = 102F, sub-bank = 99)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_OVERSHOOT_LIMIT[7:0]	7:0	Main window band1 overshoot limit.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_OVERSHOOT_LIMIT[7:0]	7:0	Main window band2 overshoot limit.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_OVERSHOOT_LIMIT[7:0]	7:0	Main window band3 overshoot limit.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_OVERSHOOT_LIMIT[7:0]	7:0	Main window band4 overshoot limit.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band1 undershoot limit.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band2 undershoot limit.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band3 undershoot limit.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band4 undershoot limit.	
28h	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**

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PEAKING Register (Bank = 102F, sub-bank = 99)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F50h)	-	7:6	Reserved.	
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_PEAKING_EN	7	Main window color adaptive peaking enable.	
	MAIN_COLOR_FACTOR_LPF_EN	6	Main window color factor LPF enable.	
	-	5:0	Reserved.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	-	3:2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CR_DELAY_NUM	6	Sub window cr delay number. #0: no delay. #1: delay 1T.	
	-	5	Reserved.	
	MAIN_CR_DELAY_NUM	4	Main window cr delay number. #0: no delay. #1: delay 1T.	
	-	3:2	Reserved.	
	SUB_YC_DELAY_EN	1	Sub window yc delay enable.	
	MAIN_YC_DELAY_EN	0	Main window yc delay enable.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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PEAKING Register (Bank = 102F, sub-bank = 99)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_CB_DELAY_NUM	6	Sub window cb delay number. #0: no delay. #1: delay 1T.	
	-	5	Reserved.	
	SUB_Y_DELAY_NUM	4	Sub window y delay number. #0: no delay. #1: delay 1T.	
	-	3	Reserved.	
	MAIN_CB_DELAY_NUM	2	Main window cb delay number. #0: no delay. #1: delay 1T.	
	-	1	Reserved.	
	MAIN_Y_DELAY_NUM	0	Main window y delay number. #0: no delay. #1: delay 1T.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_COLOR_PK_WIN4_EN	7	Sub window color adaptive win4 enable.	
	SUB_COLOR_PK_WIN3_EN	6	Sub window color adaptive win3 enable.	
	SUB_COLOR_PK_WIN2_EN	5	Sub window color adaptive win2 enable.	
	SUB_COLOR_PK_WIN1_EN	4	Sub window color adaptive win1 enable.	
	MAIN_COLOR_PK_WIN4_EN	3	Main window color adaptive win4 enable.	
	MAIN_COLOR_PK_WIN3_EN	2	Main window color adaptive win3 enable.	
	MAIN_COLOR_PK_WIN2_EN	1	Main window color adaptive win2 enable.	
	MAIN_COLOR_PK_WIN1_EN	0	Main window color adaptive win1 enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_TRANSITION_STEP[1:0]	7:6	Color adaptive win4 transition step.	
	COLOR_PK_WIN3_TRANSITION_STEP[1:0]	5:4	Color adaptive win3 transition step.	
	COLOR_PK_WIN2_TRANSITION_STEP[1:0]	3:2	Color adaptive win2 transition step.	
	COLOR_PK_WIN1_TRANSITION_STEP[1:0]	1:0	Color adaptive win1 transition step.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_ENTRY_VALUE[3:0]	7:4	Color adaptive win2 strength.	
	COLOR_PK_WIN1_ENTRY_VALUE[3:0]	3:0	Color adaptive win1 strength.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_ENTRY_VALUE[3:0]	7:4	Color adaptive win4 strength.	

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PEAKING Register (Bank = 102F, sub-bank = 99)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COLOR_PK_WIN3_ENTRY_VALUE[3:0]	3:0	Color adaptive win3 strength.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	COLOR_PK_TEST_EN[3:0]	3:0	Color adaptive test mode enable.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_PK_ADP_Y_STEP[1:0]	5:4	Main window peaking adaptive y alpha step.	
	-	3:2	Reserved.	
	MAIN_PK_ADP_Y_ALPHA_LPF_EN	1	Main window peaking adaptive y alpha low pass filter enable.	
	MAIN_PK_ADP_Y_EN	0	Main window peaking adaptive y enable.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PK_Y_LOW_THRD[7:0]	7:0	Main window peaking adaptive y low threshold.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_1[3:0]	7:4	Main window peaking adaptive y alpha LUT 1.	
	MAIN_PK_ADP_Y_ALPHA_LUT_0[3:0]	3:0	Main window peaking adaptive y alpha LUT 0, format is x.xxx, range is 0~F.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x76**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_3[3:0]	7:4	Main window peaking adaptive y alpha LUT 3.	
	MAIN_PK_ADP_Y_ALPHA_LUT_2[3:0]	3:0	Main window peaking adaptive y alpha LUT 2.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_5[3:0]	7:4	Main window peaking adaptive y alpha LUT 5.	
	MAIN_PK_ADP_Y_ALPHA_LUT_4[3:0]	3:0	Main window peaking adaptive y alpha LUT 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_7[3:0]	7:4	Main window peaking adaptive y alpha LUT 7.	
	MAIN_PK_ADP_Y_ALPHA_LUT_6[3:0]	3:0	Main window peaking adaptive y alpha LUT 6.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_UP[7:0]	7:0	Color adaptive win1 cb up.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CR_UP[7:0]	7:0	Color adaptive win1 cr up.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_DOWN[7:0]	7:0	Color adaptive win1 cb down.	
59h	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**

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PEAKING Register (Bank = 102F, sub-bank = 99)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB3h)	COLOR_PK_WIN1_CR_DOWN[7:0]	7:0	Color adaptive win1 cr down.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CB_UP[7:0]	7:0	Color adaptive win2 cb up.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CR_UP[7:0]	7:0	Color adaptive win2 cr up.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CB_DOWN[7:0]	7:0	Color adaptive win2 cb down.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CR_DOWN[7:0]	7:0	Color adaptive win2 cr down.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CB_UP[7:0]	7:0	Color adaptive win3 cb up.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CR_UP[7:0]	7:0	Color adaptive win3 cr up.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CB_DOWN[7:0]	7:0	Color adaptive win3 cb down.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN3_CR_DOWN[7:0]	7:0	Color adaptive win3 cr down.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_CB_UP[7:0]	7:0	Color adaptive win4 cb up.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_CR_UP[7:0]	7:0	Color adaptive win4 cr up.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_CB_DOWN[7:0]	7:0	Color adaptive win4 cb down.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN4_CR_DOWN[7:0]	7:0	Color adaptive win4 cr down.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_PK_ADP_Y_ALPHA_LPF_EN	1	Sub window peaking adaptive y alpha low pass filter enable.	
	SUB_PK_ADP_Y_EN	0	Sub window peaking adaptive y enable.	

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DLC Register (Bank = 102F, Sub-bank = 9A)

DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PRE_Y_GAIN_LSB[3:0]	7:4	Main window pre Y gain LSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
	MAIN_Y_GAIN_LSB[3:0]	3:0	Main window Y gain LSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PRE_Y_GAIN_LSB[3:0]	7:4	Sub window pre Y gain LSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
	SUB_Y_GAIN_LSB[3:0]	3:0	Sub window Y gain LSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	UVC_DITHER_EN	7	UV compensate dither enable.	
	-	6	Reserved.	
	SUB_UVC_LOCATE	5	Sub window UV compensate reference location. //0: after ble/wle. //1: after curve fit.	
	SUB_UVC_EN	4	Sub window UV compensate enable.	
	-	3:2	Reserved.	
	MAIN_UVC_LOCATE	1	Main window UV compensate reference location. //0: after ble/wle. //1: after curve fit0.	
	MAIN_UVC_EN	0	Main window UV compensate enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximun pixel.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximun pixel.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimun pixel.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	MAIN_Y_GAIN[6:0]	6:0	Main window Y gain MSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
14h	**REG102F29**	**7:0**	**Default : 0x40**	**Access : R/W**

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F29h)	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_GAIN[6:0]	6:0	Sub window Y gain MSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PRE_Y_GAIN[6:0]	6:0	Main window pre- Y gain MSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	SUB_PRE_Y_GAIN[6:0]	6:0	Sub window pre- Y gain MSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_POST_BRI_ADJUST_LSB[1:0]	1:0	Main window post Y adjust low bit (2's complement).	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_POST_BRI_ADJUST_LSB[1:0]	1:0	Sub window post Y adjust low bit (2's complement).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_POST_BRI_ADJUST[7:0]	7:0	Main window post Y adjust.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_POST_BRI_ADJUST[7:0]	7:0	Sub window post Y adjust.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x18**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x28**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h	**REG102F63**	**7:0**	**Default : 0x38**	**Access : R/W**

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F63h)	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x48**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x58**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x68**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x78**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x98**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0xA8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0xC8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0xE8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[15:8]	7:0	See description of '102F82h'.	

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[15:8]	7:0	See description of '102F92h'.	
4Ah	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F94h)	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[15:8]	7:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[15:8]	7:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[15:8]	7:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[15:8]	7:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[15:8]	7:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[15:8]	7:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB5h)	TOTAL_32_26[15:8]	7:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[15:8]	7:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[15:8]	7:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[15:8]	7:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[15:8]	7:0	See description of '102FBEh'.	
63h ~ 63h (102FC6h ~ 102FC7h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x60**	**Access : R/W**
	MAIN_UVC_GAIN_HIGH_LIMIT[7:0]	7:0	Main window UV compensate gain up limit (format is 4.8).	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_HIGH_LIMIT[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAIN_UVC_GAIN_LOW_LIMIT[7:0]	7:0	Main window UV compensate gain down limit (format is 4.8).	

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DLC Register (Bank = 102F, sub-bank = 9A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_LOW_LIMIT[11:8]	3:0	See description of '102FCAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '102FEEh'.	

D3D Register (Bank = 102F, Sub-bank = 9D)

D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_0[7:0]	7:0		
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_0[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_1[7:0]	7:0		
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_1[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_2[7:0]	7:0		
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_3[7:0]	7:0		
13h	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F27h)	LEFT_TOP_LEVEL_3[15:8]	7:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_4[7:0]	7:0		
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_4[15:8]	7:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_5[7:0]	7:0		
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_5[15:8]	7:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_6[7:0]	7:0		
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_6[15:8]	7:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_7[7:0]	7:0		
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_7[15:8]	7:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_8[7:0]	7:0		
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_8[15:8]	7:0	See description of '102F30h'.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_9[7:0]	7:0		
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_9[15:8]	7:0	See description of '102F32h'.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_10[7:0]	7:0		
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_10[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_11[7:0]	7:0		
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_11[15:8]	7:0	See description of '102F36h'.	

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_12[7:0]	7:0		
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_12[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_13[7:0]	7:0		
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_13[15:8]	7:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_14[7:0]	7:0		
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_14[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_15[7:0]	7:0		
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_15[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_16[7:0]	7:0		
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_16[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_17[7:0]	7:0		
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_17[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_18[7:0]	7:0		
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_18[15:8]	7:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_19[7:0]	7:0		
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_19[15:8]	7:0	See description of '102F46h'.	
24h	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F48h)	LEFT_TOP_LEVEL_20[7:0]	7:0		
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_20[15:8]	7:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_21[7:0]	7:0		
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_21[15:8]	7:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_22[7:0]	7:0		
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_22[15:8]	7:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_23[7:0]	7:0		
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_23[15:8]	7:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_24[7:0]	7:0		
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_24[15:8]	7:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_25[7:0]	7:0		
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_25[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_26[7:0]	7:0		
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_26[15:8]	7:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_27[7:0]	7:0		
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_27[15:8]	7:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_28[7:0]	7:0		

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_28[15:8]	7:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_29[7:0]	7:0		
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_29[15:8]	7:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_30[7:0]	7:0		
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_30[15:8]	7:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_31[7:0]	7:0		
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : RO**
	LEFT_TOP_LEVEL_31[15:8]	7:0	See description of '102F5Eh'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_0[7:0]	7:0		
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_0[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_1[7:0]	7:0		
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_1[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_2[7:0]	7:0		
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_2[15:8]	7:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_3[7:0]	7:0		
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_3[15:8]	7:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_4[7:0]	7:0		
34h	**REG102F69**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F69h)	RIGHT_BOTTOM_LEVEL_4[15:8]	7:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_5[7:0]	7:0		
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_5[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_6[7:0]	7:0		
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_6[15:8]	7:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_7[7:0]	7:0		
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_7[15:8]	7:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_8[7:0]	7:0		
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_8[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_9[7:0]	7:0		
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_9[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_10[7:0]	7:0		
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_10[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_11[7:0]	7:0		
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_11[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_12[7:0]	7:0		
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_12[15:8]	7:0	See description of '102F78h'.	

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_13[7:0]	7:0		
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_13[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_14[7:0]	7:0		
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_14[15:8]	7:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_15[7:0]	7:0		
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_15[15:8]	7:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_16[7:0]	7:0		
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_16[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_17[7:0]	7:0		
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_17[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_18[7:0]	7:0		
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_18[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_19[7:0]	7:0		
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_19[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_20[7:0]	7:0		
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_20[15:8]	7:0	See description of '102F88h'.	
45h	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO**

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F8Ah)	RIGHT_BOTTOM_LEVEL_21[7:0]	7:0		
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_21[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_22[7:0]	7:0		
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_22[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_23[7:0]	7:0		
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_23[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_24[7:0]	7:0		
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_24[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_25[7:0]	7:0		
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_25[15:8]	7:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_26[7:0]	7:0		
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_26[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_27[7:0]	7:0		
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_27[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_28[7:0]	7:0		
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_28[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_29[7:0]	7:0		

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_29[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_30[7:0]	7:0		
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_30[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_31[7:0]	7:0		
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	RIGHT_BOTTOM_LEVEL_31[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RESULT_READY	7		
	-	6:3	Reserved.	
	VSYNC_LOW_ACT	2	0: Vsync pulse is high active 1: vsync pulse is low active.	
	DETECT_MODE	1	0: Side-by-side detection 1: top-bottom detection.	
	TRIGGER_START_WPULSE	0	Trigger start write pulse when 1 for side-by-side or top-bottom detection.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	THRESHOLD[7:0]	7:0	THRESHOLD value of 3D checkboard detection.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	WINDOW_SIZE[1:0]	1:0	3D checkborad detection window size: 2'b00: window size = 5, 2'b01: window size = 7, 2'b10: WINDOW_SIZE = 9, 2'b11: WINDOW_SIZE = 11 (default).	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	CKBOARD_RES[7:0]	7:0		
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	CKBOARD_RES[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOUNDARY_H_TB[7:0]	7:0	Horizontal value of boundary for not detection in top-bottom mode.	
54h	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**

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D3D Register (Bank = 102F, sub-bank = 9D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FA9h)	BOUNDARY_V_TB[7:0]	7:0	Vertical value of boundary for not detection in top-bottom mode.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOUNDARY_H_SBYS[7:0]	7:0	Horizontal value of boundary for not detection in side-by-side mode.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOUNDARY_V_SBYS[7:0]	7:0	Vertical value of boundary for not detection in side-by-side mode.	

DYN_SCL Register (Bank = 102F, Sub-bank = 9F)

DYN_SCL Register (Bank = 102F, sub-bank = 9F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[7:0]	7:0	The number of menuload data (0: disable menuload).	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_REQ_LEN[7:0]	7:0	Length of menuload DMA's request (0: disable menuload).	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_EN	7	Menuload enable (SC0).	
	-	6:3	Reserved.	
	MLOAD_REQ_LEN[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[7:0]	7:0	Base address of allocated memory for menuload.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[23:16]	7:0	See description of '102F06h'.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MLOAD_BASE_ADR[26:24]	2:0	See description of '102F06h'.	
10h	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**

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DYN_SCL Register (Bank = 102F, sub-bank = 9F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F20h)	DS_REQ_LEN[3:0]	7:4	Length of dynamic scaling DMA's request (0: disable dynamic scaling).	
	DS_REQ_TH[3:0]	3:0	Threshold for one dynamic scaling DMA request.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_IPM2MI_SEL	7	Main IP dynamic scaling miu selection.	
	DS_IPS2MI_SEL	6	Sub IP dynamic scaling miu selection.	
	DS_OP2MI_SEL	5	OP dynamic scaling miu selection.	
	DS_RIU_WE	4	Enable write register through RIU.	
	IPM_DS_EN	3	Enable main IP2 dynamic scaling.	
	IPS_DS_EN	2	Enable sub IP2 dynamic scaling.	
	OP_DS_EN	1	Enable OP dynamic scaling.	
	DS_REQ_PRI	0	User specified priority of MIU.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[7:0]	7:0	Base address of allocated memory for dynamic scaling.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[23:16]	7:0	See description of '102F22h'.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DS_BASE_ADR[26:24]	2:0	See description of '102F22h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_IDX_DEPTH[7:0]	7:0	The number of dynamic scaling data per index (0: disable dynamic scaling).	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SC_INDEX_F2_SEL	1	F2 dynamic scaling index select. 0: From main. 1: From sub.	
	SC_INDEX_F1_SEL	0	F1 dynamic scaling index select. 0: From main. 1: From sub.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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DYN_SCL Register (Bank = 102F, sub-bank = 9F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DS_OP_IDX_SEL	4	Dyn_scl idx selection for OP (SC0). (only active when reg_new_idx_mode_en = 1). 0: F2(main). 1: F1(sub).	
	NEW_IDX_MODE_EN	3	Enable new MIU idx mode. 0: OP-SC1, IP, OP. 1: IPS, OP-SC1, IPM, OP.	
	-	2:0	Reserved.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	DS_MREQ_ALWAYS_ACTIVE	2	Set mreq_dyn_scl always active.	
	DS_RIU_BE[1:0]	1:0	Byte enable for DS RIU interface.	

OP1_TOP Register (Bank = 102F, Sub-bank = A0)

OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x01**	**Access : R/W**
	PIP_DISABLE	7	Disable PIP Function.	
	-	6	Reserved.	
	SC2LB_EN	5	Enable HD side by side line buffer mode.	
	-	4:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the scree.	
	MAIN_EN	0	Enable main window shown on the scree.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	
	FBL_SEL	4	Select FBL source. #b0: Source F2 is FBL. #b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x70**	**Access : R/W**
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x07**	**Access : R/W**
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the extra_y to half.	
	-	4:3	Reserved.	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. #h0: 16 pixel. #h1: 32 pixel. #h2: 64 pixel. #h3: 128 pixel. #h4: (overlap length) / 8. #h5: (overlap length) / 4. #h6: (overlap length) / 2. #h7: (overlap length).	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F1[11:8]	3:0	See description of '102F26h'.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F2[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F1[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.	
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x02**	**Access : R/W**
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).	
	EXTRA_FETCH_LINE[3:0]	3:0	How many line will be fetched by extra request. Minimum is 1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_F2_EN	1	Force F1 use F2's register setting.	
	ATP_EN	0	Manual tune parameter.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xB8**	**Access : R/W**
	SEL_DS	7	Select the source to trigger dynamic scaling. h0: Falling edge of Vsync. h1: Delay line set by REG_DS_TRIG_DLY.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. #0: vsync of SC_TOP. #1: delay one line of vfde.	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. #h0: down_eq7. #h1: down_eq8. #h2: down_eq9. #h3: delay lines set by reg_disp_trig_dly.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. #h0: Falling edge of vsync. #h1: Nearly raising edge of vsync. #h2: delay line set by reg_atp_trig_dly. #h3: Manual trig by set reg_atp_en.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. #h0: Falling edge of vfde. #h1: Raising edge of vsync. #h2: Reserved. #h3: Reserved.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SEL_MLOAD[1:0]	5:4	Select the source to trigger menuload. h0: Falling edge of VFDE. h1: Rising edge of VSync. h2: Falling edge of VSync. h3: Delay line set by REG_MLOAD_TRIG_DLY.	
	-	3:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x03**	**Access : R/W**
	ATP_TRIG_DLY[7:0]	7:0	Generate train_trig_p from delayed line of vsync.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x05**	**Access : R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate disp_trig_p from delayed line of vsync.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '102F36h'.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. Extra_eq will be disabled when overlapped length less then this threshold.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra request.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xC2**	**Access : R/W**
	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. #h0: 2 pixel. #h1: 4 pixel. #h2: 8 pixel. #h3: 16 pixel.	
	DISP_START_MODE	5	Select the display line buffer start mode. #0: start at advance 1 display line. #1: start at faling edge of vsync_init.	
	DISP_LB_MODE	4	Select the trig mode. #0: Line base. #1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. #h0: before 8 pixel. #h1: before 16 pixel. #h2: before 32 pixel. #h3: before 64 pixel.	
	DISP_RLN_MODE[1:0]	1:0	Select the under_run value of display level. #h0: update by hsync (not optimum performance). #h1: update when session done(may error). #h2: update when line done(reg_disp_trig_mode = 1'b0). #h3: Reserved.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_UNDER_MODE	3	Select the under_run value of display level. #0: 16'h0000. #1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of op1_disp.	
	DISP_LB_WEZ	1	Disable wen of display line buffer.	
	DISP_TRIG_MODE	0	Select the trig mode. #0: Trigged by self_counter. #1: Trigged by op2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x07**	**Access : R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x01**	**Access : R/W**
	DS_TRIG_DLY[7:0]	7:0	Generate DS_TRIG_P from delayed line of Vsync.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DS_TRIG_DLY[11:8]	3:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x01**	**Access : R/W**
	MLOAD_TRIG_DLY[7:0]	7:0	Generate MLOAD_TRIG_P from delayed line of Vsync.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MLOAD_TRIG_DLY[11:8]	3:0	See description of '102F44h'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FLAG_BB_ADR_INI	2	Status of cnt_bb_adr_ini, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	FLAG_BO_END_LN	1	Status of line_base_bot, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	-	0	Reserved.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BO_END_LN[7:0]	7:0	Software mode to set the line_base_bot for extra request.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_BO_END_LN[11:8]	3:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the cnt_bb_adr_ini.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_BB_ADR_INI[11:8]	3:0	See description of '102F64h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line cnt of first display position.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line cnt of minimum display level occure.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '102F88h'.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_LEN[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.	
56h	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FADh)	-	7:4	Reserved.	
	SCLB_BA_LEN[11:8]	3:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_LEN[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1A[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1B[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '102FB8h'.	
5Dh	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FBAh)	BO_LENGTH_RD[7:0]	7:0	Read bo_length.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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OP1_TOP Register (Bank = 102F, Sub-bank = A0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DISP_TF_LEN[11:8]	3:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '102FCEh'.	

ELA Register (Bank = 102F, Sub-bank = A1)

ELA Register (Bank = 102F, Sub-bank = A1)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	

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MADI Register (Bank = 102F, Sub-bank = A2)

MADI Register (Bank = 102F, Sub-bank = A2)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F1_DNR_CORE_EN	1	F1 DNR CORE FUNCTION EN.	
	F1_DNR_EN	0	F1 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. #0 : non-linear. #1 : linear.	
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. #0 : non-linear. #1 : linear.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.	
	SNR_EN	0	F2 SNR FUNCTION EN.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. #00 : add 0. #01 : add dither. #10 : add dither. #11 : add dither.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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MADI Register (Bank = 102F, Sub-bank = A2)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.	
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.	
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_SHARP_LEVEL[3:0]	3:0	SNR sharpness level.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h	**REG102F88**	**7:0**	**Default : 0xBD**	**Access : R/W**

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MADI Register (Bank = 102F, Sub-bank = A2)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F88h)	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	F2_WIN_EN	0	F2 DNR/SNR active window enable.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_XSTART[7:0]	7:0	F2 DNR/SNR active window start X.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XSTART[10:8]	2:0	See description of '102FE8h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_YSTART[7:0]	7:0	F2 DNR/SNR active window start Y.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YSTART[10:8]	2:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x68**	**Access : R/W**
	F2_WIN_XEND[7:0]	7:0	F2 DNR/SNR active window end X.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XEND[10:8]	2:0	See description of '102FECh'.	

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MADI Register (Bank = 102F, Sub-bank = A2)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0xF0**	**Access : R/W**
	F2_WIN_YEND[7:0]	7:0	F2 DNR/SNR active window end Y.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YEND[10:8]	2:0	See description of '102FEEh'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F2[7:0]	7:0	F2 hcnt for debug.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	STATUS_HCNT_F2[10:8]	2:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F2[7:0]	7:0	F2 vcnt for debug.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F2	7	F2 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F2[10:8]	2:0	See description of '102FF6h'.	

HVSP Register (Bank = 102F, Sub-bank = A3)

HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '102F02h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '102F06h'.	
04h	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F08h)	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '102F06h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '102F0Ah'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '102F0Eh'.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '102F12h'.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F2	7	Main window data format is 422.	
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F2	5	Main Cr_load initial value.	
	-	4:2	Reserved.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F2[3:0]	3:0	Main window horizontal de-ringing threshold0.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F2	7	Main window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F2[2:0]	6:4	Main window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F2[3:0]	3:0	Main window horizontal de-ringing threshold2.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F2[7:0]	7:0	Main window horizontal de-ringing offset.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F2[7:0]	7:0	Main window horizontal de-ringing offset2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F2	7	Main window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F2[2:0]	6:4	Main window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F2[3:0]	3:0	Main window vertical de-ringing threshold0.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F2	7	Main window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F2[2:0]	6:4	Main window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F2[3:0]	3:0	Main window vertical de-ringing threshold2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F2[7:0]	7:0	Main window vertical de-ringing offset.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F2[7:0]	7:0	Main window vertical de-ringing offset2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F2	7	Main window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	
1Bh (102F36h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO[7:0]	7:0	Dynamic horizontal scaling factor.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_HO[23:16]	7:0	See description of '102F38h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE[7:0]	7:0	Dynamic vertical scaling factor.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE[15:8]	7:0	See description of '102F3Ch'.	
1Fh	**REG102F3E**	**7:0**	**Default : 0x10**	**Access : R/W**

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Eh)	DY_FACTOR_VE[23:16]	7:0	See description of '102F3Ch'.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_SELECT	7	Dynamic scaling factor usage. 0: For main window. 1: For sub window.	
	-	6:0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal initial factor.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F1[19:16]	3:0	See description of '102F42h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[7:0]	7:0	Sub window vertical initial factor 1.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[15:8]	7:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[23:16]	7:0	See description of '102F46h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[7:0]	7:0	Sub window vertical initial factor 2.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[15:8]	7:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[23:16]	7:0	See description of '102F4Ah'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal scaling factor.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[15:8]	7:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[23:16]	7:0	See description of '102F4Eh'.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCALE_HO_EN_F1	0	Sub window horizontal scaling enable.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[7:0]	7:0	Sub window vertical scaling factor.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[23:16]	7:0	See description of '102F52h'.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F1	7	Sub window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F1	0	Sub window vertical scaling enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F1	7	Sub window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F1	6	Sub window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F1	5	Sub window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F1	4	Sub window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F1[2:0]	3:1	Sub window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F1	0	Sub window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F1	7	Sub window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F1	6	Sub window vertical Y scaling filter SRAM usage enable.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	C_RAM_SEL_VE_F1	5	Sub window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F1	4	Sub window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F1[2:0]	3:1	Sub window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F1	0	Sub window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F1	7	Sub window data format is 422.	
	422_INTP_F1	6	Sub window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F1	5	Sub Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F1	1	Sub window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F1	0	Sub window dithering enable for horizontal scaling process.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F1	3	Sub window vertical Y coring enable.	
	VSP_CORING_EN_C_F1	2	Sub window vertical C coring enable.	
	HSP_CORING_EN_Y_F1	1	Sub window horizontal Y coring enable.	
	HSP_CORING_EN_C_F1	0	Sub window horizontal C coring enable.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F1[7:0]	7:0	Sub window horizontal C coring threshold.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F1[7:0]	7:0	Sub window horizontal Y coring threshold.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F1[7:0]	7:0	Sub window vertical C coring threshold.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F1[7:0]	7:0	Sub window vertical Y coring threshold.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F1	7	Sub window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F1[2:0]	6:4	Sub window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F1[3:0]	3:0	Sub window horizontal de-ringing threshold0.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F1	7	Sub window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F1[2:0]	6:4	Sub window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F1[3:0]	3:0	Sub window horizontal de-ringing threshold2.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F1[7:0]	7:0	Sub window horizontal de-ringing offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F1[7:0]	7:0	Sub window horizontal de-ringing offset2.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F1	7	Sub window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F1[2:0]	6:4	Sub window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F1[3:0]	3:0	Sub window vertical de-ringing threshold0.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F1	7	Sub window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F1[2:0]	6:4	Sub window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F1[3:0]	3:0	Sub window vertical de-ringing threshold2.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F1[7:0]	7:0	Sub window vertical de-ringing offset.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F1[7:0]	7:0	Sub window vertical de-ringing offset2.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F1	7	Sub window vertical nonlinear scaling enable.	
	H_NL_EN_F1	6	Sub window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F1	3	Sub window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F1	2	Sub window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F1	1	Sub window field polarity switch.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	2_INIFAC_MD_F1	0	Sub window two initial factors mode.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F1	7	Sub window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F1	6	Sub window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F1	5	Sub window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F1	4	Sub window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F1	2	Sub window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F1	1	Sub window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F1	0	Sub window horizontal nonlinear scaling width0 LSB.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width0.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width1.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width2.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F1	7	Sub window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F1[6:0]	6:0	Sub window horizontal nonlinear scaling initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 0.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 1.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F1[7:0]	7:0	Sub window vertical nonlinear scaling width0.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F1[7:0]	7:0	Sub window vertical nonlinear scaling width1.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F1[7:0]	7:0	Sub window vertical nonlinear scaling width2.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F1	7	Sub window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F1[6:0]	6:0	Sub window vertical nonlinear scaling initial value.	
39h	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F72h)	V_NL_D0_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 0.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 1.	
3Bh (102F76h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CRAM_RW_EN	1	C SRAM read/write enable.	
	YRAM_RW_EN	0	Y SRAM read/write enable.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RAM_R_PULSE	1	SRAM read data pulse.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_ADDR[7:0]	7:0	SRAM read/write address. 0: Address 0~127. 1: Address 128~255.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[7:0]	7:0	SRAM write data.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[23:16]	7:0	See description of '102F86h'.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[31:24]	7:0	See description of '102F86h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[39:32]	7:0	See description of '102F86h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[7:0]	7:0	SRAM read data.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[23:16]	7:0	See description of '102F8Ch'.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[31:24]	7:0	See description of '102F8Ch'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[39:32]	7:0	See description of '102F8Ch'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x41**	**Access : R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.	
	-	6:0	Reserved.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x08**	**Access : R/W**
	3DLR_SIDE2LINE_EN	7	3D LR side-by-side to line-to-line enable.	
	-	6:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F2[1:0]	7:6	Main window CTI step.	
	-	5:3	Reserved.	
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CTI_STEP_F2[2]	0	See description of '102FC0h'.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F2	7	Main window CTI enable.	
	-	6:0	Reserved.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F2[3:0]	3:0	Main window CTI mutual threshold.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F2[2:0]	2:0	Main window CTI mutual step.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F2[1:0]	1:0	Main window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F2[4:0]	4:0	Main window CTI mutual level patch threshold.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F2[5:0]	5:0	Main window CTI mutual trans level slope gain.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F2[4:0]	4:0	Main window CTI mutual C low freq threshold.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F2[5:0]	5:0	Main window CTI mutual C low freq slope gain.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_CLFP_STEP_F2[1:0]	1:0	Main window CTI mutual C low freq step.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F1[1:0]	7:6	Sub window CTI step.	
	-	5:3	Reserved.	
	CTI_LPF_COEF_F1[2:0]	2:0	Sub window CTI LPF coefficients.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CTI_STEP_F1[2]	0	See description of '102FE0h'.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F1	7	Sub window CTI enable.	
	-	6:0	Reserved.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F1[3:0]	3:0	Sub window CTI mutual threshold.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F1[2:0]	2:0	Sub window CTI mutual step.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F1[1:0]	1:0	Sub window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F1[4:0]	4:0	Sub window CTI mutual level patch threshold.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F1[5:0]	5:0	Sub window CTI mutual trans level slope gain.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F1[4:0]	4:0	Sub window CTI mutual C low freq threshold.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F1[5:0]	5:0	Sub window CTI mutual C low freq slope gain.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_CLFP_STEP_F1[1:0]	1:0	Sub window CTI mutual C low freq step.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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HVSP Register (Bank = 102F, Sub-bank = A3)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EXTRA_FACTOR_EN	0	Extra horizontal initial factor enable.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_1[7:0]	7:0	Extra horizontal initial factor 1.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_2[7:0]	7:0	Extra horizontal initial factor 2.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_3[7:0]	7:0	Extra horizontal initial factor 3.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_4[7:0]	7:0	Extra horizontal initial factor 4.	

PAFRC Register (Bank = 102F, Sub-bank = A4)

PAFRC Register (Bank = 102F, Sub-bank = A4)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x13**	**Access : R/W**
	-	7:5	Reserved.	
	TAILCUT	4	TAILCUT enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Disable. 1: Enable.	
	DITH_BITS	2	Dithering bits. 0: 2-bits. 1: 4-bits.	
	TCON_OFF_EN	1	TCON FRC_GAMMA function off signal enable. 0: Ignore TCON gamma/dither turn off signal. 1: Gamma/dither function turn off by TCON FRC_GAMMA_OFF signal.	
	FRC_ON	0	PAFRC enable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_ROTATE_EN	7	Box A/B/C/D relation rotation enable.	
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.	

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PAFRC Register (Bank = 102F, Sub-bank = A4)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOP_BOX_FREEZE	4	Top box freeze.	
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.	
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].	
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.	
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.	
	B_D_SWAP	4	Blue channel diagonal swap.	
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotate.	
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotate.	
	BOX8X8_ROT_UNIT	1	0: Rotate step under per A, B, C or D. 1: Rotate step between A/B/C/D.	
	BOX_FREEZE	0	Box local rotation freeze.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	

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PAFRC Register (Bank = 102F, Sub-bank = A4)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	

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PAFRC Register (Bank = 102F, Sub-bank = A4)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4nd 4 frame rotation step.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3nd 4 frame rotation step.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Counterwise. 1: Back.	
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Counterwise. 1: Back.	
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Counterwise. 1: Back.	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Counterwise. 1: Back.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX8X8_ROT_00[1:0]	7:6	Box8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box8x8 entity 11 rotation step by reference.	
	BOX8X8_ROT_10[1:0]	1:0	Box8x8 entity 10 rotation step by reference.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.	
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.	

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PAFRC Register (Bank = 102F, Sub-bank = A4)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.	
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.	
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.	
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.	
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.	
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.	
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.	
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.	
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.	
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.	
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.	
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.	
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.	
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.	
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.	
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.	
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.	
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.	
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.	
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.	
49h	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**

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PAFRC Register (Bank = 102F, Sub-bank = A4)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F93h)	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.	
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.	
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.	
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.	
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.	
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.	
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.	
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.	
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.	
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.	

XVYCC Register (Bank = 102F, Sub-bank = A5)

XVYCC Register (Bank = 102F, Sub-bank = A5)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	-	3:0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post r channel offset.	

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XVYCC Register (Bank = 102F, Sub-bank = A5)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post g channel offset.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post b channel offset.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post r channel gain.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post g channel gain.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post b channel gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post r channel offset.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102F4Eh'.	

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XVYCC Register (Bank = 102F, Sub-bank = A5)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_BRI_OFFSET[7:0]	7:0	Sub window post g channel offset.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_BRI_OFFSET[7:0]	7:0	Sub window post b channel offset.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post r channel gain.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post g channel gain.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post b channel gain.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '102F58h'.	

DMS Register (Bank = 102F, Sub-bank = A6)

DMS Register (Bank = 102F, Sub-bank = A6)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x44**	**Access : R/W**
	-	7:5	Reserved.	
	SPIKE_NR_EN_F1	4	Spike NR Enable F1.	

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DMS Register (Bank = 102F, Sub-bank = A6)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPIKE_NR_MR_EN	3	Spike NR motion ratio enable.	
	-	2	Reserved.	
	V_C_LPF_EN_F2	1	Vertical C Low Pass Filter Enable F2.	
	SPIKE_NR_EN_F2	0	Spike NR Enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SPIKE_NR_COEF[3:0]	3:0	Spike NR Coefficient.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	P_THRD_1[4:0]	4:0	Spike NR P threshold 1.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_2[7:0]	7:0	Spike NR P threshold 2.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_3[7:0]	7:0	Spike NR P threshold 3.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	D_31_STEP[2:0]	6:4	Spike NR D31 Step.	
	-	3	Reserved.	
	D_11_21_STEP[2:0]	2:0	Spike NR D11_21 Step.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YP_22_STEP[2:0]	2:0	Spike NR YP22 Step.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SPK_MR_LPF_EN_F2	0	Spike NR motion ratio low pass filter enable F2 (lpf is 3x3 mask).	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_0[7:0]	7:0	Spike NR motion ratio look-up-table 0.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x32**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_1[7:0]	7:0	Spike NR motion ratio look-up-table 1.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_2[7:0]	7:0	Spike NR motion ratio look-up-table 2.	
56h	**REG102FAD**	**7:0**	**Default : 0x76**	**Access : R/W**

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DMS Register (Bank = 102F, Sub-bank = A6)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FADh)	SPIKE_NR_MOTION_LUT_3[7:0]	7:0	Spike NR motion ratio look-up-table 3.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x98**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_4[7:0]	7:0	Spike NR motion ratio look-up-table 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_5[7:0]	7:0	Spike NR motion ratio look-up-table 5.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_6[7:0]	7:0	Spike NR motion ratio look-up-table 6.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_7[7:0]	7:0	Spike NR motion ratio look-up-table 7.	

ACE2 Register (Bank = 102F, Sub-bank = A7)

ACE2 Register (Bank = 102F, Sub-bank = A7)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CURVE_FIT_CF_LPF_EN	5	Sub window color factor low pass filter enable for luma curve [1 2 1].	
	SUB_COLOR_CURVE_FIT_EN	4	Sub window color adaptive enable for luma curve.	
	-	3:2	Reserved.	
	MAIN_CURVE_FIT_CF_LPF_EN	1	Main window color factor low pass filter enable for luma curve [1 2 1].	
	MAIN_COLOR_CURVE_FIT_EN	0	Main window color adaptive enable for luma curve.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	COLOR_PK_WIN1_CF_ENTRY_VALUE[3:0]	3:0	Flesh color adaptive noise masking strength (x.xxx), color define from peaking, format is x.xxx, range is 4'h0~4'h8.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:1	Reserved.	
	MAIN_CTI_EN	0	Main window CTI enable.	

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ACE2 Register (Bank = 102F, Sub-bank = A7)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_CTI_STEP[2:0]	6:4	Main window CTI step.	
	-	3:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_GRAY_THRD[3:0]	3:0	Main window CTI grap patch threshold.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VIP_FUN_BYPASS_EN	0	Vip all function bypass enable.	

VOP2_RP Register (Bank = 102F, Sub-bank = AD)

VOP2_RP Register (Bank = 102F, Sub-bank = AD)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_ST[7:0]	7:0	For osd reference hs start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_NEW_REF	7	Osd new reference hs/vfde enable.	
	-	6:5	Reserved.	
	OSD_HS_ST[12:8]	4:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_END[7:0]	7:0	For osd reference hs end.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OSD_HS_END[12:8]	4:0	See description of '102F22h'.	
12h	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**

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VOP2_RP Register (Bank = 102F, Sub-bank = AD)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F24h)	OSD_VFDE_ST[7:0]	7:0	For osd reference vfde start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_VFDE_ST[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_END[7:0]	7:0	For osd reference vfde end.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_VFDE_END[11:8]	3:0	See description of '102F26h'.	

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Scalar3 (Bank = 1301)

LPLL_REG Register (Bank = 1031)

LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (103102h)	**REG103102**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
01h (103103h)	**REG103103**	**7:0**	**Default : 0x02**	**Access : R/W**
	LPLL1_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N); Default ratio=8; 0: Divide 1 ; 1: Divide 1; 2: Divide 2; 3: Divide 3; 4: Divide 4...	
02h (103104h)	**REG103104**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
02h (103105h)	**REG103105**	**7:0**	**Default : 0x07**	**Access : R/W**
	LPLL1_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
03h (103106h)	**REG103106**	**7:0**	**Default : 0x33**	**Access : R/W**
	LPLL1_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL1_2CHIP_SYN_EN	6		
	LPLL1_PD	5	Power donw control to PLL (active high).	
	LPLL1_IBIAS_ICTRL[2:0]	4:2		
	LPLL1_ICP_ICTRL[1:0]	1:0	Lpll current control.	
03h (103107h)	**REG103107**	**7:0**	**Default : 0x10**	**Access : RO, R/W**
	LPLL1_HIGH_FLAG	7		
	LPLL1_LOCK	6		
	-	5	Reserved.	
	LPLL1_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL1_EN_SKEW_DIVIDER	1		

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LPLL1_ENFRUN	0		
04h (103108h)	**REG103108**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKP_PHASE_SEL[4:0]	4:0		
04h (103109h)	**REG103109**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKM_PHASE_SEL[4:0]	4:0		
05h (10310Ah)	**REG10310A**	**7:0**	**Default : 0x22**	**Access : R/W**
	PRD_LOCK_THRESH[3:0]	7:4	Prd lock thresh.	
	PRD_STABLE_THRESH[3:0]	3:0	Clock stable thresh.	
05h (10310Bh)	**REG10310B**	**7:0**	**Default : 0x02**	**Access : R/W**
	PHASE_LOCK_THRESH[7:0]	7:0	Phase lock thresh.	
06h (10310Ch)	**REG10310C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[7:0]	7:0	Limit for clock freq correction modification.	
06h (10310Dh)	**REG10310D**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[15:8]	7:0	See description of '10310Ch'.	
07h (10310Eh)	**REG10310E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[23:16]	7:0	See description of '10310Ch'.	
08h (103110h)	**REG103110**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[7:0]	7:0	Limit for phase correction modification.	
08h (103111h)	**REG103111**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[15:8]	7:0	See description of '103110h'.	
09h (103112h)	**REG103112**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[23:16]	7:0	See description of '103110h'.	
0Ah (103114h)	**REG103114**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_LPLL_OFFSET[7:0]	7:0	Limit for lpll phase offset.	
0Ah (103115h)	**REG103115**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_LPLL_OFFSET[15:8]	7:0	See description of '103114h'.	
0Bh (103116h)	**REG103116**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PRD[3:0]	7:4	P_gain for prd_lock, gain setting is same as i_gain_prd.	

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	I_GAIN_PRD[3:0]	3:0	I_gain for prd lock. 0: >> 5. 1: >> 4. 2: >> 3. 3: >> 2. 4: >> 1. 5: Same. 6: << 1. 7: << 2. 8: << 3. 9: << 4. 10: << 5. 11: << 6. 12: << 7. 13: << 8. 14: << 9. 15: << 10.	
0Bh (103117h)	**REG103117**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PHASE[3:0]	7:4	P_gain for phase lock, gain setting is same as i_gain_prd.	
	I_GAIN_PHASE[3:0]	3:0	I_gain for phase lock, game setting is same as i_gain_prd.	
0Ch (103118h)	**REG103118**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_GAIN_PHASE_ZERO	7	Disable p_gain for lock phase.	
	I_GAIN_PHASE_ZERO	6	Disable i_gain for lock phase.	
	P_GAIN_PRD_ZERO	5	Disable p_gain for lock prd.	
	I_GAIN_PRD_ZERO	4	Disable i_gain for lock prd.	
	FRAME_LPLL_EN	3	Frame lpll enable.	
	-	2	Reserved.	
	FPLL_MODE[1:0]	1:0	FPLL Mode. 00: Lock phase mode. 01: Full mode. 10: Lock_prd_phase_mode. 11: Reduce_phase_mode.	
0Ch (103119h)	**REG103119**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVS_FRAME_DIV[3:0]	7:4	Output fame div for frame sync (bit3 ~ bit0).	
	IVS_FRAME_DIV[3:0]	3:0	Input frame div for frame sync (bit3 ~ bit0).	

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Dh (10311Ah)	**REG10311A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_2_LIMIT	4	Enable 2 limit.	
	FORCE_PHASE_CLOSE_DONE	3	S.W. Force phase close done.	
	FORCE_PHASE_REDUCE_DONE	2	S.W. Force phase reduce done.	
	FORCE_PRD_LOCK_DONE	1	S.W. Force prd lock done.	
	FORCE_PRD_STABLE	0	S.W. Force prd stable check ok.	
0Dh (10311Bh)	**REG10311B**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	SSC_EN	3	SSC mode enable.	
	PRD_SEL_ORI_VS	2	Select ori ovs as lock prd referene.	
	NON_STABLE_EN	1	Frame pll disable when non_stable flag high.	
	NO_SIGNAL_EN	0	Frame pll disable when no_signal flag high.	
0Eh (10311Ch)	**REG10311C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	EXT_OVS_FRAME_DIV	1	Output frame div for frame sync, high bit (bit4).	
	EXT_IVS_FRAME_DIV	0	Input frame div for frame sync, high bit (bit4).	
0Fh (10311Eh)	**REG10311E**	**7:0**	**Default : 0x44**	**Access : R/W**
	LPLL_SET[7:0]	7:0	PLL initial setting value.	
0Fh (10311Fh)	**REG10311F**	**7:0**	**Default : 0x55**	**Access : R/W**
	LPLL_SET[15:8]	7:0	See description of '10311Eh'.	
10h (103120h)	**REG103120**	**7:0**	**Default : 0x24**	**Access : R/W**
	LPLL_SET[23:16]	7:0	See description of '10311Eh'.	
11h (103122h)	**REG103122**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[7:0]	7:0	Phase dif value.	
11h (103123h)	**REG103123**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[15:8]	7:0	See description of '103122h'.	
12h (103124h)	**REG103124**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PHASE_UP	0	Ovs leading or lagging related to ivs. 0: Leading. 1: Lagging.	
13h (103126h)	**REG103126**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[7:0]	7:0	Reference siganl prd difference value.	
13h (103127h)	**REG103127**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[15:8]	7:0	See description of '103126h'.	
14h (103128h)	**REG103128**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PRD_UP	0	Ovs prd related to ivs prd. 0: Faster. 1: Slower.	
15h (10312Ah)	**REG10312A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
15h (10312Bh)	**REG10312B**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N); 0: Divide 1 ; 1: Divide 1; 2: Divide 2; 3: Divide 3; 4: Divide 4...	
16h ~ 16h (10312Ch ~ 10312Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
17h (10312Eh)	**REG10312E**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum step.	
17h (10312Fh)	**REG10312F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_STEP[9:8]	1:0	See description of '10312Eh'.	
18h	**REG103130**	**7:0**	**Default : 0x00**	**Access : R/W**

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103130h)	LPLL_SPAN[7:0]	7:0	Output PLL spread spectrum span.	
18h (103131h)	**REG103131**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_SPAN[13:8]	5:0	See description of '103130h'.	
19h (103132h)	**REG103132**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDCLK_DIV[7:0]	7:0	Input clock divider for prd sync.	
19h (103133h)	**REG103133**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDCLK_DIV[15:8]	7:0	See description of '103132h'.	
1Ah (103134h)	**REG103134**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDCLK_DIV[23:16]	7:0	See description of '103132h'.	
1Bh (103136h)	**REG103136**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODCLK_DIV[7:0]	7:0	Output dlock divider for prd sync.	
1Bh (103137h)	**REG103137**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODCLK_DIV[15:8]	7:0	See description of '103136h'.	
1Ch (103138h)	**REG103138**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODCLK_DIV[23:16]	7:0	See description of '103136h'.	
1Dh ~ 1Eh (10313Ah ~ 10313Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Fh (10313Eh)	**REG10313E**	**7:0**	**Default : 0x80**	**Access : R/W**
	PHASE_CLOSE_THRESH[7:0]	7:0	Phase close done thresh.	
1Fh (10313Fh)	**REG10313F**	**7:0**	**Default : 0x30**	**Access : R/W**
	REDUCE_DONE_THRESH[3:0]	7:4	Phase reduce done thresh.	
	PHASE_CLOSE_THRESH[11:8]	3:0	See description of '10313Eh'.	
20h (103140h)	**REG103140**	**7:0**	**Default : 0x52**	**Access : R/W**
	-	7	Reserved.	
	HIS_CNT_HIGH_THRESH[2:0]	6:4	History counter high thresh.	
	-	3	Reserved.	
	HIS_CNT_LOW_THRESH[2:0]	2:0	History counter low thresh.	
21h (103142h)	**REG103142**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[7:0]	7:0	Ivs prd value.	
21h	**REG103143**	**7:0**	**Default : 0x00**	**Access : RO**

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103143h)	IVS_PRD_VALUE[15:8]	7:0	See description of '103142h'.	
22h (103144h)	**REG103144**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[23:16]	7:0	See description of '103142h'.	
23h (103146h)	**REG103146**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[7:0]	7:0	Ovs prd value.	
23h (103147h)	**REG103147**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[15:8]	7:0	See description of '103146h'.	
24h (103148h)	**REG103148**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[23:16]	7:0	See description of '103146h'.	
26h (10314Ch)	**REG10314C**	**7:0**	**Default : 0x00**	**Access : RO**
	FIX_V_TOTAL[7:0]	7:0	Reduce phase modify v_total value.	
26h (10314Dh)	**REG10314D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FIX_V_TOTAL[11:8]	3:0	See description of '10314Ch'.	
27h ~ 27h (10314Eh ~ 10314Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
28h (103150h)	**REG103150**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_SET_USING[7:0]	7:0	Pll_set value for using.	
28h (103151h)	**REG103151**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_SET_USING[15:8]	7:0	See description of '103150h'.	
29h (103152h)	**REG103152**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_SET_USING[23:16]	7:0	See description of '103150h'.	
2Ah (103154h)	**REG103154**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_REDUCE_DONE	7	Phase reduce done flag.	
	PRD_LOCK_DONE	6	Prd lock done flag.	
	IVS_PRD_STABLE	5	Idclk stable flag.	
	OVS_PRD_STABLE	4	Odclk stable flag.	
	-	3	Reserved.	

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CS_STATE[2:0]	2:0	Frame pll FSM state. 3'h0 : free run. 3'h1 : lock_freq. 3'h2 : reduce_phase. 3'h3 : wait phase_close. 3'h4 : lock_phase. others: Reserved.	
2Ah (103155h)	**REG103155**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PHASE_LOCK_DONE	0	Phase lock done flag.	
2Bh ~ 2Eh (103156h ~ 10315Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (103160h)	**REG103160**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
30h (103161h)	**REG103161**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N); 0: Divide 1 ; 1: Divide 1; 2: Divide 2; 3: Divide 3; 4: Divide 4...	
31h (103162h)	**REG103162**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
31h	**REG103163**	**7:0**	**Default : 0x00**	**Access : R/W**

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103163h)	LPLL2_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N); Default ratio=8; 0: Divide 1 ; 1: Divide 1; 2: Divide 2; 3: Divide 3; 4: Divide 4...	
32h (103164h)	**REG103164**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
32h (103165h)	**REG103165**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
33h (103166h)	**REG103166**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL2_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL2_2CHIP_SYN_EN	6		
	LPLL2_PD	5	Power donw control to PLL (active high).	
	LPLL2_IBIAS_ICTRL[2:0]	4:2		
	LPLL2_ICP_ICTRL[1:0]	1:0	Lpll current control.	
33h (103167h)	**REG103167**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LPLL2_HIGH_FLAG	7		
	LPLL2_LOCK	6		
	-	5	Reserved.	
	LPLL2_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL2_EN_SKEW_DIVIDER	1		
	LPLL2_ENFRUN	0		
34h (103168h)	**REG103168**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL2_SKEW_CLKP_PHASE_SEL[5:0]	5:0		
34h (103169h)	**REG103169**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL2_SKEW_CLKM_PHASE_SEL[5:0]	5:0		
35h (10316Ah)	**REG10316A**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_2NDPLL_CLK_SEL	5		

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LPLL_POSTDIV_RESET	4		
	-	3	Reserved.	
	LPLL_2CHIP_REFIN_SEL	2		
	LPLL_2CHIP_FBIN_SEL	1		
	LPLL_2CHIP_CLKOUT_SEL	0		
35h (10316Bh)	**REG10316B**	**7:0**	**Default : 0x1F**	**Access : R/W**
	LPLL_RESERVED_DIV_I[3:0]	7:4	Reserved div sel.	
	LPLL_RESERVED_PD[3:0]	3:0	Reserved power donw control (active high).	
36h (10316Ch)	**REG10316C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[7:0]	7:0	LPLL1_TEST.	
36h (10316Dh)	**REG10316D**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[15:8]	7:0	See description of '10316Ch'.	
37h (10316Eh)	**REG10316E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[23:16]	7:0	See description of '10316Ch'.	
37h (10316Fh)	**REG10316F**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[31:24]	7:0	See description of '10316Ch'.	
38h (103170h)	**REG103170**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_SCALAR_FB_DIV2_EN	1		
	LPLL_NCO_RETIME_SEL	0	Retime NCO clock, 1'b0:enable, 1'b1:disable.	
39h (103172h)	**REG103172**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_TEST[7:0]	7:0	LPLL2_TEST.	
39h (103173h)	**REG103173**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_TEST[15:8]	7:0	See description of '103172h'.	
3Ah (103174h)	**REG103174**	**7:0**	**Default : 0x0C**	**Access : R/W**
	LPLL_RESERVED_DIV_J[3:0]	7:4	Reserved div sel.	
	OEN_FBIN	3		
	OEN_REFIN	2		
	LPLL1_RX_CLKFB_SEL	1		
	LPLL1_CLKIN_SEL	0		
3Ah (103175h)	**REG103175**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_RESERVED_DIV_M[3:0]	7:4	Reserved div sel.	
	LPLL_RESERVED_DIV_N[3:0]	3:0	Reserved div sel.	

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Bh ~ 3Ch (103176h ~ 103179h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Fh (10317Fh)	**REG10317F**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EN_HDMI	7	LPLL_EN_HDMI (project Cedric only).	
	-	6:0	Reserved.	
40h (103180h)	**REG103180**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_SYN_CLK_SEL	7		
	-	6:2	Reserved.	
	LPLL_EXT_INPUT_DIV_FIRST[1:0]	1:0		
40h (103181h)	**REG103181**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_INPUT_DIV_SECOND[7:0]	7:0		
41h (103182h)	**REG103182**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_EXT_LOOP_DIV_FIRST[1:0]	1:0		
41h (103183h)	**REG103183**	**7:0**	**Default : 0x03**	**Access : R/W**
	LPLL_EXT_LOOP_DIV_SECOND[7:0]	7:0		
42h (103184h)	**REG103184**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_EXT_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
43h (103186h)	**REG103186**	**7:0**	**Default : 0x2A**	**Access : R/W**
	-	7	Reserved.	
	LPLL_EXT_NCO_RETIME_SEL	6	1: Disable retime.	
	LPLL_EXT_PD	5	Power donw control to PLL (active high).	
	LPLL_EXT_IBIAS_ICTRL[2:0]	4:2		
	LPLL_EXT_ICP_ICTRL[1:0]	1:0	Lpll current control.	
43h (103187h)	**REG103187**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LPLL_EXT_HIGH_FLAG	7		
	LPLL_EXT_LOCK	6		
	-	5:1	Reserved.	
	LPLL_EXT_SSC_EN	0	SSC mode enable (extra).	
44h	**REG103188**	**7:0**	**Default : 0x00**	**Access : R/W**

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103188h)	-	7:4	Reserved.	
	LPLL_EXT_PHSEL[3:0]	3:0		
44h (103189h)	**REG103189**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL_EXT_COARSE_PHSEL[4:0]	4:0		
45h (10318Ah)	**REG10318A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_EXT_SCALAR_DIV_FIRST[1:0]	1:0		
45h (10318Bh)	**REG10318B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LPLL_EXT_SCALAR_DIV_SECOND[3:0]	3:0		
46h (10318Dh)	**REG10318D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LPLL_EXT_SKEW_DIV[2:0]	2:0		
48h (103190h)	**REG103190**	**7:0**	**Default : 0x44**	**Access : R/W**
	LPLL_EXT_SET[7:0]	7:0	Ext PLLSET.	
48h (103191h)	**REG103191**	**7:0**	**Default : 0x55**	**Access : R/W**
	LPLL_EXT_SET[15:8]	7:0	See description of '103190h'.	
49h (103192h)	**REG103192**	**7:0**	**Default : 0x24**	**Access : R/W**
	LPLL_EXT_SET[23:16]	7:0	See description of '103190h'.	
4Ah (103194h)	**REG103194**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_TEST[7:0]	7:0	LPLL_EXT_TEST.	
4Ah (103195h)	**REG103195**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_TEST[15:8]	7:0	See description of '103194h'.	
4Bh (103196h)	**REG103196**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_TEST[23:16]	7:0	See description of '103194h'.	
4Eh (10319Ch)	**REG10319C**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL_EXT_STEP[7:0]	7:0	Output PLL spread spectrum step (extra).	
4Eh (10319Dh)	**REG10319D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_EXT_STEP[9:8]	1:0	See description of '10319Ch'.	
4Fh (10319Eh)	**REG10319E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_SPAN[7:0]	7:0	Output PLL spread spectrum span (extra).	

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Fh (10319Fh)	**REG10319F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_EXT_SPAN[13:8]	5:0	See description of '10319Eh'.	
60h (1031C0h)	**REG1031C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LPLL1_VBYONE_DIV[2:0]	2:0	Lpll1 v-by-one divider.	
60h (1031C1h)	**REG1031C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_EN_VBYONE	7	Enable lpll1 v-by-one mode.	
	-	6:0	Reserved.	
70h (1031E0h)	**REG1031E0**	**7:0**	**Default : 0x80**	**Access : R/W**
	FSYNC_RESET_THRESH[7:0]	7:0	Fsync phase offset threshold.	
70h (1031E1h)	**REG1031E1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	EN_CLK_DIV	7	Enable lock freq mode.	
	-	6:4	Reserved.	
	EN_PLL_FSYNC_RESET	3	Enable fsync reset signal generate.	
	-	2	Reserved.	
	CLR_FSYNC_RESET_2T_FLAG	1	Clear fsync reset multi-time flag.	
	FSYNC_RESET_2T_FLAG	0	Fsync reset multi-times flag.	
72h (1031E4h)	**REG1031E4**	**7:0**	**Default : 0x00**	**Access : RO**
	IDCLK_DIV_PRD[7:0]	7:0	Input clock divider period in mclk.	
72h (1031E5h)	**REG1031E5**	**7:0**	**Default : 0x00**	**Access : RO**
	IDCLK_DIV_PRD[15:8]	7:0	See description of '1031E4h'.	
73h (1031E6h)	**REG1031E6**	**7:0**	**Default : 0x00**	**Access : RO**
	IDCLK_DIV_PRD[23:16]	7:0	See description of '1031E4h'.	
74h (1031E8h)	**REG1031E8**	**7:0**	**Default : 0x00**	**Access : RO**
	ODCLK_DIV_PRD[7:0]	7:0	Output clock divider period in mclk.	
74h (1031E9h)	**REG1031E9**	**7:0**	**Default : 0x00**	**Access : RO**
	ODCLK_DIV_PRD[15:8]	7:0	See description of '1031E8h'.	
75h (1031EAh)	**REG1031EA**	**7:0**	**Default : 0x00**	**Access : RO**
	ODCLK_DIV_PRD[23:16]	7:0	See description of '1031E8h'.	
7Eh (1031FCh)	**REG1031FC**	**7:0**	**Default : 0x00**	**Access : RO**
	F_RPT_CNT[7:0]	7:0	Input clock divider period in mclk.	
7Eh	**REG1031FD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

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LPLL_REG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1031FDh)	SPREADER_EN	7	Ivs spreader enable.	
	F_RPT_EN	6		
	PHASE_LOCK_THRESH_SEL[1:0]	5:4		
	F_RPT_CNT[11:8]	3:0	See description of '1031FCh'.	
7Fh (1031FEh)	**REG1031FE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SW_TRIG_DB_LOAD	1	Trig to load double buffer register.	
	DB_EN	0	Enable lpll register double.	
7Fh (1031FFh)	**REG1031FF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TGEN_SRC_SEL	0	Tgen source selection.	

CLKGEN1 Register (Bank = 1033)

CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (103300h)	**REG103300**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_DVBTM_TS_DIVNUM[4:0]	4:0	CLK_ATSC_DVB_DIV divider factor.	
00h (103301h)	**REG103301**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TSOUT_PH_TUN_EN	4	Enable Demod TS output clock phase tuning. 0: Disable. 1: Enable.	
	CKG_DEMOD_TEST_IN_EN	3	Enable external DEMOD Test-in clock. 0: Select internal ADC CLK. 1: Select external test-in clock.	
	CKG_DVBTM_TS_OUT_MODE	2	CLK_DEMOD_TS2PAD clock selection. 0: Select gated clock. 1: Select free-run clock.	
	CKG_ATSC_DVBTC_TS_INV	1	TSO_CLK (to pad) clock setting. 0: Normal phase to pad. 1: Invert phase to pad.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_ATSC_DVB_DIV_SEL	0	CLK_ATSC_DVB_DIV source selection. 0: Select clk_dmplldiv2. 1: Select clk_dmplldiv3.	
04h (103308h)	**REG103308**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_ATSC_TS[3:0]	3:0	CLK_ATSC_TS clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Clk_atsc_dvb_div. 01: 62 MHz. 10: 54 MHz. 11: Select XTAL.	
04h (103309h)	**REG103309**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DVBTC_TS[3:0]	3:0	CLK_DVBTC_TS clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Clk_atsc_dvb_div. 01: 62 MHz. 10: 54 MHz. 11: Reserved.	
05h (10330Bh)	**REG10330B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_TSOUT_PH_TUN_NUM[4:0]	4:0	Demod TS output clock phase tuning number. If (CKG_TSOUT_PH_TUN_NUM == reg_ckg_dvbtm_ts_divnum), Demod TS output clock is equal Demod TS internal working clock.	
0Ah (103314h)	**REG103314**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DVBTC_ADC[3:0]	3:0	CLK_DVBTC_ADC clock setting. [0]: Disable clock. [1]: Invert clock.	
0Dh (10331Ah)	**REG10331A**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_VIFDBB_DAC[3:0]	3:0	CLK_VIFDBB_DAC clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Clk_dmplldiv10. 01: Clk_dmplldiv10_div2. 10: From ADC_CLKOUT (clk_dmdadc_dac). 11: Reserved.	
0Dh (10331Bh)	**REG10331B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_VIFDBB_VDAC[3:0]	3:0	CLK_VIFDBB_VDAC clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Clk_dmplldiv10. 01: Clk_dmplldiv10_div2. 10: From ADC_CLKOUT (clk_dmdadc_dac). 11: Reserved.	
0Fh (10331Eh)	**REG10331E**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_DMDMCU[4:0]	4:0	CLK_DMDMCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: 172MHz. 001: 160HMz. 010: 144MHz. 011: 123MHz. 100: 108MHz. 101: Mem_clock. 110: Mem_clock div 2. 111: XTAL.	
12h (103324h)	**REG103324**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_FUART0_SYN[3:0]	3:0	CLK_FUART0_SYN clock setting. [1:0]: Select clock source. 00: 432 MHz. 01: MEMPLL_CLK. 10: XTALI_CLK. 11: FUART0_SYN_CLK.	
12h (103325h)	**REG103325**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_FUART1_SYN[3:0]	3:0	CLK_FUART1_SYN clock setting. [1:0]: Select clock source. 00: 432 MHz. 01: MEMPLL_CLK. 10: XTALI_CLK. 11: FUART1_SYN_CLK.	
13h (103326h)	**REG103326**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_FUART0[4:0]	4:0	CLK_FUART0 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK. 110: MEMPLL_CLK_DIV2. 111: FUART_SYTN_CLK.	
13h (103327h)	**REG103327**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_FUART1[4:0]	4:0	CLK_FUART1 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 172 MHz. 001: 160 MHz. 010: 144 MHz. 011: 123 MHz. 100: 108 MHz. 101: MEMPLL_CLK. 110: MEMPLL_CLK_DIV2. 111: FUART_SYTN_CLK.	
14h (103328h)	**REG103328**	**7:0**	**Default : 0xA9**	**Access : R/W**
	FUART_SYNTH0_NF[7:0]	7:0	Fuart0 synthesizer's divisor. [15:10] the integer part. [9:0] the deciamal part. Output clock = MPLL freq. / 6.10.	
14h (103329h)	**REG103329**	**7:0**	**Default : 0x45**	**Access : R/W**
	FUART_SYNTH0_NF[15:8]	7:0	See description of '103328h'.	
15h (10332Ah)	**REG10332A**	**7:0**	**Default : 0xA9**	**Access : R/W**
	FUART_SYNTH1_NF[7:0]	7:0	Fuart1 synthesizer's divisor. [15:10] the integer part. [9:0] the deciamal part. Output clock = MPLL freq. / 6.10.	
15h (10332Bh)	**REG10332B**	**7:0**	**Default : 0x45**	**Access : R/W**
	FUART_SYNTH1_NF[15:8]	7:0	See description of '10332Ah'.	
16h (10332Ch)	**REG10332C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FUART_SYNTH1_SW_RSTZ	3	Fuart1 synthesizer's reset. 0: Reset active. 1: Normal.	
	FUART_SYNTH0_SW_RSTZ	2	Fuart0 synthesizer's reset. 0: Reset active. 1: Normal.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FUART_SYNTH1_SW_EN	1	Fuart1 synthesizer's enable. 0: Disable. 1: Enable.	
	FUART_SYNTH0_SW_EN	0	Fuart0 synthesizer's enable. 0: Disable. 1: Enable.	
18h (103330h)	**REG103330**	**7:0**	**Default : 0x0D**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_MFE[3:0]	3:0	CLK_MFE clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 123 MHz. 01: 172 MHz. 10: 192 MHz. 11: 216 MHz.	
1Ch (103338h)	**REG103338**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DISP_IPATH[3:0]	3:0	CLK_DISP_IPATH clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Clk_vd_p. 01: 80 MHz. 10: Reserved. 11: Reserved.	
1Eh (10333Ch)	**REG10333C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_AUX[3:0]	3:0	CLK_AUX clock setting. [0]: Disable clock. [1]: Invert clock.	
20h (103340h)	**REG103340**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_GPU[4:0]	4:0	CLK_GPU clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. [4]: Deglitch free selection.	
21h (103342h)	**REG103342**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_SC2_PRE_IDCLK1[1:0]	5:4	CLK_SC2_PRE_IDCLK1 clock selection. 00: Clk_adc. 01: Clk_extdi. 10: Clk_extdi2. 11: Clk_vd_adc.	
	-	3:2	Reserved.	
	CKG_SC2_PRE_IDCLK0[1:0]	1:0	CLK_SC2_PRE_IDCLK0 clock selection. 00: Clk_adc. 01: Clk_extdi. 10: Clk_extdi2. 11: Clk_vd_adc.	
21h (103343h)	**REG103343**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_SC2_PRE_IDCLK2[1:0]	1:0	CLK_SC2_PRE_IDCLK2 clock selection. 00: Clk_adc. 01: Clk_extdi. 10: Clk_extdi2. 11: Clk_vd_adc.	
22h (103344h)	**REG103344**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_SC2_IDCLK0[4:0]	4:0	CLK_SC2_IDCLK0 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: Clk_sc2_idclk_f2. 001: Clk_lpll. 010: Clk_vd. 011: Clk_dc0. 100: Clk_odclk1. 101: Clk_icp. 110: Clk_odclk2. 111: Reserved.	
22h (103345h)	**REG103345**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_SC2_IDCLK1[4:0]	4:0	CLK_SC2_IDCLK1 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: Clk_sc2_idclk_f2. 001: Clk_lpll. 010: Clk_vd. 011: Clk_dc0. 100: Clk_odclk1. 101: Clk_icp. 110: Clk_odclk2. 111: Reserved.	
23h (103346h)	**REG103346**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_SC2_IDCLK2[4:0]	4:0	CLK_SC2_IDCLK2 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: Clk_sc2_idclk_f2. 001: Clk_lpll. 010: Clk_vd. 011: Clk_dc0. 100: Clk_odclk1. 101: Clk_icp. 110: Clk_odclk2. 111: Reserved.	
24h (103348h)	**REG103348**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SC2_FECLK_F2[3:0]	7:4	CLK_SC2_FECLK_F2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: 00: Clk_edclk. 01: Clk_fclk. 10: Reserved. 11: Reserved.	
	CKG_SC2_FECLK_F1[3:0]	3:0	CLK_SC2_FECLK_F1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: 00: Clk_edclk. 01: Clk_fclk. 10: Reserved. 11: Reserved.	
24h (103349h)	**REG103349**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SC1_FECLK2_F2[3:0]	7:4	CLK_SC1_FECLK_F2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: 00: Clk_edclk. 01: Clk_fclk. 10: Reserved. 11: Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_SC1_FECLK_F2[3:0]	3:0	CLK_SC1_FECLK_F1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: 00: Clk_edclk. 01: Clk_fclk. 10: Reserved. 11: Reserved.	
25h (10334Ah)	**REG10334A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_SC1_PRE_IDCLK0[1:0]	5:4	CLK_SC1_PRE_IDCLK0 clock selection. 00: Clk_adc. 01: Clk_extdi. 10: Clk_extdi2. 11: Clk_vd_adc.	
	-	3:2	Reserved.	
	CKG_ODCLK2[1:0]	1:0	CLK_ODCLK2 clock setting. [0]: Disable clock. [1]: Invert clock.	
25h (10334Bh)	**REG10334B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_SC1_PRE_IDCLK2[1:0]	1:0	CLK_SC1_PRE_IDCLK2 clock selection. 00: Clk_adc. 01: Clk_extdi. 10: Clk_extdi2. 11: Clk_vd_adc.	
26h (10334Ch)	**REG10334C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_SC1_IDCLK0[4:0]	4:0	CLK_SC1_IDCLK0 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: Clk_sc2_idclk_f2. 001: Clk_lpll. 010: Clk_vd. 011: Clk_dc0. 100: Clk_odclk1. 101: Clk_icp. 110: Clk_odclk2. 111: Reserved.	
26h (10334Dh)	**REG10334D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_SC1_IDCLK2[4:0]	4:0	CLK_SC2_IDCLK1 clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: Clk_sc2_idclk_f2. 001: Clk_lpll. 010: Clk_vd. 011: Clk_dc0. 100: Clk_odclk1. 101: Clk_icp. 110: Clk_odclk2. 111: Reserved.	
28h (103350h)	**REG103350**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	

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CLKGEN1 Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_GPD[4:0]	4:0	CLK_GPD clock setting. [0]: Disable clock. [1]: Invert clock. [4:2] : Select clock source. 000: 216 MHz. 001: 192 MHz. 010: 172 MHz. 011: 144 MHz. 100: 108 MHz. 101: Reserved. 110: Reserved. 111: Reserved.	
3Dh (10337Ah)	**REG10337A**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_R2_SECURE[3:0]	3:0	CLK_R2_SECURE clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] : Select clock source. 00: 240 MHz. 01: 192 MHz. 10: 172 MHz. 11: 144 MHz.	
3Eh ~ 3Fh (10337Ch ~ 10337Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

MAILBOX Register (Bank = 1033)

MAILBOX Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
80h (103300h)	**REG103300**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_0[7:0]	7:0	MAILBOX_0.	
80h (103301h)	**REG103301**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_0[15:8]	7:0	See description of '103300h'.	
81h	**REG103302**	**7:0**	**Default : 0x00**	**Access : R/W**

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MAILBOX Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103302h)	MB0_1[7:0]	7:0	MAILBOX_1.	
81h (103303h)	**REG103303**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1[15:8]	7:0	See description of '103302h'.	
82h (103304h)	**REG103304**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2[7:0]	7:0	MAILBOX_2.	
82h (103305h)	**REG103305**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2[15:8]	7:0	See description of '103304h'.	
83h (103306h)	**REG103306**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_3[7:0]	7:0	MAILBOX_3.	
83h (103307h)	**REG103307**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_3[15:8]	7:0	See description of '103306h'.	
84h (103308h)	**REG103308**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_4[7:0]	7:0	MAILBOX_4.	
84h (103309h)	**REG103309**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_4[15:8]	7:0	See description of '103308h'.	
85h (10330Ah)	**REG10330A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_5[7:0]	7:0	MAILBOX_5.	
85h (10330Bh)	**REG10330B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_5[15:8]	7:0	See description of '10330Ah'.	
86h (10330Ch)	**REG10330C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_6[7:0]	7:0	MAILBOX_6.	
86h (10330Dh)	**REG10330D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_6[15:8]	7:0	See description of '10330Ch'.	
87h (10330Eh)	**REG10330E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_7[7:0]	7:0	MAILBOX_7.	
87h (10330Fh)	**REG10330F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_7[15:8]	7:0	See description of '10330Eh'.	
88h (103310h)	**REG103310**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_8[7:0]	7:0	MAILBOX_8.	
88h (103311h)	**REG103311**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_8[15:8]	7:0	See description of '103310h'.	
89h (103312h)	**REG103312**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_9[7:0]	7:0	MAILBOX_9.	

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MAILBOX Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
89h (103313h)	**REG103313**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_9[15:8]	7:0	See description of '103312h'.	
8Ah (103314h)	**REG103314**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_A[7:0]	7:0	MAILBOX_10.	
8Ah (103315h)	**REG103315**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_A[15:8]	7:0	See description of '103314h'.	
8Bh (103316h)	**REG103316**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_B[7:0]	7:0	MAILBOX_11.	
8Bh (103317h)	**REG103317**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_B[15:8]	7:0	See description of '103316h'.	
8Ch (103318h)	**REG103318**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_C[7:0]	7:0	MAILBOX_12.	
8Ch (103319h)	**REG103319**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_C[15:8]	7:0	See description of '103318h'.	
8Dh (10331Ah)	**REG10331A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_D[7:0]	7:0	MAILBOX_13.	
8Dh (10331Bh)	**REG10331B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_D[15:8]	7:0	See description of '10331Ah'.	
8Eh (10331Ch)	**REG10331C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_E[7:0]	7:0	MAILBOX_14.	
8Eh (10331Dh)	**REG10331D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_E[15:8]	7:0	See description of '10331Ch'.	
8Fh (10331Eh)	**REG10331E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_F[7:0]	7:0	MAILBOX_15.	
8Fh (10331Fh)	**REG10331F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_F[15:8]	7:0	See description of '10331Eh'.	
90h (103320h)	**REG103320**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_10[7:0]	7:0	MAILBOX_16.	
90h (103321h)	**REG103321**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_10[15:8]	7:0	See description of '103320h'.	
91h (103322h)	**REG103322**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_11[7:0]	7:0	MAILBOX_17.	
91h	**REG103323**	**7:0**	**Default : 0x00**	**Access : R/W**

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MAILBOX Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103323h)	MB0_11[15:8]	7:0	See description of '103322h'.	
92h (103324h)	**REG103324**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_12[7:0]	7:0	MAILBOX_18.	
92h (103325h)	**REG103325**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_12[15:8]	7:0	See description of '103324h'.	
93h (103326h)	**REG103326**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_13[7:0]	7:0	MAILBOX_19.	
93h (103327h)	**REG103327**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_13[15:8]	7:0	See description of '103326h'.	
94h (103328h)	**REG103328**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_14[7:0]	7:0	MAILBOX_20.	
94h (103329h)	**REG103329**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_14[15:8]	7:0	See description of '103328h'.	
95h (10332Ah)	**REG10332A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_15[7:0]	7:0	MAILBOX_21.	
95h (10332Bh)	**REG10332B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_15[15:8]	7:0	See description of '10332Ah'.	
96h (10332Ch)	**REG10332C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_16[7:0]	7:0	MAILBOX_22.	
96h (10332Dh)	**REG10332D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_16[15:8]	7:0	See description of '10332Ch'.	
97h (10332Eh)	**REG10332E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_17[7:0]	7:0	MAILBOX_23.	
97h (10332Fh)	**REG10332F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_17[15:8]	7:0	See description of '10332Eh'.	
98h (103330h)	**REG103330**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_18[7:0]	7:0	MAILBOX_24.	
98h (103331h)	**REG103331**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_18[15:8]	7:0	See description of '103330h'.	
99h (103332h)	**REG103332**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_19[7:0]	7:0	MAILBOX_25.	
99h (103333h)	**REG103333**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_19[15:8]	7:0	See description of '103332h'.	

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MAILBOX Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
9Ah (103334h)	**REG103334**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1A[7:0]	7:0	MAILBOX_26.	
9Ah (103335h)	**REG103335**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1A[15:8]	7:0	See description of '103334h'.	
9Bh (103336h)	**REG103336**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1B[7:0]	7:0	MAILBOX_27.	
9Bh (103337h)	**REG103337**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1B[15:8]	7:0	See description of '103336h'.	
9Ch (103338h)	**REG103338**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1C[7:0]	7:0	MAILBOX_28.	
9Ch (103339h)	**REG103339**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1C[15:8]	7:0	See description of '103338h'.	
9Dh (10333Ah)	**REG10333A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1D[7:0]	7:0	MAILBOX_29.	
9Dh (10333Bh)	**REG10333B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1D[15:8]	7:0	See description of '10333Ah'.	
9Eh (10333Ch)	**REG10333C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1E[7:0]	7:0	MAILBOX_30.	
9Eh (10333Dh)	**REG10333D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1E[15:8]	7:0	See description of '10333Ch'.	
9Fh (10333Eh)	**REG10333E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1F[7:0]	7:0	MAILBOX_31.	
9Fh (10333Fh)	**REG10333F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1F[15:8]	7:0	See description of '10333Eh'.	
A0h (103340h)	**REG103340**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_20[7:0]	7:0	MAILBOX_32.	
A0h (103341h)	**REG103341**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_20[15:8]	7:0	See description of '103340h'.	
A1h (103342h)	**REG103342**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_21[7:0]	7:0	MAILBOX_33.	
A1h (103343h)	**REG103343**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_21[15:8]	7:0	See description of '103342h'.	
A2h	**REG103344**	**7:0**	**Default : 0x00**	**Access : R/W**

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MAILBOX Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103344h)	MB0_22[7:0]	7:0	MAILBOX_34.	
A2h (103345h)	**REG103345**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_22[15:8]	7:0	See description of '103344h'.	
A3h (103346h)	**REG103346**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_23[7:0]	7:0	MAILBOX_35.	
A3h (103347h)	**REG103347**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_23[15:8]	7:0	See description of '103346h'.	
A4h (103348h)	**REG103348**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_24[7:0]	7:0	MAILBOX_36.	
A4h (103349h)	**REG103349**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_24[15:8]	7:0	See description of '103348h'.	
A5h (10334Ah)	**REG10334A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_25[7:0]	7:0	MAILBOX_37.	
A5h (10334Bh)	**REG10334B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_25[15:8]	7:0	See description of '10334Ah'.	
A6h (10334Ch)	**REG10334C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_26[7:0]	7:0	MAILBOX_38.	
A6h (10334Dh)	**REG10334D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_26[15:8]	7:0	See description of '10334Ch'.	
A7h (10334Eh)	**REG10334E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_27[7:0]	7:0	MAILBOX_39.	
A7h (10334Fh)	**REG10334F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_27[15:8]	7:0	See description of '10334Eh'.	
A8h (103350h)	**REG103350**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_28[7:0]	7:0	MAILBOX_40.	
A8h (103351h)	**REG103351**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_28[15:8]	7:0	See description of '103350h'.	
A9h (103352h)	**REG103352**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_29[7:0]	7:0	MAILBOX_41.	
A9h (103353h)	**REG103353**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_29[15:8]	7:0	See description of '103352h'.	
AAh (103354h)	**REG103354**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2A[7:0]	7:0	MAILBOX_42.	

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MAILBOX Register (Bank = 1033)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
AAh (103355h)	**REG103355**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2A[15:8]	7:0	See description of '103354h'.	
ABh (103356h)	**REG103356**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2B[7:0]	7:0	MAILBOX_43.	
ABh (103357h)	**REG103357**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2B[15:8]	7:0	See description of '103356h'.	
ACh (103358h)	**REG103358**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2C[7:0]	7:0	MAILBOX_44.	
ACh (103359h)	**REG103359**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2C[15:8]	7:0	See description of '103358h'.	
ADh (10335Ah)	**REG10335A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2D[7:0]	7:0	MAILBOX_45.	
ADh (10335Bh)	**REG10335B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2D[15:8]	7:0	See description of '10335Ah'.	
AEh (10335Ch)	**REG10335C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2E[7:0]	7:0	MAILBOX_46.	
AEh (10335Dh)	**REG10335D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2E[15:8]	7:0	See description of '10335Ch'.	
AFh (10335Eh)	**REG10335E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2F[7:0]	7:0	MAILBOX_47.	
AFh (10335Fh)	**REG10335F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2F[15:8]	7:0	See description of '10335Eh'.	

VDMCU51_IF Register (Bank = 1034)

VDMCU51_IF Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (103460h)	**REG103460**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	VDMCU_RST	0	set: Reset VD MCU51; default => reset VD MCU51.	
30h (103461h)	**REG103461**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

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VDMCU51_IF Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VDMCU_SRAM_EN	0	set: Enable VD MCU51 SRAM.	
31h (103462h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
31h (103463h)	**REG103463**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY[3:0]	7:4	Set as 0x5 to enable "vdmcu51_if".	
	-	3:2	Reserved.	
	HK2VD_INT	1	set: Assert interrupt to VD MCU51.	
	ADDR_AUTO_INC	0	set: Address will auto-increase when Read/Write "reg_sram_data".	
32h (103464h)	**REG103464**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDR[7:0]	7:0	VD MCU 51 code sram ADDRess. Note: Auto-increase when "ADDR_auto_inc" is set and write "reg_sram_wd" or read "reg_sram_rd". PS: Do not read h0005 and h0007 by MS TV tool, or it may be incresed.	
32h (103465h)	**REG103465**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDR[15:8]	7:0	See description of '103464h'.	
36h (10346Ch)	**REG10346C**	**7:0**	**Default : 0x00**	**Access : WO**
	SRAM_WD[7:0]	7:0	Write: Write data to VD MCU 51 code sram.	
38h (103470h)	**REG103470**	**7:0**	**Default : 0x00**	**Access : RO**
	SRAM_RD[7:0]	7:0	Read: Read data from VD MCU 51 code sram.	

URDMA Register (Bank = 1034)

URDMA Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (1034C0h)	**REG1034C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_SW_RST	7	RX Engine software reset. 0: De-assert. 1: Assert.	
	TX_SW_RST	6	TX Engine software reset. 0: De-assert. 1: Assert.	

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URDMA Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RX_ENDINA	5	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	TX_ENDINA	4	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	RX_URDMA_EN	3	URDMA RX Hardware Enable. 0: Disable. 1: Enable.	
	TX_URDMA_EN	2	URDMA TX Hardware Enable. 0: Disable. 1: Enable.	
	URDMA_MODE	1	URDMA Mode selects, when mode enable, URDMA hardware will replace MCU to access UART, otherwise MCU still control UART directly. 0: Disable. 1: Enable.	
	SW_RST	0	URDMA software reset. 0: De-assert. 1: Assert.	
60h (1034C1h)	**REG1034C1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	RX_BUSY	5	RX controller in BUSY state.	
	TX_BUSY	4	TX controller in BUSY state.	
	RX_OP_MODE	3	RX controller operation mode. 0: Default. 1: Stop RX DMA activity when threshold interrupt occurs, until update RX_BUF_BASE.	
	-	2:0	Reserved.	
61h (1034C2h)	**REG1034C2**	**7:0**	**Default : 0x40**	**Access : R/W**
	INTR_THRESHOLD[7:0]	7:0	Interrupt threshold, to configure interrupt MCU period. Setting how much. Data received from UART, and alert MCU, byte unit.	
61h (1034C3h)	**REG1034C3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INTR_THRESHOLD[11:8]	3:0	See description of '1034C2h'.	

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URDMA Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (1034C4h)	**REG1034C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_H[7:0]	7:0	Configure TX buffer base address[26:16] in DRAM, 8byte unit.	
62h (1034C5h)	**REG1034C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TX_BUF_BASE_H[10:8]	2:0	See description of '1034C4h'.	
63h (1034C6h)	**REG1034C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[7:0]	7:0	Configure TX buffer base address[15:0] in DRAM, 8byte unit.	
63h (1034C7h)	**REG1034C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[15:8]	7:0	See description of '1034C6h'.	
64h (1034C8h)	**REG1034C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_SIZE[7:0]	7:0	Configure TX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
64h (1034C9h)	**REG1034C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TX_BUF_SIZE[12:8]	4:0	See description of '1034C8h'.	
65h (1034CAh)	**REG1034CA**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[7:0]	7:0	Read TX buffer read pointer from URDMA, byte unit.	
65h (1034CBh)	**REG1034CB**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[15:8]	7:0	See description of '1034CAh'.	
66h (1034CCh)	**REG1034CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[7:0]	7:0	Update TX buffer write pointer to URDMA, byte unit.	
66h (1034CDh)	**REG1034CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[15:8]	7:0	See description of '1034CCh'.	
67h (1034CEh)	**REG1034CE**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	TX_TIMEOUT[3:0]	3:0	Configure TX time out value, to clean TX buffer data and send to UART. 2^(TX_TIMEOUT) Cycle unit.	
68h (1034D0h)	**REG1034D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_H[7:0]	7:0	Configure RX buffer base address[26:16] in DRAM, 8byte unit.	

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URDMA Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
68h (1034D1h)	**REG1034D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RX_BUF_BASE_H[10:8]	2:0	See description of '1034D0h'.	
69h (1034D2h)	**REG1034D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[7:0]	7:0	Configure RX buffer base address[15:0] in DRAM, 8byte unit.	
69h (1034D3h)	**REG1034D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[15:8]	7:0	See description of '1034D2h'.	
6Ah (1034D4h)	**REG1034D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_SIZE[7:0]	7:0	Configure RX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
6Ah (1034D5h)	**REG1034D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RX_BUF_SIZE[12:8]	4:0	See description of '1034D4h'.	
6Bh (1034D6h)	**REG1034D6**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[7:0]	7:0	Read RX buffer write pointer from URDMA, byte unit.	
6Bh (1034D7h)	**REG1034D7**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[15:8]	7:0	See description of '1034D6h'.	
6Ch (1034D8h)	**REG1034D8**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	RX_TIMEOUT[3:0]	3:0	Configure RX time out value, to clean UART RX FIFO and write to DRAM. 2^(RX_TIMEOUT) Cycle unit.	
6Dh (1034DAh)	**REG1034DA**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RX_MCU_INTR	7	Identify rx controller to MCU interrupt event, this bit is logical OR of RX_INTR1~2 flag, and clear by RX_INTR_CLR.	
	RESERVE2	6	Reserve.	
	RX_INTR2	5	Identify Rx interrupt is cause by interrupt threshold function.	
	RX_INTR1	4	Identify Rx interrupt is cause by timeout function.	
	RESERVE1	3	Reserve.	
	RX_INTR2_EN	2	Rx interrupt threshold function enable.	

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URDMA Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RX_INTR1_EN	1	Rx timeout interrupt function enable.	
	RX_INTR_CLR	0	MCU clear rx control interrupt signal. Once write and auto clear.	
6Dh (1034DBh)	**REG1034DB**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TX_MCU_INTR	7	Identify tx controller to MCU interrupt event.	
	RESERVE3[4:0]	6:2	Reserve.	
	TX_INTR_EN	1	TX controller to MCU interrupt enable.	
	TX_INTR_CLR	0	MCU clear tx control interrupt signal. Once write and auto clear.	
6Eh (1034DCh)	**REG1034DC**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[7:0]	7:0	Reserve.	
6Eh (1034DDh)	**REG1034DD**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[15:8]	7:0	See description of '1034DCh'.	
6Fh (1034DEh)	**REG1034DE**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[7:0]	7:0	Reserve.	
6Fh (1034DFh)	**REG1034DF**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[15:8]	7:0	See description of '1034DEh'.	
70h (1034E0h)	**REG1034E0**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	RESERVE6[4:0]	7:3	Reserve.	
	PREFCH_CLK_GATE1	2	Gated clock MINF post-write module. 0: Clock enable. 1: Clock gated.	
	PREFCH_CLK_GATE	1	Gated clock MINF pre-fetch module. 0: Clock enable. 1: Clock gated.	
	MINF_SW_RSTZ	0	MINF pre-fetch / post-write module SW reset. 0: SW reset. 1: Normal.	
70h (1034E1h)	**REG1034E1**	**7:0**	**Default : 0x00**	**Access : RO**
	POSTWR_BUSY	7	Identify MINF post write in busy state.	
	RESERVE6[11:5]	6:0	See description of '1034E0h'.	
71h (1034E2h)	**REG1034E2**	**7:0**	**Default : 0x46**	**Access : R/W**
	PREFCH_PATCH	7	SW patch control bit.	

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URDMA Register (Bank = 1034)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PREFCH_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	PREFCH_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	PREFCH_PRI	3	Define DRAM access priority.	
	PREFCH_RASTRD	2	MINF pre-fetch fast read enable.	
	PREFCH_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	PREFCH_CLR	0	SW clear MINF pre-fetch buffer. 0: Normal. 1: Clear.	
71h (1034E3h)	**REG1034E3**	**7:0**	**Default : 0x46**	**Access : R/W**
	POSTWR_FLUSH1_PATCH	7	SW flush path.	
	POSTWR_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	POSEWR_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	POSTWR_PRI	3	Define DRAM access priority.	
	POSTWR_FLUSH1	2	SW flush path.	
	POSTWR_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	POSTWR_FLUSH	0	SW flush MINF post write buffer. 0: Normal. 1: Flush.	

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AFEC Register (Bank = 1035)

AFEC Register (Bank = 1035)				
Index	**Mnemonic**	**Bit**	**Description**	
34h	**REG34**	**7:0**	**Default : 0x40**	**Access : R/W**
	SVIDEO_EN	7	0: Chroma source from CVBS-channel input; 1:chroma source from C-channel input.	
	ADC_C_ALWAYS_ON	6	Chroma ADC 16fsc-to-4fsc down-sampling is enabled.	
	-	5:0	Reserved.	
D6h	**REGD6**	**7:0**	**Default : 0xAA**	**Access : R/W**
	-	7:3	Reserved.	
	VCR_TH[2:0]	2:0	Move to SW.	
D8h	**REGD8**	**7:0**	**Default : 0xF0**	**Access : R/W**
	VCR_PRECOAST[3:0]	7:4	DPLL coast.	
	HV_HSLISEL_VCR[1:0]	3:2		
	HV_SLILOW_SEL[1:0]	1:0		
DAh	**REGDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED8[7:0]	7:0	Move to SW.	
DEh	**REGDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	LINE_START_VF_SEL[1:0]	7:6	Line start V half line.	
	-	5:0	Reserved.	
EAh	**REGEA**	**7:0**	**Default : 0x40**	**Access : R/W**
	656_SET_CLR_OP	7	ITU_656_V set/clear behaviour option. 0: Original. 1: Another way to avoid long ITU_656_V interval.	
	656_OFST[6:0]	6:0		
ECh	**REGEC**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	DBCLK_TEST	4		
	-	3	Reserved.	
	656_BLANK_MODE	2		
	656_EN	1		
	-	0	Reserved.	
EEh	**REGEE**	**7:0**	**Default : 0x02**	**Access : R/W**
	656_BLANK_MAX[7:0]	7:0		
F0h	**REGF0**	**7:0**	**Default : 0x00**	**Access : R/W**

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AFEC Register (Bank = 1035)

Index	Mnemonic	Bit	Description	
	YUV[7:0]	7:0	Used as input of the 4fsc-to-16fsc up-sampling if REG_SELUPS=3.	
F2h	**REGF2**	**7:0**	**Default : 0x18**	**Access : R/W**
	656_HDES_O_9_2[7:0]	7:0	BT656 SAV position. For VCR, 656_HDES = 656_HDES_o - 656_HDES_VCR_OFST * 4. Otherwise, 656_HDES = 656_HDES_o.	
F4h	**REGF4**	**7:0**	**Default : 0x20**	**Access : R/W**
	656_HDES_O_1_0[1:0]	7:6		
	-	5:0	Reserved.	
FEh	**REGFE**	**7:0**	**Default : 0x61**	**Access : R/W**
	-	7:6	Reserved.	
	3DAC_INSHV	5	Insert HV into display DAC source.	
	3DAC_HSEL	4	Insert H's source selection; 0: windowPLL; 1: display PLL.	
	3DAC_INSBLACK	3	Insert black level back to DAC source.	
	SELFB	2	0: YCbCr source from comb444; 1: YCbCr source from AFEC testmode.	
	SELUPS[1:0]	1:0	Upsampling source; 00: Comb YC; 01: YCbCr; 10: VD_Mix; 11: Debug;	
18h	**REG18**	**7:0**	**Default : 0x4A**	**Access : R/W**
	TEST_Y[7:0]	7:0		
1Eh	**REG1E**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:4	Reserved.	
	FSC_TABLE_3_2[1:0]	3:2	Frequency synthesizer base. 0: 160MHz. 1: 15*14.31818MHz. 2: 216Mhz. 3: 15*14.31818MHz. Only valid for REG_FSC_TABLE[4] = 1.	
	FSC_TABLE_1_0[1:0]	1:0	Frequency synthesizer output. 0: 4*fsc. 1: 8*fsc. 2: 16*fsc. 3: 16*fsc.	
28h	**REG28**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:1	Reserved.	

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AFEC Register (Bank = 1035)				
Index	**Mnemonic**	**Bit**	**Description**	
	RESERVED9	0	Reserved for future usage.	
2Ah	**REG2A**	**7:0**	**Default : 0x2A**	**Access : R/W**
	SPL_SPD_NOISY[1:0]	7:6	Coarse hsync pll tracking speed for noisy signal.	
	SPL_SPD_VCR[1:0]	5:4	Coarse hsync pll phase tracking speed for VCR outside vsync..	
	SPL_SPD_VCR_V[1:0]	3:2	Coarse hsync pll phase tracking speed for VCR during vsync.	
	-	1:0	Reserved.	
36h	**REG36**	**7:0**	**Default : 0x10**	**Access : R/W**
	RESERVED12[1:0]	7:6		
	-	5:0	Reserved.	
C6h	**REGC6**	**7:0**	**Default : 0x90**	**Access : R/W**
	APL_COMB_LL_FREQ_EN	7		
	-	6:0	Reserved.	

COMB Register (Bank = 1036)

COMB Register (Bank = 1036)				
Index	**Mnemonic**	**Bit**	**Description**	
20h	**REG20**	**7:0**	**Default : 0x17**	**Access : R/W**
	SVDOIN	7	S-video input.	
	SVDOCBP	6	Band pass filter for S-vidoe C channel.	
	DIRADCIN	5	Direct use ADC input(bypass AFEC).	
	NEW_COMB_EN	4	New Comb enable.	
	MANUCOMB	3	0/1 -> auto/manu select working mode.	
	WORKMD[2:0]	2:0	Working mode: 0/1: 1D, 2: 2D, 3: 3D, other: Enhanced 3D.	
22h	**REG22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CRMAOFF	1	Chroma off.	
	BSTOFF	0	Burst off.	
24h	**REG24**	**7:0**	**Default : 0x18**	**Access : R/W**
	FREESYNC	7	H/V sync free run.	
	FREECNTMD	6	Free run counter mode, 0/1 -> NTSC/PAL.	
	SNOWTYPE[1:0]	5:4	Snow Type, 0: never, 1: auto, 2: force.	
	VWINPOS[3:0]	3:0	Vertical window position.	

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COMB Register (Bank = 1036)

Index	Mnemonic	Bit	Description	
26h	**REG26**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:6	Reserved.	
	DEMO3DMD[1:0]	5:4	2D/3D demo mode. 0x: Off. 10: 2D/3D. 11: 3D/2D.	
	-	3:2	Reserved.	
	PKTMD[1:0]	1:0	Packet mode, 0/1/2 -> 64/128/256 pixels per packet.	
28h	**REG28**	**7:0**	**Default : 0x88**	**Access : R/W**
	HSTRATIO[2:0]	7:5	History ratio.	
	NRLEVEL[4:0]	4:0	Noise reduction strength.	
2Ah	**REG2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ETPXVEN	3	Extra vertical entropy enable.	
	SEPETPV	2	Separate vertical entropy.	
	LP2DYMD[1:0]	1:0	Low pass mode of 2D - Y. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
2Ch	**REG2C**	**7:0**	**Default : 0x70**	**Access : R/W**
	BNDOF2D3D[7:0]	7:0	Boundary of 2D/3D demo mode.	
2Eh	**REG2E**	**7:0**	**Default : 0xC0**	**Access : R/W**
	HORSTPOS[7:0]	7:0	3D window horizontal starting position, 0..255 -> -128..127.	
30h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h	**REG32**	**7:0**	**Default : 0x8D**	**Access : R/W**
	FREEHTOT_LOW[7:0]	7:0	Free run HSync total (L).	
34h	**REG34**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	FREEHTOT_HIGH[3:0]	3:0	Free run HSync total (H).	
36h	**REG36**	**7:0**	**Default : 0x83**	**Access : R/W**
	PHSDETEN	7	Line-lock phase detection enable.	
	PHSDETINV	6	Output inverse.	
	NEWLLEN	5	New line lock enable(for no burst).	

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COMB Register (Bank = 1036)				
Index	**Mnemonic**	**Bit**	**Description**	
	SCLR_DO_DEM	4	New comb do dem disable.	
	PAL_CMP_INV	3	New_comb pal cmp up inverse bit.	
	PHSDETSFT[2:0]	2:0	Shift-right bit number.	
38h	**REG38**	**7:0**	**Default : 0xEC**	**Access : R/W**
	HSFRAFEC	7	H sync from AFEC.	
	VSFRAFEC	6	V sync from AFEC.	
	BLKFRAFEC	5	Black level from AFEC(MCU).	
	-	4	Reserved.	
	LNFRMCU	3	525/625 line information from MCU.	
	FREQFRMCU	2	3.58/4.43 MHz information from MCU.	
	STDSEL[1:0]	1:0	NTSC/PAL decision. 00: From MCU. 01: Force NTSC. 10: Force PAL. 11: From AFEC.	
40h	**REG40**	**7:0**	**Default : 0x67**	**Access : R/W**
	-	7	Reserved.	
	YNCHMD[2:0]	6:4	Notch mode of Y.	
	MANUCAN3D	3	Bypass Can3DMd for debugging.	
	CNCHMD[2:0]	2:0	Notch mode of C.	
42h	**REG42**	**7:0**	**Default : 0x81**	**Access : R/W**
	-	7:4	Reserved.	
	CRMAFLTMD[1:0]	3:2	Chroma filter mode. 00: Off. 01: Band pass. 10: Median type A. 11: Median type B.	
	CDEMCHK[1:0]	1:0	Chroma vertical check(dem). 00: Off. 01: PAL only. 1x: Always do.	
44h	**REG44**	**7:0**	**Default : 0x86**	**Access : R/W**
	-	7:4	Reserved.	
	NEWMOTYSEL	3	New Motion Y Selection.	
	NEWMOTYDIFFSEL	2	New Motion Y Difference Selection.	
	STLMD_ECO[1:0]	1:0	Still mode selection.	

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COMB Register (Bank = 1036)				
Index	**Mnemonic**	**Bit**	**Description**	
46h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
48h	**REG48**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	3DMOTDET5F	1	3D motion detection use 5 frames.	
	-	0	Reserved.	
5Ch	**REG5C**	**7:0**	**Default : 0x0C**	**Access : R/W**
	THDEM[7:0]	7:0	Threshold for 2D comb filter,Check seperated. Chroma complement with up/down line or not.	
5Eh	**REG5E**	**7:0**	**Default : 0xF8**	**Access : R/W**
	NEWMOTYTH[3:0]	7:4	New Motion Y Threshold.	
	DEMOFFSET[3:0]	3:0	Threshold for 2D comb filter,Check seperated. Chroma complement with up/down line or not.	
60h	**REG60**	**7:0**	**Default : 0xA7**	**Access : R/W**
	MOTXEN	7	Extra reference of motion detection. 1DH Y diff or 1DH Y+C diff.	
	MOTXSEL	6	Extra motion mode. 1: Y+C, 0:Y only.	
	MOTZEN	5	Ultra reference of motion detection. Patch NTSC only = time domain 2 frame CVBS diff & spatial domain 2 tapes LP. Actually it's like spation LP get Y then time domain 2 consecutive frame do Y subtraction.	
	LONG3D	4	Using 5 frame do y/c separate.	
	MOTMD[1:0]	3:2	Motion different mode select. 0: Motion X (1DH Y or Y+C diff). 1: LPF of motion X. 2: Min of motion X. 3: Max of motion X.	
	DYNTHMD[1:0]	1:0	Dynamic threshold mode. 1: Enable motion vector X2 (actually modify motion vector if 2D entropy < reg3A dynamic threshold). 2: Enable motion vector X4 (actually modify motion vector if 2D entropy < 1/2 * reg3A dynamic threshold). 3: Enable motion vector X8 (actually modify motion vector if 2D entropy < 1/4 *reg3A dynamic threshold).	
62h	**REG62**	**7:0**	**Default : 0x20**	**Access : R/W**

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Index	**Mnemonic**	**Bit**	**Description**	
	MOTYTHU[7:0]	7:0	Upper bound motionY threshold.	
64h	**REG64**	**7:0**	**Default : 0x10**	**Access : R/W**
	MOTYTHL[7:0]	7:0	Lower bound motionY threshold.	
66h	**REG66**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTCTHU[7:0]	7:0	Upper bound motionC threshold.	
68h	**REG68**	**7:0**	**Default : 0x10**	**Access : R/W**
	MOTCTHL[7:0]	7:0	Lower bound motionC threshold.	
6Ah	**REG6A**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTTHX[7:0]	7:0	Extra motion threshold.	
6Ch	**REG6C**	**7:0**	**Default : 0x30**	**Access : R/W**
	MOTTHZ[7:0]	7:0	Z-Extra motion threshold.	
6Eh	**REG6E**	**7:0**	**Default : 0x8C**	**Access : R/W**
	STLDET	7	Still image detection enable.	
	STLTH[6:0]	6:0	Still threshold.	
70h	**REG70**	**7:0**	**Default : 0x04**	**Access : R/W**
	MFMODE[1:0]	7:6	Motion factor mode(max/avg/MotY/MotC). (source motion factor is the same, but after Luma/Chroma different threshold will get MotY, MotC, max = max(MotY, MotC).	
	PAL3D_FLT_SEL	5	0: LPF of (CVBS difference) MAXof (CVBS difference) in specital domain.	
	PAL3D_DIFF_SEL	4	0: CVBS difference of F4-F3 or F4-F1 in time domain (F4: current frame). 1: MAX(F4-F3, F4-F1) in time domain.	
	COMB_3DETPC_SEL	3	Use chroma diff for 3D entropy calculation.	
	STDTRSP[2:0]	2:0	Still image detect reponse time, 0: 1 field, 1: 2 field, 7: 128 field.	
72h	**REG72**	**7:0**	**Default : 0x02**	**Access : R/W**
	STLBK[7:0]	7:0	Motion level go back when find motion once.	
74h	**REG74**	**7:0**	**Default : 0x30**	**Access : R/W**
	DYNTH[7:0]	7:0	Dynamic motion threshold.	
76h	**REG76**	**7:0**	**Default : 0x00**	**Access : R/W**
	NOISELVL[7:0]	7:0	Noise level for dynamic motion detection.	
78h	**REG78**	**7:0**	**Default : 0x2F**	**Access : R/W**
	NEWMOTYEN	7	New Motion Y Enable.	

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	NEWMOTCEN	6	New Motion C Enable.	
	NEWMOTCGAIN[1:0]	5:4	New Motion C Gain.	
	NEWMOTCTH[3:0]	3:0	New Motion C Threshold.	
7Ah	**REG7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMBASEADRH[7:0]	7:0	Base address of DRAM request.(H).	
7Ch	**REG7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMBASEADRM[7:0]	7:0	Base address of DRAM request.(M).	
7Eh	**REG7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMBASEADRL[7:0]	7:0	Base address of DRAM request.(L).	
80h	**REG80**	**7:0**	**Default : 0x94**	**Access : R/W**
	-	7:3	Reserved.	
	BLNKDETMD	2	Blank level detect mode, 0: Either 240 or 252, 1: 230~262 is possible.	
	VDETMD[1:0]	1:0	Vertical timing detect mode. 0x: Auto. 10: Force 525 line. 11: Force 625 line.	
82h	**REG82**	**7:0**	**Default : 0x08**	**Access : R/W**
	SENSSIGDET[7:0]	7:0	Sensitivity of signal detect.	
84h	**REG84**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SYNCLVLTLRN[7:0]	7:0	Sync level tolerance.	
86h	**REG86**	**7:0**	**Default : 0x60**	**Access : R/W**
	VCRCOASTLEN[7:0]	7:0	VCR coast length.	
88h	**REG88**	**7:0**	**Default : 0x80**	**Access : R/W**
	HBIDLY[7:0]	7:0	Horizontal blanking region position.	
8Ah	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
8Eh	**REG8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTIFIR_GPATCH_COR[3:0]	7:4	CTI FIR Gray Patch Coring (val*2).	
	CTIFIR_GPATCH_GAIN[1:0]	3:2	CTI FIR Gray Patch Gain (0.25/0.5/1/2).	
	CTIFIR_GPATCH_MD[1:0]	1:0	CTI FIR Gray Patch Mode ([0]: Off [1]:30% [2]: 60% [3]:100%).	
90h	**REG90**	**7:0**	**Default : 0x20**	**Access : R/W**
	YCPIPE[1:0]	7:6	Y/C pipe delay.	
	DEGPIPE[1:0]	5:4	Degree pipe delay.	

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	-	3:0	Reserved.	
92h	**REG92**	**7:0**	**Default : 0x01**	**Access : R/W**
	IAN_MAXEV2_GAIN[1:0]	7:6	T-CrossH: V2 entropy gain selection.	
	IAN_MAXEV1_GAIN[1:0]	5:4	T-CrossH: V1 entropy gain selection.	
	-	3:1	Reserved.	
	IAN_EH_EN	0	H-direction T cross patch enable.	
94h	**REG94**	**7:0**	**Default : 0x56**	**Access : R/W**
	CTIFIR_GAIN[3:0]	7:4	CTI FIR Gain (1/2/3/4/6/8/12/16/24/32/48/64/96/128).	
	-	3	Reserved.	
	CTIFIR_MD[1:0]	2:1	CTI FIR Mode for Max/Min Windows([0]: wide [1]: med [2] small [3] little).	
	CTIFIR_EN	0	CTI FIR Enable.	
9Ch	**REG9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PIPDBGHST[1:0]	5:4	Motion factor pipeline control.	
	PIPCHKHST[3:0]	3:0	Motion history pipeline control.	
9Eh	**REG9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	3DBLUR_GAIN[4:0]	4:0	3D blur gain (1~1/16).	
A0h	**REGA0**	**7:0**	**Default : 0x07**	**Access : R/W**
	DBG_2DCOMB_YCETP_SEL[1:0]	7:6	Selection of (entropyh/eh4/eh2) / (entropyv/ev2/ev1) / (entropyv-h/sw_gain/cdet_swgain). With d[5:4] = 2'd1/2'd2/2'd3.	
	DBG_2DCOMB_ENTROPY[1:0]	5:4	00: Normal. 01: EntropyH. 10: EntropyV. 11: EntropyV-entropyH.	
	AUTOSTOPSYNC	3	Automatic stop H/V sync when no input.	

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	LNFREEMD[2:0]	2:0	Line buffer free run mode. 0: Off(always synchronize). 1: 909 return. 2: 910 return. 3: 917 return. 4: 1127 return. 5: 1135 return. 6: Decided by register. 7: Automatic.	
A4h	**REGA4**	**7:0**	**Default : 0x8E**	**Access : R/W**
	HRETPOS_LOW[7:0]	7:0	Horizontal return position in line buffer free run mode(7:0).	
A6h	**REGA6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	HRETPOS_HIGH[2:0]	2:0	Horizontal return position in line buffer free run mode(10:8).	
A8h	**REGA8**	**7:0**	**Default : 0x02**	**Access : R/W**
	TILTTLRN[7:0]	7:0	Line position tilt tolerance.	
AAh	**REGAA**	**7:0**	**Default : 0x04**	**Access : R/W**
	JITTLRN3D[7:0]	7:0	3D timing detection tolerance.	
ACh	**REGAC**	**7:0**	**Default : 0x40**	**Access : R/W**
	LCKSTEP[7:0]	7:0	3D lock counter go back distance when sync unstable.	
AEh	**REGAE**	**7:0**	**Default : 0x68**	**Access : R/W**
	LCK3DTHU[7:0]	7:0	3D timing detection threshold.	
B0h	**REGB0**	**7:0**	**Default : 0x40**	**Access : R/W**
	LCK3DTHL[7:0]	7:0	3D timing detection threshold.	
B2h	**REGB2**	**7:0**	**Default : 0x08**	**Access : R/W**
	JITTLRN1[7:0]	7:0	Tolerance of h-sync jitter.	
B4h	**REGB4**	**7:0**	**Default : 0x20**	**Access : R/W**
	JITTLRN2[7:0]	7:0	Tolerance of h-sync jitter.	
B6h	**REGB6**	**7:0**	**Default : 0x10**	**Access : R/W**
	HSLCKTHU[7:0]	7:0	Upper bound threshold of hysteresis h-sync lock counter.	
B8h	**REGB8**	**7:0**	**Default : 0x08**	**Access : R/W**
	HSLCKTHL[7:0]	7:0	Lower bound threshold of hysteresis h-sync lock counter.	
BCh	**REGBC**	**7:0**	**Default : 0x14**	**Access : R/W**
	SYNCDLY[7:0]	7:0	H sync(from decoder to scaler) pipe delay.	
BEh	**REGBE**	**7:0**	**Default : 0x80**	**Access : R/W**

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	HSLDCNTMD[1:0]	7:6	H-sync lead counter mode.	
	CNTSTEPMD[1:0]	5:4	Counter step mode.	
	-	3:0	Reserved.	
C0h	**REGC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	IFMODE[1:0]	7:6	IF compenstaion mode.	
	IFCOEF[5:0]	5:0	IF compenstaion coefficient, 2-bit integer, 4-bit frac.	
D8h	**REGD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_MODE	7	ACC mode selection.	
	-	6:4	Reserved.	
	CBINV	3	Cb inverse for s-video.	
	CRINV	2	Cr inverse for s-video.	
	-	1:0	Reserved.	
E0h	**REGE0**	**7:0**	**Default : 0xF0**	**Access : R/W**
	-	7:6	Reserved.	
	CGMODE[1:0]	5:4	Auto chroma gain mode. 00: Off. 01: Auto. 10: Manu. 11: MCU control.	
	BRSTFRAFEC	3	Burst height from AFEC.	
	-	2	Reserved.	
	DBG_GAIN_SEL[1:0]	1:0	Debug gain selection.	
E2h	**REGE2**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SAWCMPDETEN	7	SAW compensation detection enable.	
	-	6:0	Reserved.	
E4h	**REGE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	BSTHGHT[7:0]	7:0	Burst height for auto chroma gain, 0: auto, 112 for NTSC and 117 for PAL; other: use RegBSTHGHT/DetBSTHGHT as C gain.	
E6h	**REGE6**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTST[7:0]	7:0	Contrast adjustment coefficient.	
E8h	**REGE8**	**7:0**	**Default : 0x80**	**Access : R/W**
	BRHT[7:0]	7:0	Brightness adjustment coefficient.	
EAh	**REGEA**	**7:0**	**Default : 0x80**	**Access : R/W**
	SAT[7:0]	7:0	SATuration adjustment coefficient.	

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F0h	**REGF0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CRMAGAIN_LOW[7:0]	7:0	Chroma gain value for manual chroma gain(7:0).	
F2h	**REGF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CRMAGAIN_HIGH[5:0]	5:0	Chroma gain value for manual chroma gain(13:8).	
FAh	**REGFA**	**7:0**	**Default : 0x80**	**Access : R/W**
	SNOWDELAY[7:0]	7:0	Latency of snow output after signal missing.	
FCh	**REGFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_CRMAGAIN_INC[2:0]	7:5	Chroma gain step of ACC.	
	ACCUPONLY	4	ACC up only.	
	ACCDELAY[3:0]	3:0	ACC latency.	
FEh	**REGFE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ACCMAXGAIN[7:0]	7:0	ACC maximum gain.	
00h	**REG00**	**7:0**	**Default : 0xC8**	**Access : R/W**
	YGAIN[7:0]	7:0	Luma gain for U/V demodulation.	
02h	**REG02**	**7:0**	**Default : 0x96**	**Access : R/W**
	CBGAIN[7:0]	7:0	Cb gain for U/V demodulation.	
04h	**REG04**	**7:0**	**Default : 0x6A**	**Access : R/W**
	CRGAIN[7:0]	7:0	Cr gain for U/V demodulation.	
06h	**REG06**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	CTIMODE[1:0]	5:4	CTI mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
	-	3:2	Reserved.	
	CBCRLPMD[1:0]	1:0	Cb/Cr low pass mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
08h	**REG08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CTSTDITHEN	6	Dithering when contrast adjustment.	

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	CTSTDITHPOS[1:0]	5:4	Dithering position(offset) of contrast.	
	-	3	Reserved.	
	SATDITHEN	2	Dithering when saturation adjustment.	
	SATDITHPOS[1:0]	1:0	Dithering position(offset) of saturation.	
0Ah	**REG0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDEMDITHEN	6	Dithering when demodulation Y-gain.	
	YDEMDITHPOS[1:0]	5:4	Dithering position(offset) of Y gain.	
	-	3	Reserved.	
	CDEMDITHEN	2	Dithering when demodulation C-gain.	
	CDEMDITHPOS[1:0]	1:0	Dithering position(offset) of C gain.	
0Ch	**REG0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETPV_COR[3:0]	7:4	Entropy V coring.	
	ETPH_COR[3:0]	3:0	Entropy H coring.	
0Eh	**REG0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETPV1_COR[3:0]	7:4	Entropy V1 coring.	
	ETPH2_COR[3:0]	3:0	Entropy H2 coring.	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMPRTBASEH[7:0]	7:0	End address of DRAM request.(H).	
12h	**REG12**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMPRTBASEM[7:0]	7:0	End address of DRAM request.(M).	
1Ah	**REG1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBCTRL[7:0]	7:0	Some control signals for FPGA.	
1Ch	**REG1C**	**7:0**	**Default : 0xE0**	**Access : R/W**
	FPGACTRL[7:0]	7:0	Some control signals for FPGA.	
1Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h	**REG20**	**7:0**	**Default : 0x13**	**Access : R/W**
	-	7:4	Reserved.	
	YDETV_PATCH_EN	3	YDET Patch V Enable.	
	MBS_V_HDIFF_EN	2	Jeff H MBS-C Enable([0]: {1,0,2,0,1} [1]: {2,0,0,0,-2}).	
	MIN_YDETH_EN	1	Minimum YDETH Mode Enable ([0]: Normal [1]: min(2tap,3tap)).	
	NEW_YDET_EN	0	CVBS Lowpass YDET Enable.	

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22h	**REG22**	**7:0**	**Default : 0x12**	**Access : R/W**
	YDIFFV1_LUMA_ENG_GAIN[1:0]	7:6	YDET V Luma Gain(div 1/2/4/8).	
	YDIFFV1_CRMA_ENG_GAIN[1:0]	5:4	YDET V Chroma Gain(div 1/2/4/8).	
	YDIFFH2_LUMA_ENG_GAIN[1:0]	3:2	YDET H Luma Gain(div 1/2/4/8).	
	YDIFFH2_CRMA_ENG_GAIN[1:0]	1:0	YDET H Chroma Gain(div 1/2/4/8).	
24h	**REG24**	**7:0**	**Default : 0x51**	**Access : R/W**
	DET_FILTER_MD_H_B[1:0]	7:6	PAL H DET Filter Mode B([00]:lpf[1,2,-1] [11]:bpf[1,-1]).	
	-	5	Reserved.	
	PAL_MBS_TAP_MD_H_B	4	PAL H Multiburst Tap B([0]:2tap [1]:3tap) Note: If we set [0], det_filter_md MUST set [11]).	
	-	3	Reserved.	
	DET_FILTER_MD_H_A[1:0]	2:1	PAL H DET Filter Mode A([00]:lpf[1,2,-1] [11]:bpf[1,-1]).	
	PAL_MBS_TAP_MD_H_A	0	PAL H Multiburst Tap A([0]:2tap [1]:3tap) Note: If we set [0], det_filter_md MUST set [11]).	
26h	**REG26**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DET_FILTER_MD_V[1:0]	2:1	PAL V DET Filter Mode([0]: 2tap mode: {2,0,-2}/{0,2,-2} [1]: 3tap mode: {1,1,-2}/{0,2,-2}).	
	PAL_MBS_TAP_MD_V	0	PAL V Multiburst Tap([0]:2tap [1]:3tap).	
28h	**REG28**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB_GAIN_H[3:0]	7:4	YDET Patch H Multiburst Gain (multiply 1~16).	
	C_GAIN_H[1:0]	3:2	YDET Patch H Chroma Gain (divide 2,4,8,16).	
	ENG_SCALE[1:0]	1:0	YDET Patch Multiburst-Chroma Energy Scale(multiply 4/8/16/32).	
2Ah	**REG2A**	**7:0**	**Default : 0xCC**	**Access : R/W**
	CDET_V_LUMA_ENG_GAIN[1:0]	7:6	CDET V Luma Gain(multiply 1/2/4/8).	
	CDET_V_CRMA_ENG_GAIN[1:0]	5:4	CDET V Chroma Gain(multiply 1/2/4/8).	
	CDET_H_LUMA_ENG_GAIN[1:0]	3:2	CDET H Luma Gain(multiply 1/2/4/8).	
	CDET_H_CRMA_ENG_GAIN[1:0]	1:0	CDET H Chroma Gain(multiply 1/2/4/8).	
2Ch	**REG2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CDET_SWITCH_THR[7:0]	7:0	CDET Switch threshold.	
2Eh	**REG2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CDET_SWITCH_STEP[1:0]	7:6	CDET Switch Step (multiply 1/2/4/8).	
	-	5:0	Reserved.	

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30h	**REG30**	**7:0**	**Default : 0x2A**	**Access : R/W**
	PAL_2DCNCH_MD[1:0]	7:6	PAL Chroma 2D 9x5 Mode ([00]:V{12221} [01]:{14641} [1x] 01210).	
	PAL_DIFFV2_SEL	5	CVDiff V2 Select for PAL([0]: Blend(max2, DiffUD) [1]: max(max2, DiffUD)).	
	LPF_FACTOR[4:0]	4:0	CVBS Lowpass Blending Factor.	
32h	**REG32**	**7:0**	**Default : 0x01**	**Access : R/W**
	CVH2PATCH_EN	7	SC's Diagonal Patch Enable(NTSC443 Only).	
	CVDIFF_H2_GAIN[2:0]	6:4	SC's Diagonal Patch Gain (multiply 1/0.5/0.25/0.125//0.0625/0.03125/2/4).	
	PAL_DIFFV1_SEL	3	PAL cvdiff v1 select [0]: Ian v1 [1]: Jeff v1.	
	PAL_CVDIFF_V2_GAIN[2:0]	2:0	CVDiff V2 Gain for PAL (multiply 0/1/2/4/8/0.5/0.25/0.125).	
34h	**REG34**	**7:0**	**Default : 0x03**	**Access : R/W**
	AMPV1_GAIN[3:0]	7:4	AMP_YDIFF_V1 Gain (divide 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).	
	AMPH2_GAIN[3:0]	3:0	AMP_YDIFF_H2 Gain (divide 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).	
36h	**REG36**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CHROMA_ADPBLD_SEL	4	Chroma Fix Select for AdaptiveCrma Blending ([0]: Original [1]: 12221Fix).	
	YDETHBND_TH[2:0]	3:1	YDET H Bound TH by Reg.	
	YDETHBND_EN	0	YDET H Bound Enable by Reg.	
38h	**REG38**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7	Reserved.	
	V5DBG_EN	6	Entropy V5 Debug Mode Enable (Use V2).	
	V5FLT_SEL	5	Entropy V5 Filter Select ([0]: Max [1]: LP12221).	
	PALETPV_SEL	4	PAL Entropy V Select ([0]: Original [1]: Entropy V5).	
	ETP_H2GAIN[1:0]	3:2	Entropy H2 Gain (mul 1/2/4/8).	
	PALV1_EN	1	Disable PAL V1 Calculation in PAL(for pal use only).	
	H2V1_EN	0	H2 v1 Enable ([0]: set y21_gain 0 [1]: default).	
3Ah	**REG3A**	**7:0**	**Default : 0x08**	**Access : R/W**
	EV2_PROCFLT_SEL[1:0]	7:6	Entropy V2 Proc Filter Select([00]: Original [01]: lp121(NTSConly) [10]: m_MaxMin [11]: lp12221 m_cvdiffv2).	

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Index	**Mnemonic**	**Bit**	**Description**	
	-	5	Reserved.	
	EH4_PROCFLT_SEL	4	Entropy H4 Proc Filter Select ([0]: Original [1]: LP{12221}).	
	EV1_POSTFLT_SEL	3	Entropy V1 Post Filter Select ([0]: Original [1]: lp121).	
	EV1_PROCFLT_SEL	2	Entropy V1 Proc Filter Select ([0]: Original [1]: minmax).	
	EH2_POSTFLT_SEL	1	Entropy H2 Post Filter Select ([0]: Max [1]: Lp12221).	
	EH2_PROCFLT_SEL	0	Entropy H2 Proc Filter Select ([0]: Original [1]: minmax).	
3Ch	**REG3C**	**7:0**	**Default : 0xC1**	**Access : R/W**
	IAN_MAXEH4_GAIN[1:0]	7:6	T-Cross Patch H4 gain (1/2/4/8).	
	IAN_MAXEH2_GAIN[1:0]	5:4	T-Cross Patch H2 gain (1/2/4/8).	
	-	3:1	Reserved.	
	IAN_EV_EN	0	T-Cross Patch V Enable.	
3Eh	**REG3E**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	SAWBLENDDIV[4:0]	4:0	SAW blend division.	
40h	**REG40**	**7:0**	**Default : 0x48**	**Access : R/W**
	ADP9X5_CSWEN	7	Adaptive 9X5 use CDET switch gain enable.	
	ADPGAIN_SCUP_EN	6	Adaptive 9x5 Scale Up Enable.	
	REFER_3X3LRDIFF_EN	5	Adaptive 9x5 Reference Adaptive 3x3 Difference Enable(for LR Diff).	
	REFER_H4_EN	4	Adaptive 3x3 Reference Adaptive 9x5 Difference Enable(for LR Diff).	
	ADPCRMA_SEL	3	Adaptive Chroma Select ([0]: 14641 [1]: 12221).	
	ADPLUMA_SEL	2	Adaptive Luma Select ([0]: 14641 [1]: 12221).	
	ADP2DSEL[1:0]	1:0	Adaptive Mode (9x5 / 9x3 / 3x5 / 3x3).	
42h	**REG42**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINLR1P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.	
	ADPGAINLR0P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
44h	**REG44**	**7:0**	**Default : 0x21**	**Access : R/W**
	ADPGAINLR3P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.	
	ADPGAINLR2P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
46h	**REG46**	**7:0**	**Default : 0x84**	**Access : R/W**
	ADPGAINLR5P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.	
	ADPGAINLR4P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
48h	**REG48**	**7:0**	**Default : 0xEC**	**Access : R/W**

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	ADPGAINLR7P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.	
	ADPGAINLR6P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
4Ah	**REG4A**	**7:0**	**Default : 0x0F**	**Access : R/W**
	ADPGAINLR9P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.	
	ADPGAINLR8P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
4Ch	**REG4C**	**7:0**	**Default : 0x60**	**Access : R/W**
	-	7	Reserved.	
	ADPGAINLR8TOAP[2:0]	6:4	Adp3x3 Lookup Gain LR Table (Sign Bit), 8~Ap[4].	
	ADPGAINLRAP[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
4Eh	**REG4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINLR0TO7P[7:0]	7:0	Adp3x3 Lookup Gain LR Table (Sign Bit), 0~7p[4].	
50h	**REG50**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINUD1P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD0P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
52h	**REG52**	**7:0**	**Default : 0x21**	**Access : R/W**
	ADPGAINUD3P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD2P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
54h	**REG54**	**7:0**	**Default : 0x84**	**Access : R/W**
	ADPGAINUD5P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD4P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
56h	**REG56**	**7:0**	**Default : 0xEC**	**Access : R/W**
	ADPGAINUD7P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD6P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
58h	**REG58**	**7:0**	**Default : 0x0F**	**Access : R/W**
	ADPGAINUD9P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD8P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
5Ah	**REG5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	ADPGAINUD8TOAP[2:0]	6:4	Adp3x3 Lookup Gain UD Table (Sign Bit), 8~Ap[4].	
	ADPGAINUDAP[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
5Ch	**REG5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINUD0TO7P[7:0]	7:0	Adp3x3 Lookup Gain UD Table (Sign Bit), 0~7p[4].	
5Eh	**REG5E**	**7:0**	**Default : 0x20**	**Access : R/W**
	LP2DYREF[7:0]	7:0	Reference for adaptive luma low pass filter.	

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60h	**REG60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5_CREGION_SEL[1:0]	5:4	Adaptive9x5 chroma region select.	
	-	3	Reserved.	
	ADP9X5_DBGSEL[2:0]	2:0	Adaptive 9x5 Debug Output Select.	
62h	**REG62**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN0[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
64h	**REG64**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN1[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
66h	**REG66**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN2[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
68h	**REG68**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN3[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
6Ah	**REG6A**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN4[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
6Ch	**REG6C**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN5[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
6Eh	**REG6E**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN6[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
70h	**REG70**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN7[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
72h	**REG72**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN8[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
74h	**REG74**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	

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	ADP9X5GAIN9[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
76h	**REG76**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAINA[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
78h	**REG78**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	FP_HOR_PIPE[1:0]	5:4	Final Patch Horizontal version pipe selection.	
	-	3:1	Reserved.	
	FP_HOR_EN	0	Enable Final Patch Horizontal version.	
7Ah	**REG7A**	**7:0**	**Default : 0x50**	**Access : R/W**
	IAN_TH_HOR[7:0]	7:0	Ian PureLuma TH_Ver (25) : U/D Diff Threshold for Detection.	
7Ch	**REG7C**	**7:0**	**Default : 0x50**	**Access : R/W**
	IAN_DIFF_SHIFTR[1:0]	7:6	Ian PureLuma R Diff Shift(div 1/2/4/8) before TH.	
	IAN_DIFF_SHIFTL[1:0]	5:4	Ian PureLuma L Diff Shift(div 1/2/4/8) before TH.	
	IAN_DIFF_MSHTR[1:0]	3:2	Ian PureLuma R Diff Shift(div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_MSHTL[1:0]	1:0	Ian PureLuma L Diff Shift(div 4/8/16/32) after TH (8~=32 inC).	
7Eh	**REG7E**	**7:0**	**Default : 0x04**	**Access : R/W**
	LP2DYTH[7:0]	7:0	Threshold for adaptive luma low pass filter.	
80h	**REG80**	**7:0**	**Default : 0xA0**	**Access : R/W**
	CRMA2D_SEL[1:0]	7:6	Chroma 2D Select (5x5/5x5/adaptive/DEMbld).	
	LUMA2D_SEL[1:0]	5:4	Luma 2D Select (5x5/5x5/adaptive/adaptive).	
	CRMAOUT_MODE[1:0]	3:2	Chroma Output Mode ([00]: Normal [01]: 1DH [10]: 1DV [11]: 2D).	
	LUMAOUT_MODE[1:0]	1:0	Luma Output Mode ([00]: Normal [01]: 1DH [10]: 1DV [11]: 2D).	
82h	**REG82**	**7:0**	**Default : 0x33**	**Access : R/W**
	YETPV_GAIN[3:0]	7:4	Luma Entropy Gain V for Lookup Table (mul (1~16)/4).	
	YETPH_GAIN[3:0]	3:0	Luma Entropy Gain H for Lookup Table (mul (1~16)/4).	
84h	**REG84**	**7:0**	**Default : 0x33**	**Access : R/W**
	CETPV_GAIN[3:0]	7:4	Chroma Entropy Gain V for Lookup Table (mul (1~16)/4).	
	CETPH_GAIN[3:0]	3:0	Chroma Entropy Gain H for Lookup Table (mul (1~16)/4).	
86h	**REG86**	**7:0**	**Default : 0x1F**	**Access : R/W**

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Index	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	AUTO2D_EN	4	When it is unknown TV System, force 2D Output Enable.	
	CETP_SCDN_EN	3	Chroma Entropy Scaled Down Enable.	
	CETP_SCUP_EN	2	Chroma Entropy Scaled Up Enable.	
	YETP_SCDN_EN	1	Luma Entropy Scaled Down Enable.	
	YETP_SCUP_EN	0	Luma Entropy Scaled Up Enable.	
88h	**REG88**	**7:0**	**Default : 0x00**	**Access : R/W**
	YBLD_FORCE_SW_GAIN[3:0]	7:4	Luma Blending Forced Switch Gain(0~128).	
	-	3:1	Reserved.	
	YBLD_FORCE_SW	0	Luma Blending Forced Switch Enable.	
8Ah	**REG8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RSD_DIFF_STEP[2:0]	6:4	Rsd difference step.	
	RSD_DIFF_THR[3:0]	3:0	Rsd difference threshold.	
8Ch	**REG8C**	**7:0**	**Default : 0x20**	**Access : R/W**
	YGAINYH1P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAINYH0P[3:0]	3:0	Luma Lookup Gain Table YH.	
8Eh	**REG8E**	**7:0**	**Default : 0x85**	**Access : R/W**
	YGAINYH3P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAINYH2P[3:0]	3:0	Luma Lookup Gain Table YH.	
90h	**REG90**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYH5P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAINYH4P[3:0]	3:0	Luma Lookup Gain Table YH.	
92h	**REG92**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYH7P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAINYH6P[3:0]	3:0	Luma Lookup Gain Table YH.	
94h	**REG94**	**7:0**	**Default : 0x20**	**Access : R/W**
	YGAINYV1P[3:0]	7:4	Luma Lookup Gain Table YV.	
	YGAINYV0P[3:0]	3:0	Luma Lookup Gain Table YV.	
96h	**REG96**	**7:0**	**Default : 0x85**	**Access : R/W**
	YGAINYV3P[3:0]	7:4	Luma Lookup Gain Table YV.	
	YGAINYV2P[3:0]	3:0	Luma Lookup Gain Table YV.	
98h	**REG98**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYV5P[3:0]	7:4	Luma Lookup Gain Table YV.	

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	YGAINYV4P[3:0]	3:0	Luma Lookup Gain Table YV.	
9Ah	**REG9A**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYV7P[3:0]	7:4	Luma Lookup Gain Table YV.	
	YGAINYV6P[3:0]	3:0	Luma Lookup Gain Table YV.	
9Ch	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
9Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
A0h	**REGA0**	**7:0**	**Default : 0xB9**	**Access : R/W**
	PEAKING_PALCMP_INV	7	Peaking palcmp inverse.	
	IAN_ENH_CLIP[2:0]	6:4	Clipping TH (0/16/32/64/96/128/160/192).	
	IAN_ENH_CORING[1:0]	3:2	Coring TH (0/4/8/16).	
	NTSC_PEAKING_SEL	1	Ntsc peaking method select ([0]: Ian Mode [1]: X Mode).	
	IAN_ENH_PEAKING_EN	0	Ian Enhanced Peaking Enable.	
A2h	**REGA2**	**7:0**	**Default : 0x40**	**Access : R/W**
	IAN_ENH_Y1GAIN[7:0]	7:0	Y1 gain (div(16~128) >>3).	
A4h	**REGA4**	**7:0**	**Default : 0x40**	**Access : R/W**
	IAN_ENH_Y2GAIN[7:0]	7:0	Y2 gain (div(16~128) >>3).	
A6h	**REGA6**	**7:0**	**Default : 0x60**	**Access : R/W**
	IAN_ENH_Y3GAIN[7:0]	7:0	Y3 gain (div(16~128) >>3).	
A8h	**REGA8**	**7:0**	**Default : 0x20**	**Access : R/W**
	IAN_MIN_CDIFFH[7:0]	7:0	Peaking minimum C Difference Horizontal.	
AAh	**REGAA**	**7:0**	**Default : 0x08**	**Access : R/W**
	IAN_MIN_CDIFFV[7:0]	7:0	Peaking minimum C Difference Vertical.	
ACh	**REGAC**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	IAN_CDIFFV_RANGE[1:0]	3:2	Peaking C Difference Vertical Range (16/32/64/128).	
	IAN_CDIFFH_RANGE[1:0]	1:0	Peaking C Difference Horizontal Range (16/32/64/128).	
AEh	**REGAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	YETP2D_VGAIN[3:0]	7:4	Y ETP2D VGain (V->2D).	
	YETP2D_HGAIN[3:0]	3:0	Y ETP2D HGain (H->2D).	
B0h	**REGB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	CETP2D_VGAIN[3:0]	7:4	C ETP2D VGain (V->2D).	
	CETP2D_HGAIN[3:0]	3:0	C ETP2D HGain (H->2D).	

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B4h	**REGB4**	**7:0**	**Default : 0x01**	**Access : R/W**
	DBG_FP_MD[3:0]	7:4	Final Patch Debug Mode([3]: Debug Enable(1) [2:1]: VDiff(0)/HDiff(1)/Gain(2) [0]: Up(0)/Down(1)).	
	-	3:1	Reserved.	
	FINALPATCH_EN	0	Ian Final Patch Enable.	
B6h	**REGB6**	**7:0**	**Default : 0x42**	**Access : R/W**
	-	7	Reserved.	
	IAN_PLHDIFF_SC[2:0]	6:4	Ian PureLuma H-Diff Scale Select (mul 0/0.125/0.25/0.5/1/2/4/8).	
	-	3	Reserved.	
	IAN_PLHDIFF_TH[2:0]	2:0	Ian PureLuma H-Diff Threshold Select(32/64/128/256).	
B8h	**REGB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IAN_DIFF_SHIFTD[1:0]	7:6	Ian PureLuma D Diff Shift(div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_SHIFTU[1:0]	5:4	Ian PureLuma U Diff Shift(div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_MSHTD[1:0]	3:2	Ian PureLuma D Diff Shift(div 1/2/4/8) before TH.	
	IAN_DIFF_MSHTU[1:0]	1:0	Ian PureLuma U Diff Shift(div 1/2/4/8) before TH.	
BAh	**REGBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	IAN_TH_VER[7:0]	7:0	Ian PureLuma TH_Ver (25) : U/D Diff Threshold for Detection.	
BCh	**REGBC**	**7:0**	**Default : 0x05**	**Access : R/W**
	PLHDIFF_TH[7:0]	7:0	Pure Luma H difference threshold.	
BEh	**REGBE**	**7:0**	**Default : 0x33**	**Access : R/W**
	CETP2D_MD[1:0]	7:6	C ETP2D mode([0]: Area2D [1]: RegSet [2]: Area2D+RegSet [3] : max(Are2D, RegSet).	
	CETP2D_STR[1:0]	5:4	C ETP2D strength([0]: 25% [1]: 50% [2]: 75% [3]: 100%).	
	YETP2D_MD[1:0]	3:2	Y ETP2D mode([0]: Area2D [1]: RegSet [2]: Area2D+RegSet [3] : max(Are2D, RegSet).	
	YETP2D_STR[1:0]	1:0	Y ETP2D strength([0]: 25% [1]: 50% [2]: 75% [3]: 100%).	
C0h	**REGC0**	**7:0**	**Default : 0x00**	**Access : RO**
	HSLOCK	7	HSync lock happen.	
	LOCK3D	6	Good timing happen.	
	MEMRDBWEVN	5	Memory Rd Bandwidth Evn.	
	MEMWRBWEVN	4	Memory Wr Bandwidth Evn.	

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	NOTHSLOCK	3	HSync unlock happen.	
	NOTLOCK3D	2	Good timing disappear.	
	HSCHG	1	H-Sync counter change.	
	MEMBWEVN	0	DRAM bandwidth not enough.	
C2h	**REGC2**	**7:0**	**Default : 0x00**	**Access : RO**
	STLIMG	7	Still image happen.	
	NOTSTLIMG	6	Still image disappear.	
	CCHNLACT	5	C-chanel active(maybe S-video input).	
	NOTCCHNLACT	4	C-chanel quiet(maybe CVBS input).	
	-	3	Reserved.	
	FLDCNTCHG	2	Field counter change.	
	-	1:0	Reserved.	
C4h	**REGC4**	**7:0**	**Default : 0x00**	**Access : RO**
	LN525	7	525 line system.	
	LN625	6	625 line system.	
	F358	5	3.58 MHz system.	
	F443	4	4.43 MHz system.	
	NOINPUT	3	No input.	
	VDOMD[2:0]	2:0	Video mode. 0: NTSC_M. 1: NTSC_443. 2: PAL_M. 3: PAL_BDGHIN. 4: PAL_Nc. 5: PAL_60. 6: Input without burst. 7: Unknown.	
C6h	**REGC6**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	INTERLACE	0	INTERLACE input.	
C8h	**REGC8**	**7:0**	**Default : 0x00**	**Access : RO**
	DETBLANK[7:0]	7:0	Detected blank level.	
CAh	**REGCA**	**7:0**	**Default : 0x00**	**Access : RO**
	CURBLANK[7:0]	7:0	Current used blank level.	
CCh	**REGCC**	**7:0**	**Default : 0x00**	**Access : RO**

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COMB Register (Bank = 1036)				
Index	**Mnemonic**	**Bit**	**Description**	
	SYNCLVL[7:0]	7:0	Detected sync level.	
CEh	**REGCE**	**7:0**	**Default : 0x00**	**Access : RO**
	SYNCHGHT[7:0]	7:0	Detected sync height.	
D0h	**REGD0**	**7:0**	**Default : 0x00**	**Access : RO**
	BURSTHGHT[7:0]	7:0	Detected burst height.	
D2h	**REGD2**	**7:0**	**Default : 0x00**	**Access : RO**
	DETHORTOTAL_LOW[7:0]	7:0	Detected horizontal total(7:0).	
D4h	**REGD4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	DETHORTOTAL_HIGH[2:0]	2:0	Detected horizontal total(10:8).	
D6h	**REGD6**	**7:0**	**Default : 0x00**	**Access : RO**
	RPTCOVFH[7:0]	7:0	Reported chroma overflow count per line.	
D8h	**REGD8**	**7:0**	**Default : 0x00**	**Access : RO**
	RPTCOVFV[7:0]	7:0	Reported chroma overflow count per field.	
DAh	**REGDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MOT_DIFF_MIN_SEL	7	3D motion diff min filter selection.	
	-	6:4	Reserved.	
	MOTDIFF_COR[3:0]	3:0	3D motion diff coring.	
E0h	**REGE0**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	DYNETPEXT	5	Extend the Etp3D rang 1pixel by max filter.	
	DYNETPAVG	4	Average 3DY entropy and 2D entropy.	
	-	3:0	Reserved.	
E2h	**REGE2**	**7:0**	**Default : 0xA0**	**Access : R/W**
	SMVBYEN	7	Small vibration algorithm enable.	
	-	6	Reserved.	
	SMVBYNOMMD[1:0]	5:4	Small vibration normalize value (16/32/64/128).	
	-	3:0	Reserved.	
E4h	**REGE4**	**7:0**	**Default : 0x47**	**Access : R/W**
	SMVBYETP3DTH[7:0]	7:0	Small vibration entropy 3D blend threshold.	
E6h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
E8h	**REGE8**	**7:0**	**Default : 0x17**	**Access : R/W**
	SMVBYCOR[3:0]	7:4	Small vibration motion difference corring.	

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COMB Register (Bank = 1036)				
Index	**Mnemonic**	**Bit**	**Description**	
	SMVBYBLENDWT[3:0]	3:0	Small vibration motion blend weight of origianl motion difference.	
FEh	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

VBI Register (Bank = 1037)

VBI Register (Bank = 1037)				
Index	**Mnemonic**	**Bit**	**Description**	
20h	**REG20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TTEN	0	Teletext enable bit 0: disable ; 1: enable.	
22h	**REG22**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMASRC_ADR_7_0[7:0]	7:0	DMA source linear address (lower 8 bits).	
24h	**REG24**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMASRC_ADR_15_8[7:0]	7:0	DMA source linear address (middle 8 bits).	
26h	**REG26**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMASRC_ADR_23_16[7:0]	7:0	DMA source linear address (upper 8 bits).	
28h	**REG28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMADES_ADR_7_0[7:0]	7:0	DMA destination linear address (lower 8 bits).	
2Ah	**REG2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMADES_ADR_15_8[7:0]	7:0	DMA destination linear address (middler 8 bits).	
2Ch	**REG2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMADES_ADR_23_16[7:0]	7:0	DMA destination linear address (upper 8 bits).	
2Eh	**REG2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAQW_CNT_7_0[7:0]	7:0	DMA block move count (unit: 8 bytes ; lower 8 bits).	
30h	**REG30**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAQW_CNT_15_8[7:0]	7:0	DMA block move count (unit: 8 bytes ; upper 8 bits).	
32h	**REG32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMA_FUNC[4:0]	4:0	DMA function.	
34h	**REG34**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:2	Reserved.	
	DMA_READY	1	DMA ready status.	

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Index	Mnemonic	Bit	Description	
	DMA_FIRE	0	DMA engine fire signal.	
36h	**REG36**	**7:0**	**Default : 0x20**	**Access : R/W**
	DMAERASE_DATA[7:0]	7:0	DMA erase data.	
38h	**REG38**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TAG_INT_EN	2	Tag interrupt enable.	
	DMA_INT_EN	1	DMA interrupt enable.	
	VBI_INT_EN	0	VBI interrupt enable.	
3Ch	**REG3C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMA_WBE_PRE[3:0]	7:4	DMA previous write byte enable.	
	DMA_WBE_POST[3:0]	3:0	DMA post write byte enable.	
3Eh	**REG3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DC_RAW	3	Designation code raw data mode.	
	VBI_HEADER_RAW	2	VBI header raw data mode.	
	VBI_ALL_RAW	1	VBI data raw data mode.	
	SRH_ENG_CLEAR	0	Tag search engine clear.	
40h	**REG40**	**7:0**	**Default : 0x00**	**Access : RO**
	VBIREADY	7	VBI line end and teletext slicer ready indication.	
	-	6:5	Reserved.	
	VBI_LINE_CNT[4:0]	4:0	VBI line counter.	
42h	**REG42**	**7:0**	**Default : 0x00**	**Access : RO**
	TTSLICERRDY_A	7	Teletext slicer ready indication.	
	VBI_FIELD_CNT_6_0[6:0]	6:0	VBI field counter.	
44h	**REG44**	**7:0**	**Default : 0x00**	**Access : R/W**
	BURST_RE_MD	7	Burst read mode enable.	
	BURST_WE_MD	6	Burst write mode enable.	
	MCU_ADR_PORT[5:0]	5:0	MCU memory access address port.	
46h	**REG46**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU_DATA_PORT[7:0]	7:0	MCU memory access data port.	
48h	**REG48**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAGRW_POS_7_0[7:0]	7:0	Tag read/write position (lower 8 bits).	
4Ah	**REG4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAG_PT_DELTA32[3:0]	7:4	Tag length 32 delta.	

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Index	Mnemonic	Bit	Description	
	TAGRW_POS_11_8[3:0]	3:0	Tag read/write position (upper 4 bits).	
4Ch	**REG4C**	**7:0**	**Default : 0x00**	**Access : RO**
	PAGEBUF_ADDR_7_0[7:0]	7:0	Page buffer linear address (lower 8 bits).	
4Eh	**REG4E**	**7:0**	**Default : 0x00**	**Access : RO**
	PAGEBUF_ADDR_15_8[7:0]	7:0	Page buffer linear address (middle 8 bits).	
50h	**REG50**	**7:0**	**Default : 0x00**	**Access : RO**
	PAGEBUF_ADDR_23_16[7:0]	7:0	Page buffer linear address (upper 8 bits).	
52h	**REG52**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAGEBUF_CNT_7_0[7:0]	7:0	Pager buffer counter (lower 8 bits).	
54h	**REG54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PAGEBUF_CNT_11_8[3:0]	3:0	Pager buffer counter (upper 4 bits).	
56h	**REG56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FW_SEARCH_SEL	3	MCU memory access data switch to FW search result data.	
	CYC_DISABLE	2	Disable cyclic search when touch physical size.	
	SEARCH_NOSUB	1	Search without sub-code.	
	REQ_64	0	The length of search request. 0->32 ; 1->64.	
58h	**REG58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAGAZINE[3:0]	3:0	MAGAZINE.	
5Ah	**REG5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAGE_TENS[3:0]	7:4	Page number tens.	
	PAGE_UNITS[3:0]	3:0	Page number units.	
5Ch	**REG5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CODE4[1:0]	5:4	Sub-code S4.	
	SUB_CODE3[3:0]	3:0	Sub-code S3.	
5Eh	**REG5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CODE2[2:0]	6:4	Sub-code S2.	
	SUB_CODE1[3:0]	3:0	Sub-code S1.	
60h	**REG60**	**7:0**	**Default : 0xFF**	**Access : R/W**

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Index	**Mnemonic**	**Bit**	**Description**	
	TAG_BASE_15_8[7:0]	7:0	Tag base address.	
62h	**REG62**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TAG_BASE_23_16[7:0]	7:0	Tag base address.	
64h	**REG64**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAGE_BASE_15_8[7:0]	7:0	Page base address.	
66h	**REG66**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAGE_BASE_23_16[7:0]	7:0	Page base address.	
68h	**REG68**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAGE_SIZE[7:0]	7:0	One page size.	
6Ah	**REG6A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TAG_PHY_SIZE[7:0]	7:0	Tag physical size (lower 8 bits).	
6Ch	**REG6C**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TAG_PHY_SIZE_11_8[3:0]	3:0	Tag physical size (upper 4 bits).	
6Eh	**REG6E**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:4	Reserved.	
	BUF_ADDR_RDY	3	Page buffer linear address ready.	
	HIT_STATUS	2	Search hit status.	
	TAG_READY	1	Tag ready status.	
	TAG_FIRE	0	Tag engine fire signal.	
70h	**REG70**	**7:0**	**Default : 0x00**	**Access : R/W**
	TTBASEADDR2_7_0[7:0]	7:0	Teletext base address 2 (lower 8 bits).	
72h	**REG72**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTBASEADDR2_15_8[7:0]	7:0	Teletext base address 2 (middle 8 bits).	
74h	**REG74**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTBASEADDR2_23_16[7:0]	7:0	Teletext base address 2 (upper 8 bits).	
76h	**REG76**	**7:0**	**Default : 0x12**	**Access : R/W**
	TTVBIBUFLEN_7_0[7:0]	7:0	Teletext VBI buffer length (lower 8 bits).	
78h	**REG78**	**7:0**	**Default : 0x00**	**Access : R/W**
	TTVBIBUFLEN_15_8[7:0]	7:0	Teletext VBI buffer length (upper 8 bits).	
7Ah	**REG7A**	**7:0**	**Default : 0x00**	**Access : RO**
	TTPKTCNT_A_7_0[7:0]	7:0	Teletext packet counter (lower 8 bits).	
7Ch	**REG7C**	**7:0**	**Default : 0x00**	**Access : RO**
	TTPKTCNT_A_15_8[7:0]	7:0	Teletext packet counter (upper 8 bits).	

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Index	Mnemonic	Bit	Description	
80h	**REG80**	**7:0**	**Default : 0x21**	**Access : R/W**
	CRIAMPTHDL_9_8[1:0]	7:6	Closed caption clock run-in amplitude L (upper 2 bits).	
	CCLINESTR1_4_3[1:0]	5:4	Closed caption line start 1 (upper 2 bits).	
	CRIDETENNUM_10_8[2:0]	3:1	Closed caption clock run-in detection enable number (upper 3 bits).	
	SLCTHDMODE	0	Closed caption slicer threshold mode.	
82h	**REG82**	**7:0**	**Default : 0x52**	**Access : R/W**
	CCLINESTR1_2_0[2:0]	7:5	Closed caption line start 1 (lower 3 bits).	
	CCLINEEND1[4:0]	4:0	Closed caption line end 1.	
84h	**REG84**	**7:0**	**Default : 0x1C**	**Access : R/W**
	CCINTTYPE	7	Closed caption interrupt type. 0: Assert 8T after CC line in even field if CC is found. 1: According to CcReq.	
	-	6:0	Reserved.	
86h	**REG86**	**7:0**	**Default : 0xA8**	**Access : R/W**
	CRIDETENNUM_7_0[7:0]	7:0	Closed caption clock run-un detection enable number (lower 8 bits).	
88h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
8Ah	**REG8A**	**7:0**	**Default : 0xA0**	**Access : R/W**
	CRIAMPTHDL_7_0[7:0]	7:0	Closed caption clock run-in amplitude L (lower 8 bits).	
8Ch	**REG8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CCFRAMTRIGNUM_4_0[4:0]	5:1	Closed caption frame trigger number. This controls CcFramTrig (VBI_IRQ_Status[3]). When CcFramCnt == CcFramTrigNum, CcFramTrig would be asserted.	
	CCEN	0	Closed caption enable.	
8Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
90h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
92h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
94h	**-**	**7:0**	**Default : -**	**Access : -**

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Index	Mnemonic	Bit	Description	
	-	-	Reserved.	
96h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
98h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
9Ah	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
9Ch	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
9Eh	**REG9E**	**7:0**	**Default : 0xF8**	**Access : R/W**
	CRIAMPTHDH_7_0[7:0]	7:0	Closed caption clock run-in amplitude upper threshold (lower 8 bits).	
A0h	**REGA0**	**7:0**	**Default : 0x72**	**Access : R/W**
	CRIAMPTHDH_9_8[1:0]	7:6	Closed caption clock run-in amplitude upper threshold (upper 2 bits).	
	-	5	Reserved.	
	CCLINESTR2[4:0]	4:0	Closed caption line start 2.	
A2h	**REGA2**	**7:0**	**Default : 0xB2**	**Access : R/W**
	-	7:5	Reserved.	
	CCLINEEND2[4:0]	4:0	Closed caption line end 2.	
A4h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
A6h	**REGA6**	**7:0**	**Default : 0x90**	**Access : R/W**
	CCSCWINDLEN[7:0]	7:0	Closed caption start code checking window length.	
A8h	**REGA8**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	CCSTRCODEMASK[2:0]	5:3	Closed caption start code mask. 1: Mask(ignore) ; 0: normal.	
	CCSTRCODE[2:0]	2:0	Closed caption start code.	
AAh	**REGAA**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CCBYTEERRH	1	Closed caption byte error (upper part).	
	CCBYTEERRL	0	Closed caption byte error (lower part).	
ACh	**REGAC**	**7:0**	**Default : 0x00**	**Access : RO**

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Index	Mnemonic	Bit	Description	
	CCODDFOUND	7	Closed caption odd byte found indication.	
	CCEVEFOUND	6	Closed cation even byte found indication.	
	-	5	Reserved.	
	CCFRAMCNT[4:0]	4:0	Closed caption frame counter. If there is CC data in odd or even field, this counter would increase 1 for this frame.	
AEh	**REGAE**	**7:0**	**Default : 0x00**	**Access : RO**
	CCBYTES_7_0[7:0]	7:0	Closed caption bytes (lower 8 bits).	
B0h	**REGB0**	**7:0**	**Default : 0x00**	**Access : RO**
	CCBYTES_15_8[7:0]	7:0	Closed caption bytes (upper 8 bits).	
B6h	**REGB6**	**7:0**	**Default : 0x00**	**Access : RO**
	CC_PACKET_COUNTER[7:0]	7:0	Closed caption packet counter.	
B8h	**REGB8**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	
	CCBUFLEN[6:0]	6:0	Closed caption buffer length.	
BAh	**REGBA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CCBASEADDR_23_16[7:0]	7:0	Closed caption base address (upper 8 bits).	
BCh	**REGBC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CCBASEADDR_15_8[7:0]	7:0	Closed caption base address (middle 8 bits).	
BEh	**REGBE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CCBASEADDR_7_0[7:0]	7:0	Closed caption base address (lower 8 bits).	
D2h	**REGD2**	**7:0**	**Default : 0x05**	**Access : R/W**
	TTINTPZXTH[7:0]	7:0	Teletext interpolation zero crossing threshold. When the difference of TtIntp zero crossing value is smaller than TtInptZXTh, Kp value will change to TtKpSel2nd.	
D4h	**REGD4**	**7:0**	**Default : 0x0D**	**Access : R/W**
	-	7:5	Reserved.	
	TT2KPMODE[1:0]	4:3	Teletext two Kp mode. 0,1: disable. 2: Using 2nd Kp value when the difference of TtIntp zero crossing value is smaller than TtInptZXTh each line. ; 3: using 2nd Kp value value when the difference of TtIntp zero crossing value is smaller than TtInptZXTh each field.	
	TTKPSEL2ND[2:0]	2:0	Teletext DPLL phase error gain selection 2nd parameter. 0: 2^-9; 1: 2^-10; 2: 2^-11; 3: 2^-12; 4: 2^-13; 5: 2^-14; 6: 2^-15; 7: 2^-16.	

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Index	Mnemonic	Bit	Description	
D6h	**REGD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_IRQ_FORCE[7:0]	7:0	VBI Iterrupt Request Force Bits.	
D8h	**REGD8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VBI_IRQ_MASK[7:0]	7:0	VBI Iterrupt Request Mask Bits.	
DAh	**REGDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_IRQ_CLR[7:0]	7:0	VBI Iterrupt Request Clear Bits.	
DCh	**REGDC**	**7:0**	**Default : 0x00**	**Access : RO**
	VBI_IRQ_STATUS[7:0]	7:0	VBI Iterrupt Request Status Report.	
DEh	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
E0h	**REGE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	VPSWSSEN	7	VPS / Wss enable bit. 1'b1: enable ; 1'b0: disable.	
	VPSEACHFLD	6	Vps Each Field option. 0: Only detect in odd field; 1: detect in odd and even field.	
	WSSEACHFLD	5	Wss Each Field option. 0: Only detect in odd field; 1: detect in odd and even field.	
	-	4	Reserved.	
	VBI_RST	3	VBI software reset.	
	TTINTTYPE[1:0]	2:1	Teletext interrupt type.[1]: 0: assert 8T cycle ; 1: wait ttx_intack to clear the assertion. [0]: 0: Interrupt is issued when Teletext slicer is ready afterTeletext available lines ; 1: Interrupt is issued after Teletext available lines no matter whether there is Teletext data.	
	TTFRCEN	0	Teletext forced enable bit. Teletext function could be enabled by two ways. The formal way is enabled from internal MCU and stable VD state is necessary. The other way is enabled by this bit directly.	
E2h	**REGE2**	**7:0**	**Default : 0xA0**	**Access : R/W**
	TTINICRIWINDSTRPT_7_0[7:0]	7:0	Teletext initial state clock run-in window start point (lower 7 bits).	
E4h	**REGE4**	**7:0**	**Default : 0x3C**	**Access : R/W**
	-	7:6	Reserved.	
	TTLINEUPDDEF	5	Teletext line default update enable.	

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Index	Mnemonic	Bit	Description	
	TTLINEUPDREG335	4	Teletext line 335 update enable.	
	TTLINEUPDREG318	3	Teletext line 318 update enable.	
	TTLINEUPDREG22	2	Teletext line 22 update enable.	
	TTCRIWINDMODE	1	Teletext clock run-in window mode. 0: Teletext clock run-in start-point and end-point are using TtIniCriWindStrPt and TtIniCriWindEndPt in initial state and TtSdyCriWindStrPt and TtSdyCriWindEndPt in steady state. ; 1: Teletext clock run-in start-point and end-point are always using TtIniCriWindStrPt and TtIniCriWindEndPt.	
	TTINICRIWINDSTRPT_8	0	Teletext initial clock run-in window start point (MSB).	
E6h	**REGE6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTLINEUPDREG06_13[7:0]	7:0	Teletext line 6 to 13 (bit 7 to 0) update enable.	
E8h	**REGE8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTLINEUPDREG14_21[7:0]	7:0	Teletext line 14 to 21 (bit 7 to 0) update enable.	
EAh	**REGEA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTLINEUPDREG319_326[7:0]	7:0	Teletext line 319 to 326 (bit 7 to 0) update enable.	
ECh	**REGEC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTLINEUPDREG327_334[7:0]	7:0	Teletext line 327 to 334 (bit 7 to 0) update enable.	
EEh	**REGEE**	**7:0**	**Default : 0x1A**	**Access : R/W**
	TTCRIAMPACCPT[7:0]	7:0	Teletext clock run-in amplitude accumulation start point.	
F0h	**REGF0**	**7:0**	**Default : 0x01**	**Access : R/W**
	TTDPLLPT[7:0]	7:0	Teletext DPLL start point.	
F2h	**REGF2**	**7:0**	**Default : 0x7D**	**Access : R/W**
	TTBLKLVLPT[7:0]	7:0	Teletext blank level accumulation start point.	
F4h	**REGF4**	**7:0**	**Default : 0xCF**	**Access : R/W**
	TTVBILINEEND_4_3[1:0]	7:6	Teletext VBI line end (upper 2 bits). It is used to generate a notice signal to ttdec_top to indicate Teletext data is received in this field.	
	TTDPLLENLEN[5:0]	5:0	Teletext DPLL enable length.	
F6h	**REGF6**	**7:0**	**Default : 0x27**	**Access : R/W**
	TTFRAMCODE[7:0]	7:0	Teletext framing code value.	
F8h	**REGF8**	**7:0**	**Default : 0x06**	**Access : R/W**
	TTVBILINEEND_2_0[2:0]	7:5	Teletext VBI line end (lower 3 bits).	
	TTDATLINESTR1[4:0]	4:0	Teletext data line start 1 (odd field).	
FAh	**REGFA**	**7:0**	**Default : 0x36**	**Access : R/W**

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Index	Mnemonic	Bit	Description	
	TTFCWINDMODE	7	Teletext framing code window mode. This is valid when TtCriWindMode = 1.	
	TTFCERRBOND	6	Teletext framing code error bond value. 0: Fully match framing code. 1: Allow 1 error in framing code.	
	TTSLICERRDYMODE	5	Teletext slicer ready mode. 0: Teletext slicer is ready when TtFcCnt >= TtFcCntThd at TtChkPt ; 1: Teletext slicer is ready when TtFcCnt >= TtFcCntThd ;	
	TTDATLINEEND1[4:0]	4:0	Teletext data line end 1 (odd field).	
FCh	**REGFC**	**7:0**	**Default : 0x85**	**Access : R/W**
	TTINITPKTEN	7	Teletext initial packet counter enable. 0: Packet counter increases when Teletext packet is detected with upper-bound (TtVbiBufLen) ; 1: packet counter increases when Teletext packet is detected without upper-bound.	
	-	6:5	Reserved.	
	TTDATLINESTR2[4:0]	4:0	Teletext data line start 2 (even field).	
FEh	**REGFE**	**7:0**	**Default : 0xF6**	**Access : R/W**
	TTBASEADDRSEL	7	Teletext base address source selection.	
	TTSLPTRMODE[1:0]	6:5	Teletext single line point mode. [1]: 1: start from the line when previous line is no Teletext ; 0: start from TtDatLineStrl. [0]: 1: Enable TTSLPTRMODE ; 0: Disable TTSLPTRMODE.	
	TTDATLINEEND2[4:0]	4:0	Teletext data line end 2 (even field).	
00h	**REG00**	**7:0**	**Default : 0x54**	**Access : R/W**
	TTKPSELMAN[2:0]	7:5	Teletext DPLL phase error gain parameter selection. 0: 2^-9; 1: 2^-10; 2: 2^-11; 3: 2^-12; 4: 2^-13; 5: 2^-14; 6: 2^-15; 7: 2^-16.	
	TTBLKLVLMODE	4	Teletext blank level mode. 0: Calculate blank level from TtBlkLvlPt in the line set by TtBlkLvlLine. 1: Calculate blank level in every line from TtBlkLvlPt ;	
	TTBLKLVLLINE[3:0]	3:0	Teletext blank level line.	
02h	**REG02**	**7:0**	**Default : 0x37**	**Access : R/W**
	TTCRIAMPTHD[7:0]	7:0	Teletext clock run-in amplitude threshold.	
04h	**REG04**	**7:0**	**Default : 0x8E**	**Access : R/W**

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	TTPHACCINCNORM1_15_8[7:0]	7:0	Teletext phase accumulated incremental normalized parameter 1, used in PAL.	
06h	**REG06**	**7:0**	**Default : 0x6B**	**Access : R/W**
	TTPHACCINCNORM1_7_0[7:0]	7:0	Teletext phase accumulated incremental normalized parameter 1, used in PAL.	
08h	**REG08**	**7:0**	**Default : 0x36**	**Access : R/W**
	TTINICRIWINDENDPT_7_0[7:0]	7:0	Teletext initial clock run-in window end point (lower 8 bits).	
0Ah	**REG0A**	**7:0**	**Default : 0x80**	**Access : R/W**
	TTINICRIWINDENDPT_8	7	Teletext initial clock run-in window end point (MSB).	
	-	6:0	Reserved.	
0Ch	**REG0C**	**7:0**	**Default : 0x8C**	**Access : R/W**
	TTMUCRIAMP[1:0]	7:6	Teletext blending parameter for clock run-in amplitude. 0: 1/4; 1: 1/8 ; 2: 1/16; 3: 1/32.	
	TTCRIWINDLEN[5:0]	5:0	Teletext clock run-in window length.	
0Eh	**REG0E**	**7:0**	**Default : 0x19**	**Access : R/W**
	TTSLCTHDTRKPT[7:0]	7:0	Teletext slicer threshold track point. If TtSlcThdAdpOn = 1, slice threshold automatic tracking would be started after TTSLCTHDTRKPT.	
10h	**REG10**	**7:0**	**Default : 0x14**	**Access : R/W**
	TTSDYFCMONCNTTHD[7:0]	7:0	Teletext line monitor counter threshold in steady state. TtChkPt is at TtDatLineEnd when TtMonCnt = TTSDYFCMONCNTTHD.	
12h	**REG12**	**7:0**	**Default : 0xC1**	**Access : R/W**
	TTINITPKTSEL	7	Teletext packet receiving mode selection. 0: Refresh when the field changes ; 1: refresh when reaching TtVbiBufLen.	
	TTPHACCMODE	6	Teletext phase accumulation parameter mode. 0: Depend on SCM_FSC ; 1: depend on TtPhAccType.	
	TTPHACCTYPE	5	0: TtPhAccIncNorm1 ; 1: TtPhAccIncNorm2.	
	TTSRCHFCCNTTHD[4:0]	4:0	Teletext framing code counter threshold in search-framing-code state. If TtFcCnt were not over threshold, re-training would be ignited.	
14h	**REG14**	**7:0**	**Default : 0x31**	**Access : R/W**
	-	7	Reserved.	
	TTCRIAMPHALFHLMT_9_8[1:0]	6:5	Teletext CRI half amplitude high limit (upper 2 bits).	

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	TTSDYFCCNTTHD[4:0]	4:0	Teletext framing code counter threshold in steady state. It's also used as Teletext trigger line for debugging.	
16h	**REG16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	TTSRCHFCMONCNTTHD[4:0]	4:0	Teletext line monitor counter threshold in search-framing-code state. TtChkPt is at TtDatLineEnd when TtMonCnt = TTSRCHFCMONCNTTHD.	
18h	**REG18**	**7:0**	**Default : 0x9A**	**Access : R/W**
	TTMUCRIFOUNDPT[1:0]	7:6	Teletext blending parameter for clock run-in found point. 0: 1/2 ; 1: 1/4 ; 2: 1/8 ; 3: 1/16.	
	TTLVLAVGMD	5	Teletext slicer level average mode. 0: 16 samples ; 1: 8 samples.	
	-	4	Reserved.	
	TTFASTDPLLACQON	3	Teletext fast DPLL acquisition on.	
	TTSYMBINTPBASE[2:0]	2:0	Teletext symbol interpolation base.	
1Ah	**REG1A**	**7:0**	**Default : 0xE5**	**Access : R/W**
	TTSLCTHDADPON	7	Teletext slicer threshold adaptation on.	
	TTSIGDETSEL	6	Teletext signal detection type selection. 0: TtSlcThd is based on TtBlkLvl+TtCriAmpValHalf, which are average values after accumulation. TtCriFound is base on mode0. ; 1: TtSlcThd is based on CcDin1_2Fsc with error adjustment. TtCriFound is based on mode1;	
	TTMUSLCTHDERR[1:0]	5:4	Teletext slicer threshold error parameter selection, useful when TtSigDetSel=1. 0: 1/8 ; 1: 1/16 ; 2: 1/32 ; 3: 1/64.	
	TTSLCTHDLATSEL[1:0]	3:2	Teletext slicer threshold latch selection. Select delay point of CcDin1_2Fsc for slice threshold. 0: 0 ; 1: 1 ; 2: 2 ; 3: 3.	
	TTBLKLVLLATSEL[1:0]	1:0	Teletext blank level latch selection. Select delay point of CcDin1_2Fsc for blank level. 0: 12 ; 1: 11 ; 2: 10 ; 3: 9.	
1Ch	**REG1C**	**7:0**	**Default : 0x78**	**Access : R/W**
	TTPHACCINCNORM2_15_8[7:0]	7:0	Teletext phase accumulated incremental normalized parameter 2, used in SECAM.	

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1Eh	**REG1E**	**7:0**	**Default : 0x81**	**Access : R/W**
	TTPHACCINCNORM2_7_0[7:0]	7:0	Teletext phase accumulated incremental normalized parameter 2, used in SECAM.	
20h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
22h	**REG22**	**7:0**	**Default : 0x50**	**Access : R/W**
	TTLINE_CNTRFLDTHD_9_8[1:0]	7:6	Teletext line counter folded threshold (upper 2 bits).	
	TTCRIDETSEL	5	0: The same as TtSigDetSel setting. 1: Inversion of TtSigDetSel setting.	
	VPSDATLINESTR[4:0]	4:0	VPS data line start definition.	
24h	**REG24**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7	Reserved.	
	VPSCRIWINDENDPT_9_8[1:0]	6:5	VPS clock run-in window end point (upper 2 bits).	
	VPSDATLINEEND[4:0]	4:0	VPS data line end definition.	
26h	**REG26**	**7:0**	**Default : 0xA3**	**Access : R/W**
	VPSCRIWINDSTRPT[7:0]	7:0	VPS clock run-in window start point.	
28h	**REG28**	**7:0**	**Default : 0x86**	**Access : R/W**
	VPSCRIWINDENDPT_7_0[7:0]	7:0	VPS clock run-in window end point (lower 7 bits).	
2Ah	**REG2A**	**7:0**	**Default : 0x36**	**Access : R/W**
	VPSSLCTHDPT[7:0]	7:0	VPS start point for slicer threshold calculation.	
2Ch	**REG2C**	**7:0**	**Default : 0x14**	**Access : R/W**
	VPSDPLLPT[7:0]	7:0	VPS DPLL start point.	
2Eh	**REG2E**	**7:0**	**Default : 0x0F**	**Access : R/W**
	TTFCWINDENDPT_9_8[1:0]	7:6	Teletext framing code window end point (upper 2 bits).	
	VPSDPLLENLEN[5:0]	5:0	VPS DPLL enable length.	
30h	**REG30**	**7:0**	**Default : 0x37**	**Access : R/W**
	VPSCRIAMPTHD[7:0]	7:0	VPS clock run-in amplitude threshold.	
32h	**REG32**	**7:0**	**Default : 0x8C**	**Access : R/W**
	VPSPHACCINCNORM_15_8[7:0]	7:0	VPS phase accumulation incremental normalized parameter.	
34h	**REG34**	**7:0**	**Default : 0x01**	**Access : R/W**
	VPSPHACCINCNORM_7_0[7:0]	7:0	VPS phase accumulation incremental normalized parameter.	
3Ah	**REG3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TTBASEADDR1_7_0[7:0]	7:0	Teletext base address 1 (lower 8 bits).	
3Ch	**REG3C**	**7:0**	**Default : 0xFF**	**Access : R/W**

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	TTBASEADDR1_15_8[7:0]	7:0	Teletext base address 1 (middle 8 bits).	
3Eh	**REG3E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTBASEADDR1_23_16[7:0]	7:0	Teletext base address 1 (upper 8 bits).	
40h	**REG40**	**7:0**	**Default : 0xAF**	**Access : R/W**
	TTFCWINDENDPT_7_0[7:0]	7:0	Teletext framing code window end point (lower 8 bits).	
42h	**REG42**	**7:0**	**Default : 0x39**	**Access : R/W**
	TTLINE_CNTRFLDTHD_7_0[7:0]	7:0	Teletext line counter folded threshold (lower 8 bits).	
44h	**REG44**	**7:0**	**Default : 0x24**	**Access : R/W**
	TTCRIAMPHALFLLMT[7:0]	7:0	Teletext CRI half amplitude low limit.	
46h	**REG46**	**7:0**	**Default : 0x2C**	**Access : R/W**
	TTCRIAMPHALFHLMT_7_0[7:0]	7:0	Teletext CRI half amplitude high limit (lower 8 bits).	
4Ah	**REG4A**	**7:0**	**Default : 0x00**	**Access : RO**
	VPSSCCNT_3_0[3:0]	7:4	VPS start code counter.	
	WSSSCCNT_3_0[3:0]	3:0	WSS start code counter.	
4Ch	**REG4C**	**7:0**	**Default : 0x00**	**Access : RO**
	VPSBYTE3[7:0]	7:0	VPS byte 3, which is the received byte set by VpsByteIdx3.	
4Eh	**REG4E**	**7:0**	**Default : 0x00**	**Access : RO**
	VPSBYTE4[7:0]	7:0	VPS byte 4, which is the received byte set by VpsByteIdx4.	
50h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
52h	**REG52**	**7:0**	**Default : 0x00**	**Access : RO**
	TTPKTCNT_7_0[7:0]	7:0	Teletext packet counter (lower 8 bits).	
54h	**REG54**	**7:0**	**Default : 0x00**	**Access : RO**
	TTPKTCNT_15_8[7:0]	7:0	Teletext packet counter (upper 8 bits).	
56h	**REG56**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TTFLDCNT[3:0]	3:0	Teletext field counter.	
58h	**REG58**	**7:0**	**Default : 0x00**	**Access : RO**
	VPSBITBIPHERRCNT1[3:0]	7:4	VPS bit bi-phase error counter 1 (Index 1 byte).	
	VPSBITBIPHERRCNT2[3:0]	3:0	VPS bit bi-phase error counter 2 (Index 2 byte).	
5Ah	**REG5A**	**7:0**	**Default : 0x00**	**Access : RO**
	VPSBYTE1[7:0]	7:0	VPS byte 1, which is the received byte set by VpsByteIdx1.	
5Ch	**REG5C**	**7:0**	**Default : 0x00**	**Access : RO**
	VPSBYTE2[7:0]	7:0	VPS byte 2, which is the received byte set by VpsByteIdx2.	

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5Eh	**REG5E**	**7:0**	**Default : 0x00**	**Access : RO**
	WSSSCSTUS	7	WSS start code status. 1 when WssScCnt >= WssScRealCntThd, set by WssSdyScRealCntThd or WssPullScRealCntThd.	
	WSSSLICERRDY	6	WSS slicer ready indication.	
	-	5	Reserved.	
	VPSSLICERRDY	4	VPS slicer ready indication. 1 when VpsScCnt >= VpsScCntThd, set by VpsSrchScCntThd or VpsSdyScCntThd, and VPS state is steady.	
	-	3:2	Reserved.	
	TTSLICERRDY	1	Teletext slicer ready indication. 1 when TtFcCnt >= TtFcCntThd at TtChkPt and TtState is steady.	
	-	0	Reserved.	
60h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
62h	**REG62**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:4	Reserved.	
	VPSSRCHSCMONCNTTHD[3:0]	3:0	VPS search start code monitor counter threshold.	
64h	**REG64**	**7:0**	**Default : 0x8A**	**Access : R/W**
	VPSSTRCODE_15_8[7:0]	7:0	VPS start code (upper 8 bits).	
66h	**REG66**	**7:0**	**Default : 0x99**	**Access : R/W**
	VPSSTRCODE_7_0[7:0]	7:0	VPS start code (lower 8 bits).	
68h	**REG68**	**7:0**	**Default : 0x42**	**Access : R/W**
	VPSKPSELMAN[2:0]	7:5	VPS DPLL gain parameter selection. 0: 2^-9 ; 1: 2^-10 ; 2: 2^-11 ; 3: 2^-12 ; 4: 2^-13 ; 5: 2^-14 ; 6: 2^-15 ; 7: 2^-16.	
	VPSSRCHSCCNTTHD[4:0]	4:0	VPS search start code counter threshold. Refer to VpsSlicerRdy.	
6Ah	**REG6A**	**7:0**	**Default : 0x61**	**Access : R/W**
	VPSSYMBINTPBASE[2:0]	7:5	VPS symbol interpolation base.	
	VPSSDYSCCNTTHD[4:0]	4:0	VPS steady state start code counter threshold. Refer to VpsSlicerRdy.	
6Ch	**REG6C**	**7:0**	**Default : 0xB5**	**Access : R/W**
	VPSBYTEIDX4[3:0]	7:4	VPS byte index 4.	

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	VPSBYTEIDX3[3:0]	3:0	VPS byte index 3.	
6Eh	**REG6E**	**7:0**	**Default : 0xED**	**Access : R/W**
	VPSBYTEIDX2[3:0]	7:4	VPS byte index 2.	
	VPSBYTEIDX1[3:0]	3:0	VPS byte index 1.	
70h	**REG70**	**7:0**	**Default : 0x4F**	**Access : R/W**
	VPSSCWINDENDPT_9_8[1:0]	7:6	VPS start code window end point (upper 2 bits).	
	VPSINTTYPE	5	VPS interrupt type. 0: Issue after VPS detection line if VPS slicer is ready. 1: Always issue after VPS detection line.	
	WSSINTTYPE	4	WSS interrupt type. 0: Issue after WSS detection line if WSS slicer is ready. 1: Always issue afterWSS detection line.	
	VPSBYTENUM[3:0]	3:0	VPS byte number.	
72h	**REG72**	**7:0**	**Default : 0x7D**	**Access : R/W**
	VWBLKLVLPT[7:0]	7:0	VPS / WSS start point for blank level calculation.	
74h	**REG74**	**7:0**	**Default : 0x63**	**Access : R/W**
	VPSSCWINDENDPT_7_0[7:0]	7:0	VPS / WSS start code window end point (lower 8 bits).	
76h	**REG76**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:6	Reserved.	
	WSSDATACHKOP	5	WSS data check option. 0: No checking data difference. 1: Checking data difference.	
	VPSSDYSCMONCNTTHD[4:0]	4:0	VPS steady state start code monitor counter threshold.	
78h	**REG78**	**7:0**	**Default : 0x40**	**Access : R/W**
	WSS525SYMBINTPBASE[7:0]	7:0	WSS symbol interpolation base for NTSC 525-line system.	
7Ah	**REG7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	WSS525PHACCINC[7:0]	7:0	WSS phase accumulation incremental parameter for NTSC 525-line system.	
7Ch	**REG7C**	**7:0**	**Default : 0x78**	**Access : R/W**
	WSSCRIAMPTHD_N[7:0]	7:0	WSS clock run-in amplitude threshold for NTSC 525-line system.	
7Eh	**REG7E**	**7:0**	**Default : 0x58**	**Access : R/W**
	NP_MODE[1:0]	7:6	NTSC/PAL mode selection for debugging.	
	WSSBITIDTHRSD[5:0]	5:0	WSS bit identification threshold for 525-line system. 1 bit equals 32 cycles at 4*Fsc.	

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Index	**Mnemonic**	**Bit**	**Description**	
80h	**REG80**	**7:0**	**Default : 0x57**	**Access : R/W**
	WSSKPSELMAN[2:0]	7:5	WSS DPLL gain parameter selection. 0: 2^-9 ; 1: 2^-10 ; 2: 2^-11 ; 3: 2^-12 ; 4: 2^-13 ; 5: 2^-14 ; 6: 2^-15 ; 7: 2^-16.	
	WSSDATLINESTR_P[4:0]	4:0	WSS Data start line for PAL 625-line system.	
82h	**REG82**	**7:0**	**Default : 0xA3**	**Access : R/W**
	WSSCRIWINDSTRPT[7:0]	7:0	WSS clock run-in window start point.	
84h	**REG84**	**7:0**	**Default : 0x9C**	**Access : R/W**
	WSSCRIWINDENDPT_7_0[7:0]	7:0	WSS clock run-in window end point (lower 8 bits).	
86h	**REG86**	**7:0**	**Default : 0x4B**	**Access : R/W**
	WSSCRIWINDENDPT_9_8[1:0]	7:6	WSS clock run-in window end point (upper 2 bits).	
	WSSDPLLENLEN[5:0]	5:0	WSS DPLL enable length.	
88h	**REG88**	**7:0**	**Default : 0x32**	**Access : R/W**
	WSSSLCTHDENENDPT[7:0]	7:0	WSS slicer threshold enable end point.	
8Ah	**REG8A**	**7:0**	**Default : 0x78**	**Access : R/W**
	WSSCRIAMPTHD_P[7:0]	7:0	WSS clock run-in amplitude threshold for PAL 625-line system.	
8Ch	**REG8C**	**7:0**	**Default : 0xB8**	**Access : R/W**
	WSSSCWINDENDPT_7_0[7:0]	7:0	WSS start code window end point (lower 8 bits).	
8Eh	**REG8E**	**7:0**	**Default : 0x1E**	**Access : R/W**
	WSSSTRCODE_23_16[7:0]	7:0	WSS start code (upper 8 elements).	
90h	**REG90**	**7:0**	**Default : 0x3C**	**Access : R/W**
	WSSSTRCODE_15_8[7:0]	7:0	WSS start code (middle 8 elements).	
92h	**REG92**	**7:0**	**Default : 0x1F**	**Access : R/W**
	WSSSTRCODE_7_0[7:0]	7:0	WSS start code (lower 8 elements).	
94h	**REG94**	**7:0**	**Default : 0x42**	**Access : R/W**
	WSSPULLSCMONCNTTHD[3:0]	7:4	WSS pull-in state start code monitor counter threshold.	
	WSSPULLSCREALCNTTHD[3:0]	3:0	WSS pull-in state start code real counter threshold.	
96h	**REG96**	**7:0**	**Default : 0xC8**	**Access : R/W**
	WSSSDYSCMONCNTTHD[3:0]	7:4	WSS steady state start code monitor counter threshold.	
	WSSSDYSCREALCNTTHD[3:0]	3:0	WSS steady state start code real counter threshold.	
98h	**REG98**	**7:0**	**Default : 0xBD**	**Access : R/W**
	WSSDATLINEEND_P[4:0]	7:3	WSS Data end line for PAL 625-line system.	

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Index	**Mnemonic**	**Bit**	**Description**	
	WSSSTUSCHKOP	2	WSS status check option. 1: Depend on WssScChkPt ; 0: Original method.	
	WSSSCWINDENDPT_9_8[1:0]	1:0	WSS start code window end point (upper 2 bits).	
9Ah	**REG9A**	**7:0**	**Default : 0x00**	**Access : RO**
	WSSWORD_7_0[7:0]	7:0	WSS Word (lower 8 bits).	
9Ch	**REG9C**	**7:0**	**Default : 0x00**	**Access : RO**
	WSSWORD_15_8[7:0]	7:0	WSS Word (middle 8 bits).	
9Eh	**REG9E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	WSSWORD_19_16[3:0]	3:0	WSS Word (upper 4 bits).	
C0h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
C2h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SECAM Register (Bank = 1038)

SECAM Register (Bank = 1038)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h	**REG02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCM_RST	7	SECAM software reset. 1: Reset ; 0: normal operation.	
	MIXC_EN	6	Chroma mixing enable. 1: Enable according to settings of Wfunc_iso and Ydev_thrsd ; 0: disable.	
	WFUNC_ISO	5	Chroma weighting function isolation. 0: Normal; 1: Isolate asymmetric weighting.	
	SCM_RES_OP	4	SCM_RESULT report option. 0: Immediate. 1: During VBI.	
	-	3	Reserved.	
	ID_MODE	2	Identification mode selection. Set to 1 only if using frame ID for SECAM detection in line 7~15 and line 320~328.	

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SECAM Register (Bank = 1038)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCMID_OP	1	SECAM identification option. 1: Ignore VD state stable condition. 0: Identification is on when VD state is stable.	
	SCMID_EN	0	SECAM identification forced enable.	
04h	**REG04**	**7:0**	**Default : 0x98**	**Access : R/W**
	SAMPLE_ST0_7_0[7:0]	7:0	Start of sample point (lower 8 bits) for 4.43MHz.	
06h	**REG06**	**7:0**	**Default : 0xA4**	**Access : R/W**
	SAMPLE_END0_7_0[7:0]	7:0	End of sample point (lower 8 bits) for 4.43MHz.	
08h	**REG08**	**7:0**	**Default : 0x1B**	**Access : R/W**
	LINE_STA[7:0]	7:0	Start of line number of odd field.	
0Ah	**REG0A**	**7:0**	**Default : 0x54**	**Access : R/W**
	LINE_STB_7_0[7:0]	7:0	Start of line number of even field.	
0Ch	**REG0C**	**7:0**	**Default : 0x01**	**Access : R/W**
	SAMPLE_ST0_10_8[2:0]	7:5	Start of sample point (upper 3 bits) for 4.43MHz.	
	SAMPLE_END0_10_8[2:0]	4:2	End of sample point (upper 3 bits) for 4.43MHz.	
	LINE_STB_9_8[1:0]	1:0	Start of line number of even field (upper 2 bits).	
0Eh	**REG0E**	**7:0**	**Default : 0xF0**	**Access : R/W**
	LINE_LEN0[7:0]	7:0	Length of obervation line for 4.43MHz.	
10h	**REG10**	**7:0**	**Default : 0x01**	**Access : R/W**
	SCM_Y2Y601_BP	7	SECAM Y(Luma) to BT601 operation bypassing option.	
	MAG_MODE[1:0]	6:5	0: Original value. 1: Mag_int/2; 2: mag_int/8; 3: mag/32.	
	ID_CTR_MODE[1:0]	4:3	SECAM identification criterion mode. 0: Depend on magnitude difference. 1: Depend on magnitude and sign difference. 2: Depend on magnitude difference and sign flipping. 3: Depend on magnitude difference, sign difference, and sign flipping.	
	ID_ACT_FIELD[2:0]	2:0	Active field number of SECAM identification.	
12h	**REG12**	**7:0**	**Default : 0x60**	**Access : R/W**
	MAG_THRSD44_7_0[7:0]	7:0	Magnitude threshold for Fsc 4.43MHz (lower 8 bits).	
14h	**REG14**	**7:0**	**Default : 0x21**	**Access : R/W**
	MAG_THRSD44_15_8[7:0]	7:0	Magnitude threshold for Fsc 4.43MHz (middle 8 bits).	
16h	**REG16**	**7:0**	**Default : 0x40**	**Access : R/W**

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SECAM Register (Bank = 1038)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	LINE_PIXNUM_10_8[2:0]	6:4	Pixel number of line buffer (upper 3 bits).	
	MAG_THRSD44_19_16[3:0]	3:0	Magnitude threshold for Fsc 4.43MHz (upper 4 bits).	
18h	**REG18**	**7:0**	**Default : 0x48**	**Access : R/W**
	LINE_PIXNUM_7_0[7:0]	7:0	Pixel number of line buffer (if the number is 1097, program 11'h448).	
1Ah	**REG1A**	**7:0**	**Default : 0x06**	**Access : R/W**
	ID_THRSD[7:0]	7:0	Threshold for SECAM identification.	
1Ch	**REG1C**	**7:0**	**Default : 0x88**	**Access : R/W**
	NONSCM_THRSD[3:0]	7:4	Non-SECAM decision threshold.	
	SCM_THRSD[3:0]	3:0	SECAM decision threshold.	
20h	**REG20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAG_THRSD42_7_0[7:0]	7:0	Magnitude threshold for Fsc 4.285MHz (lower 8 bits).	
22h	**REG22**	**7:0**	**Default : 0x20**	**Access : R/W**
	MAG_THRSD42_15_8[7:0]	7:0	Magnitude threshold for Fsc 4.285MHz (middle 8 bits).	
24h	**REG24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAG_THRSD42_19_16[3:0]	3:0	Magnitude threshold for Fsc 4.285MHz (upper 4 bits).	
26h	**REG26**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAG_DEV_THRSD_7_0[7:0]	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned lower 8 bits).	
28h	**REG28**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAG_DEV_THRSD_15_8[7:0]	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned upper 8 bits).	
2Ah	**REG2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HW_SCM_COFF_EN	7	Hardware SECAM color-off enable. 0: Disable ; 1: Enable.	
	SCM_COFF_THRSD[6:0]	6:0	Hardware SECAM color-off threshold (2 lines / unit).	
2Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h	**REG32**	**7:0**	**Default : 0x03**	**Access : R/W**

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SECAM Register (Bank = 1038)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCM_BPYN	7	Bypass Y(Luma) notch filter option. 0: Normal mode. 1: Bypass mode.	
	OBV_MODE	6	Observation mode. 0: Field base. 1: Within one field.	
	-	5:4	Reserved.	
	SCMGCLK_OP	3	SECAM clock gating option. 0: Gate SECAM clock when operating at 3.58MHZ(or not stable VD state) ; 1: No clock gating.	
	CMBGCLK_OP	2	Comb clock gating option. 1: Gate comb filter clock when SECAM decoder is operating. 0: No clock gating.	
	CLPMD[1:0]	1:0	Chroma LPF mode. 0: Bypass ; 1: 1.5MHz ; 2: 1.25MHz ; 3: 1MHz.	
34h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
36h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
38h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Ah	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Ch	**REG3C**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_YSEP_FLTMD[2:0]	7:5	Y seperation filter selection.	
	SCM_CBCRLPON	4	SECAM Cb/Cr LPF switch. 0: Off ; 1: on.	
	LUMAFIXMD	3	Luma Fix Mode. 0: Normal ; 1: Luma is controlled by SDBKLevel.	
	SCM_YDLYMD[2:0]	2:0	SECAN Luma(Y) delay mode. 0: Advance 4 ; 1: advance 3 ; 2: advance 2 ; 3: advance 1 ; 4: normal ; 5: delay 1 ; 6: delay 2 ; 7: delay 3.	
3Eh	**REG3E**	**7:0**	**Default : 0x30**	**Access : RO, R/W**
	SCM_IRQ_FORCE[1:0]	7:6	SECAM Interrupt force bits.	
	SCM_IRQ_MASK[1:0]	5:4	SECAM Interrupt mask bits.	

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SECAM Register (Bank = 1038)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCM_IRQ_CLR[1:0]	3:2	SECAM Interrupt clear bits.	
	SCM_IRQ_STATUS[1:0]	1:0	SECAM Interrupt status bits.	
40h	**REG40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCMINTTYPE	3	SECAM interrupt type. 0: Issue when SECAM ID result changes ; 1: issue when detection related data updates.	
	-	2:0	Reserved.	
5Ch	**REG5C**	**7:0**	**Default : 0x06**	**Access : R/W**
	TRIG_LINE_NUM_7_0[7:0]	7:0	Trigger line number for generating interrupt (lower 8 bits).	
5Eh	**REG5E**	**7:0**	**Default : 0x80**	**Access : R/W**
	SCM_CGAINMD	7	SECAM chroma gain register mode. 0: Controlled by DSP ; 1: Controlled by 2Fh[6:5].	
	SCM_CGAINREG[1:0]	6:5	SECAM chroma Gain. 1: X2 ; 2: x4 ; others:x1.	
	-	4:2	Reserved.	
	TRIG_LINE_NUM_9_8[1:0]	1:0	Trigger line number for generating interrupt (upper 2 bits).	
60h	**REG60**	**7:0**	**Default : 0x00**	**Access : RO**
	SCMID_DONE	7	SECAM Identification done indication.	
	SCMID_YES	6	SECAM signal found bit.	
	DR_LINE	5	Dr line indication.	
	DB_LINE	4	Db line indication.	
	INTB	3	Line type indication.	
	SCMID_STS[2:0]	2:0	SECAM ID status (3'b000->idle ; 3'b001,3'b010,3'b011->ID progress ; 3'b110->SECAM ; 3'b111->no SECAM signal discovery.	
6Ah	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
6Ch	**REG6C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HW_SCM_COFF	4	Hardware SECAM color-off indication.	
	-	3:2	Reserved.	

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SECAM Register (Bank = 1038)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	SCM_FSC[1:0]	1:0	Fsc status from AFEC_TOP. 2'b00->NTSC 3.58MHz ; 2'b01->PAL 4.43MHz ; 2'b10->SECAM 4.285156MHz.

UTMI2 Register (Bank = 1039)

UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (103900h)	**REG103900**	**7:0**	**Default : 0x05**	**Access : R/W**
	R_DM_PDEN	7	Override value to Enable FS/LS DM pull-down resistor. 0 = normal. 1 = pull down.	
	R_DP_PDEN	6	Override value to Enable FS/LS DP pull-down resistor. 0 = normal. 1 = pull down.	
	R_PUMODE	5	Override DP/DM pull-up resistor value control. 0 = Pull-up resistor ~ 900~1575 ohm. 1 = Pull-up resistor ~ 1425~3090 ohm.	
	DM_PUEN	4	Override value to Enable FS/LS DM pull-up resistor. 0 = normal. 1 = pull up.	
	DP_PUEN	3	Override value to Enable FS/LS DP pull-up resistor. 0 = normal. 1 = pull up.	
	REF_PDN	2	Override value to Power-down USB_XCVR reference block. 0 = normal. 1 = power down.	
	TERM_OVERRIDE	1	Enable FS/LS termination override mode. 0 = Disable. 1 = Enable override mode.	
	PDN_OVERRIDE	0	Enable USB_XCVR power-down control override mode. 0 = Disable. 1 = Enable override mode.	
00h	**REG103901**	**7:0**	**Default : 0xFF**	**Access : R/W**

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103901h)	REG_PDN	7	Override value to Power-down USB_XCVR build-in regulator block. 0 = normal. 1 = power down.	
	IREF_PDN	6	Override value to Power-down USB_XCVR HS current reference block. 0 = normal. 1 = power down.	
	VBUSDET_PDN	5	Override value to Power-down USB_XCVR VBUS detector block. 0 = normal. 1 = power down.	
	FL_XCVR_PDN	4	Override value to Power-down USB_XCVR FS/LS transceiver block. 0 = normal. 1 = power down.	
	HS_PREAMP_PDN	3	Override value to Power-down USB_XCVR HS pre-amplifier block. 0 = normal. 1 = power down.	
	HS_TED_PDN	2	Override value to Power-down USB_XCVR HS TED block. (squelch circuit). 0 = normal. 1 = power down.	
	PLL_PDN	1	Override value to Power-down USB_XCVR PLL block. 0 = normal. 1 = power down.	
	HS_DM_PDN	0	Override value to Power-down USB_XCVR HS de-serializer block. 0 = normal. 1 = power down.	
01h (103902h)	**REG103902**	**7:0**	**Default : 0x80**	**Access : R/W**
	BOND_SEL	7	Select internal regulator. 0 = Use external regulator. 1 = Use internal regulator.	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HS_TX_TEN	6	Force enable HS_TX analog Parallel-to-Serial function.(No use). 0 = Normal. 1 = force enable current source.	
	FL_LOWIMODE	5	Full/Low speed receiver power saving mode. 0 = Normal. 1 = Enable Low current mode.	
	BITSTUFF_EN	4	Override value to control Bit-Stuff mode. 0 = Force Bit-Stuff disable. 1 = Force Bit-Stuff enable.	
	NRZI_EN	3	Override value to control NRZI mode. 0 = Force NRZI disable. 1 = Force NRZI enable.	
	CLK12_SEL	2	PLL 12MHz reference clock source select. 0 = From XTAL_IN.(12Mhz). 1 = From digital synthesizer.(48Mhz-N.f).	
	FSLS_SEL	1	Override value to select Full/Low speed USB_XCVR. 0 = Full speed mode. 1 = Low speed mode.	
	SEL_OVERRIDE	0	Source select and enable override control. (No use).	
01h (103903h)	**REG103903**	**7:0**	**Default : 0x90**	**Access : R/W**
	HS_RTERM_PDN	7	Power down option of high speed terminal resistor.	
	LINESTATE_SEL	6	Line state mode report selection in HS mode. 0 = Normal. 1 = select RX_CHIRP as line state.	
	EOP40_DET_DELAY_CNT[2:0]	5:3	HS EOP_40 window delay for disconnect detection. (1T = 1/120 MHz). 00 = no delay. 01 = delay 1T. 10 = delay 2T. 11 = delay 3T. (Default value is 2).	
	FL_SEL_OVERRIDE	2	Full/Low speed mode select override value. 0 = Normal. 1 = Controlled by register fs_ls_sel (bit-1).	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NRZI_OVERRIDE	1	NRZI enable controlled by register. 0 = Normal. 1 = Controlled by nrzi_en (bit-3).	
	BITSTUFF_OVERRIDE	0	Bit-stuff enable controlled by register. 0 = Normal. 1 = Controlled by bitstuff_en (bit-4).	
02h (103904h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (103905h)	**REG103905**	**7:0**	**Default : 0x30**	**Access : R/W**
	UTMI_TX_WAIT_CNT[3:0]	7:4	TX HS delay for min inter-packet 32 bit-time wait state. (1T = 1/120 MHz). 000 = zero wait state. 001 = 1T. .... 101 = 6T. 111 = 7T. (Default is 3).	
	TX_OUT_SEL_MULTI_PHASE[1:0]	3:2	UTMI TX OUT multi cycle phase selection. 00 = phase 0. 01 = phase 1. 10 = phase 2. 11 = phase 3.	
	TX_IN_SEL_MULTI_PHASE[1:0]	1:0	UTMI TX IN Multi cycle phase selection. 00 = phase 0. 01 = phase 1. 10 = phase 2. 11 = phase 3.	
03h (103906h)	**REG103906**	**7:0**	**Default : 0x20**	**Access : R/W**
	OTG_DUAL_ROLE	7	Enable OTG dual role mode. 0 = Register control. 1 = Normal function.(OTG mode).	
	HS_STAGE_SELECT[1:0]	6:5	RX HS data recovery reference stage control. 00 = 1 stage. 01 = 2 stage. 00 = 3 stage. 01 = 4 stage. (Default is 1).	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_FL_LATENCY_DELAY_1	4	TX in Full/Low speed mode delay 1 DFF. 0 = normal (combinational out to analog). 1 = Enable (DFF out to analog).	
	TX_FL_EARLY_4	3	TX in fl mode 4 to 1 fifo bypass 1 DFF.(no use). 0 = Disable. 1 = Enable.	
	TX_FORCE_HS_CURRENT_ENABLE	2	Force HS TX current source enable. 0 = Normal. 1 = Force current source.	
	UTMI_TX_SW_RESET	1	UTMI TX software reset. 0 = Normal. 1 = Enable software reset.	
	RX_SWRESET	0	UTMI RX software reset. 0 = Normal. 1 = Enable software reset.	
03h (103907h)	**REG103907**	**7:0**	**Default : 0x30**	**Access : R/W**
	VBUSDET_TEST[1:0]	7:6	VBUS_VALID LEVEL SELECT (the effect of 5k load resistor is including). 00: 4.35V. 01: 4.13V. 10: 3.92V. 11: 4.56V.	
	TX_RESERVED[3:0]	5:2	[1:0] = clock_switch_sel (Default is 2'b00). [2] = cid_over_dis (Default is 1). [3] = vbus_over_dis (Default is 1).	
	CDR_MODE_SEL	1	RX HS data recovery voting mode select. 0 = old cdr mode. 1 = new cdr mode select to collect more RX edge information.	
	TX_RESET_FSM	0	Synchronous TX FSM software reset. 0 = Disable. 1 = reset TX internal FSM engine.	
04h (103908h)	**REG103908**	**7:0**	**Default : 0x83**	**Access : R/W**
	CLK_EXTRA_0_EN	7	pd_bg_current: Power down bandgap current.	
	CLKTEST_EN	6	Test mode enable including: UPLL reset control.	
	-	5:2	Reserved.	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	UTMI_CLK120_EN	1	Override value to enable UTMI 120M clock source. 0 = stop. 1 = Enable.	
	UTMI_CLK_EN	0	Override value to enable UTMI 30MHz and 60MHz clock source. 0 = stop. 1 = Enable.	
04h (103909h)	**REG103909**	**7:0**	**Default : 0x04**	**Access : R/W**
	HS_RX_ROBOUST_EN	7	Enable High speed Rx roboust feature.	
	-	6	Reserved.	
	CLK_274_EN	5	Enable 274MHz clock output.	
	CLK214_SYN_EN	4	Enable clock synthesizer.	
	FORCE_PLL_ON	3	Override enable to enable utmi pll by register. 0 = Normal. 1 = Force utmi pll always on.	
	CLK_CTL_OVERRIDE	2	Override enable to enable clock source by register. 0 = Normal. 1 = Force clock enable by register setting.	
	XTAL12_EN	1	Register to select the source of clk_uhc. 0 = 30MHz for UPLL. 1 = crystal clock.	
	CLK_EXTRA_1_EN	0	reg_all_pass: Enable ISI improvement.	
05h (10390Ah)	**REG10390A**	**7:0**	**Default : 0x40**	**Access : R/W**
	CLK_EXTRA_0_INV	7	Reserved.	
	CLKTEST_INV	6	Register control for UPLL divider reset (low active). 0 = Reset. 1 = Normal.	
	-	5:2	Reserved.	
	UTMI_CLK120_INV	1	Inverse 120MHz clock source. 0 = Normal. 1 = Inverse clock.	
	UTMI_CLK_INV	0	Inverse 30MHz and 60MHz clock source. 0 = Normal. 1 = Inverse clock.	
05h	**REG10390B**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10390Bh)	CK_INV_RESERVED[6:0]	7:1	Reserved register. Bit <11:9>: HS_TX_CKI select. Bit <12>: enable old HS disconnect sampling mechanism. Bit <13> enable DP/DM swap mechanism. Bit <14>: disable drive port reset (for FL tranceiver only). Bit <15>: select the latch on HS data transfer interface.	
	CLK_EXTRA_1_INV	0	Inverse clock extra1. 0 = Normal. 1 = Inverse clock.	
06h (10390Ch)	**REG10390C**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAC_CLK_SEL[1:0]	7:6	MAC clock selection. Bit <6>: set to 1 represent dynamic switched clock for MAC. Set to 0 is the old FIFO access mechanism for MAC. Bit <7>: reserved.	
	TEST_CLOCK_SELECT[5:0]	5:0	UTMI test clock selection. 00h = clk_120mhz_utmi_z. 01h = clk_30mhz_utmi_z. 02h = clk_120_12_1p5_mhz_tx_fsm_z. 03h = clk_120_48_6_mhz_rx_fsm_z. 04h = clk_48_6_mhz_fs_ls_rx_cdr_z. 05h = clk_120_12_1p5_mhz_rx_decoder_z. 06h = clk_10khz_power_on_fsm_z. 07h = clk_1khz_pll_clk_ready_timer_z. 08h = clk_extra_ref_0_z. 09h = clk_extra_ref_1_z. Other = N.A.	
06h (10390Dh)	**REG10390D**	**7:0**	**Default : 0x00**	**Access : R/W**
	UTMI_CKINV_EN_SEL[1:0]	7:6	UTMI 30MHz inverse clock enable generated by 120MHz. 00 = select phase 0. 01 = select phase 1. 10 = select phase 2. 11 = select phase 3. (Default is 1).	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	UTMI_CK_EN_SEL[1:0]	5:4	UTMI 30MHz clock enable generated by 120MHz. 00 = select phase 0. 01 = select phase 1. 10 = select phase 2. 11 = select phase 3. (Default is 3). (refer to UTMI_CKINV_EN_SEL offset is 2).	
	CLK_EXTRA1_DIV_SELECT[1:0]	3:2	Reserved.	
	CLK_EXTRA0_DIV_SELECT	1	Reserved.	
	DOUBLE_DATA_RATE	0	The control option for enable double data rate transfer.	
07h	**REG10390E**	**7:0**	**Default : 0x00**	**Access : RO**

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UTMI2 Register (Bank = 1039)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	UTMI_DIGITAL_STATUS[7:0]	7:0	UTMI digital part status report. 1. Status [0] : Error flag in elasticity buffer. 0 = normal. 1 = elasticity buffer error. 2. Status [1] : Sync pattern error detected status. 0 = normal. 1 = sync strip error. 3. Status [2] : EOP error detected status. 0 = normal. 1 = EOP error. 4. Status [3] :Bit-stuffer error status in Full/Low speed mode. 0 = normal. 1 = bit stuff error. 5. Status [4] : Underflow status in elasticity buffer. 0 = not underflow. 1 = underflow. 6. Status [5] : Overflow status in elasticity buffer. 0 = not overflow. 1 = overflow. 7. Status [6] : clock_ready. 8. Status [7] : UTMI interrupt status. 0 = no IRQ. 1 = IRQ active. 9. Status [8] : Enable Chirp function while UTMI as a device. 0 = normal. 1 = chirp. 10. Status [9] : Enable Chirp function while UTMI as a host. 0 = normal. 1 = chirp. 11. Status [10] : Disconnect status in host mode. 0 = connected.

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (10390Fh)	**REG10390F**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_DIGITAL_STATUS[15:8]	7:0	See description of '10390Eh'.	
08h (103910h)	**REG103910**	**7:0**	**Default : 0x00**	**Access : R/W**
	SE0_SET	7	Enable HS 45 ohm resistor on. 0 = Normal. 1 = Force 45 ohm resistor on.	
	UTMI_INT_CLR	6	Register control for high speed TX serializer enable in term resistor override mode. 1 = Enable. 0 = Disable.	
	FORCE_TX_NONBUSY	5	Force UTMI RX side always input tx_busy signal control. 0 = Normal. 1 = Force tx_busy is 0.	
	FORCE_RX_NONBUSY	4	Force UTMI TX side always input rx_busy signal control. 0 = Normal. 1 = Force rx_busy is 0.	
	TEST_BUS_SELECT[3:0]	3:0	UTMI test bus selection for debugging. 0000 = select test 0. 0001 = select test 1. 0010 = select test 2. ..... 1111 = select test 15. (refer to note 1).	
08h (103911h)	**REG103911**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_OVERRIDE	7	Enable HS tx controlled by regiseter. 0 = Normal. 1 = Enable override mode.	
	ERROR_FLAG_CLR	6	Write 1 & write 0 to clear error flag in digital status (address 7). 0: Disable. 1: Enable clear error flag.	
	PHY_MODE_ENABLE	5	Enable UTMI in Phy mode. 0 = Normal. 1 = set UTMI in/out ports from pad.	
	POWER_GOOD_RST	4	SW reset for power good signal. 0 = Normal. 1 = Software reset instead of powergood reset.	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_OVERRIDE	3	Enable FL tx controlled by regiseter. 0 = Normal. 1 = Enable override mode.	
	TX_SE0	2	Override FL tx send SE0. 0 = Disable SE0. 1 = Force tx sending SE0.	
	TX_EN	1	Override FL tx enable. 0 = Disable tx. 1 = Force tx enable.	
	TX_DATA	0	Override FL tx data. 0 = transmit 0. 1 = transmit 0.	
09h (103912h)	**REG103912**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DEGLITCH_ENZ	7	Register to enable deglitch module. 0 = Enable vdd2low deglitch function. 1 = Disable.	
	VDD2LOW_RST_ENZ	6	Register to enable reset signal of vdd2low. 0 = enable to output vdd2low_rst signal. 1 = Normal.	
	DEGLITCH_PRD[5:0]	5:0	Register to set vdd2low degitch period.	
09h (103913h)	**REG103913**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_P1	7	Enable Port-1 debug port.	
	IB_RTERM_TEST[2:0]	6:4	HS RTERM current test.	
	REG_TEST[2:0]	3:1	REG_TEST_p1: Regulator test (port 1 only).	
	USBSYN_RST	0	SW reset for UTMI digital synthesizer. 0 = Normal. 1 = Softeare reset digital synthesizer module in UTMI.	
0Ah (103914h)	**REG103914**	**7:0**	**Default : 0x0B**	**Access : R/W**
	XCVRSEL[1:0]	7:6	Override value to set XCVRSEL value(MAC to UTMI). 00 = high speed. 01 = full speed. 10 = low speed. 11 = N.A.	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPMODE[1:0]	5:4	Override value to set OPMODE value. (MAC to UTMI). 00 = mode 0. 01 = mode 1. 10 = mode 2. 11 = mode 3.	
	IDDIG	3	Override value to set IDDIG value.(UTMI to MAC). 0 = connected plug is a mini-A. 1 = connected plug is a mini-B.	
	SESSEND	2	Override value to set SESSEND value. (UTMI to MAC). 0 = Vbus > 0.8 V. 1 = Vbus < 0.2 V.	
	AVALID	1	Override value to set A-port value. (UTMI to MAC). 0 = Vbus < 0.8 V. 1 = Vbus > 2.0 V.	
	VBUSVALID	0	Override value to set VBUS VALID value. (UTMI to MAC). 0 = Vbus < 4.4 V. 1 = Vbus > 4.75 V.	
0Ah (103915h)	**REG103915**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_IEN_MASK_METHOD	7	Mask hs_tx_ien method.	
	HS_TX_IEN_MASK	6	Mask hs_tx_ien.	
	HOST_CHIRP_DET	5	HOST_CHIRP_DET.	
	USB_BOND_SET	4	Override value for option USB_BOND. 0 = Two port UTMI setting. 1 = One port UTMI setting.	
	USB_BOND_OVD	3	Override bonding option USB_BOND. 0 = Normal. 1 = bonding controlled by register.	
	SUSPENDM	2	Override value to control SUSPENDM. 0 = device in suspend mode. 1 = device in normal mode.	
	MACMODE_OVD	1	Override enable to control mac mode. 0 = Normal. 1 = Change Mac control signal from register.	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TERMSEL	0	Override value to set TERMSEL value. (MAC to UTMI). 0 = high speed. 1 = full/low speed.	
0Bh (103916h)	**REG103916**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[7:0]	7:0	Digital synthesizer clock frequency setting. MPLL clock divided by N.f setting. N = 5 bits. F = 27 bits.	
0Bh (103917h)	**REG103917**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[15:8]	7:0	See description of '103916h'.	
0Ch (103918h)	**REG103918**	**7:0**	**Default : 0xCC**	**Access : R/W**
	SYNTHESIZE_NF[23:16]	7:0	See description of '103916h'.	
0Ch (103919h)	**REG103919**	**7:0**	**Default : 0x23**	**Access : R/W**
	SYNTHESIZE_NF[31:24]	7:0	See description of '103916h'.	
10h	**REG103920**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI2 Register (Bank = 1039)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	PLL_TEST[7:0]	7:0	1. PLL_TEST[0]: PLL reference input clock selection (accompanied with PLL_TEST[0]). {PLL_TEST[26], PLL_TEST[0]}. 00 = Naked crystal input. 01 = Reserved+K98. 10 = Synthesized clock. 11 = Buffered crystal input. 2. PLL_TEST[2:1]: PLL loop divider selection. 00 = / 40. 01 = / 20. 10 = / 10. 11 = / (PLL_TEST[7:3]) / 2. 3. PLL_TEST[7:3]: PLL loop divider control from 3 to 65 (N+1). 000000 = / 65. 000001 = NA. 000010 = / 3. 000011 = / 4. .. 111111 = / 64. 4. PLL_TEST[9:8]: PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, source select. 00 = FBCK33. 01 = REFCK33. 10 = FBCK18. 11 = CLK480 to digital. 5. PLL_TEST[11:10]:PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, post-divider dividing ratio selection. 00 = /1. 01 = /2. 10 = /4. 11 = /8. 6. PLL_TEST[13:12]:CLK480 to digital output phase selection. 00 = A0. 01 = A90. 10 = A0B. 11 = A90B.

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (103921h)	**REG103921**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[15:8]	7:0	See description of '103920h'.	
11h (103922h)	**REG103922**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[23:16]	7:0	See description of '103920h'.	
11h (103923h)	**REG103923**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[31:24]	7:0	See description of '103920h'.	
12h (103924h)	**REG103924**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[39:32]	7:0	See description of '103920h'.	
13h (103926h)	**REG103926**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TED_TEST[7:0]	7:0	1. HS_TED_TEST[1:0] : De-glitch time setting for Squelch. 00 = 4 high-speed bit time. 01 = 6 high-speed bit time. 10 = 8 high-speed bit time. 11 = 2 high-speed bit time. 2. HS_TED_TEST[3:2] :Squelch detector input offset selection. 00 = 0mV. 01 = +12mV. 10 = -12mV. 11 = 0mV. 3. HS_TED_TEST[7:4] : Reserved.	
13h (103927h)	**REG103927**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PREAMP_TEST[7:0]	7:0	1. HS_PREAMP_TEST[1:0] : Reserved. 2. HS_PREAMP_TEST[3:2] : High-speed receiver bias current selection. 00 = 40u. 01 = 30u. 10 = 60u. 11 = 50u. 3. HS_PREAMP_TEST[7:4] : Reserved.	
14h	**REG103928**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI2 Register (Bank = 1039)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	FL_XCVR_TEST[7:0]	7:0	1. FL_XCVR_TEST[2:0] : Full/low-speed slew rate control capacitor fine tune. 000 = 1.2p. 001 = 1.3p. 010 = 1.4p. 011 = 1.5p. 100 = 0.8p. 101 = 0.9p. 110 = 1.0p. 111 = 1.1p. 2. FL_XCVR_TEST[5:3] : High-speed pull-down resistor fine tune. 000 = 100%. 001 = 97.5%. 010 = 97.5%. 011 = 95%. 100~111 = 80%. 3. FL_XCVR_TEST[7:6] :Full/low-speed pull down resistor fine tune. 00 = 19.35k. 01 = 17.3k. 10 = 21.45k. 11 = 19.35k. 4. FL_XCVR_TEST[9:8] : Full/low-speed pull down resistor fine tune. 00 = 1.2k. 01 = 1.3k. 10 = 1.17k. 11 = 1.19k. 5. FL_XCVR_TEST[10] : Full/low speed slew rate control current fine tune. 0 = current 1X. 1 = current 0.8X. 6. FL_XCVR_TEST[11] : Disable Full/low speed data re-timing by CLK120. 0 = Enabled. 1 = Disabled. 7.

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (103929h)	**REG103929**	**7:0**	**Default : 0x00**	**Access : R/W**
	FL_XCVR_TEST[15:8]	7:0	See description of '103928h'.	
15h	**REG10392A**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI2 Register (Bank = 1039)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	REF_TEST[7:0]	7:0	1. REF_TEST[1:0] : VSPOUT voltage control (for Squelch voltage threshold). 00 = 0.275V. 01 = 0.225V. 10 = 0.250V. 11 = 0.300V. 2. REF_TEST[3:2] : VSMOUT voltage control (for Squelch voltage threshold). 00 = 0.150V. 01 = 0.100V. 10 = 0.125V. 11 = 0.175V. 3. REF_TEST[5:4] : VCPOUT voltage control (for Disconnect voltage threshold). 00 = 0.70V. 01 = 0.60V. 10 = 0.65V. 11 = 0.75V. 4. REF_TEST[7:6] : VCMOUT voltage control (for Disconnect voltage threshold). 00 = 0.15V. 01 = 0.05V. 10 = 0.10V. 11 = 0.20V. 5. REF_TEST[9:8] : PGD comparator voltage threshold select (with hysteresis=100mV). 1.8V Threshold Vthh Vthl. 00 1.30V 1.20V. 01 1.25V 1.15V. 10 1.20V 1.10V. 11 1.15V 1.05V. 3.3V Threshold Vthh Vthl. 00 2.87V 2.63V. 01 2.74V 2.52V. 10 2.82V 2.58V. 11 2.71V 2.46V. 6. REF_TEST[10] : Enable Power-Good Detector to detect USB phy 3.3V power supply.

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (10392Bh)	**REG10392B**	**7:0**	**Default : 0x00**	**Access : R/W**
	REF_TEST[15:8]	7:0	See description of '10392Ah'.	
16h	**REG10392C**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI2 Register (Bank = 1039)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	HS_TX_TEST[7:0]	7:0	1. HS_TX_TEST[2:0] : Reserved. 2. HS_TX_TEST[3] :Enable high-speed TX test clock output (accompanied with HS_TX_TEST[28]). 0 = Disable. 1 = Enable. 3. HS_TX_TEST[6:4] : High-speed TX output current adjust. 000 = 100%. 001 = 101.6%. 010 = 103.3%. 011 = 105.0%. 100 = 93.3%. 101 = 95.0%. 110 = 96.7%. 111 = 98.3%. 4. HS_TX_TEST[8:7] : High-speed TX pre-emphasis adjust. 00 = 10.0%. 01 = 10.8%. 10 = 8.33%. 5. HS_TX_TEST[9] : Power-down High-speed TX pre-emphasis bias current. 0 = Enable. 1 = Power-down. 6. HS_TX_TEST[10] : Power-down high-speed TX current bias current. 0 = Enable. 1 = Power-down. 7. HS_TX_TEST[13:11] : HS_RTERM bias current adjust. 000 = 6/6. 001 = 7/6. 010 = 8/6. 011 = 9/6. 100 = 2/6. 101 = 3/6. 110 = 4/6. 111 = 5/6.

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (10392Dh)	**REG10392D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[15:8]	7:0	See description of '10392Ch'.	
17h (10392Eh)	**REG10392E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[23:16]	7:0	See description of '10392Ch'.	
17h (10392Fh)	**REG10392F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[31:24]	7:0	See description of '10392Ch'.	
18h (103930h)	**REG103930**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS[7:0]	7:0	Status report for utmi atop. Status[0] : UTMI pll lock status. Status[1] : UTMI pll flag. Status[2] : UTMI pll flag. Status[3] : UTMI pll clock test status. Status[4] : Power good status. Status[5] : Vbus voltage valid status. Status[6] : OTG session end status (VBUSLO for FS only PHY type). Status[7] : Pad CID status. Status[8] : AVALID_ATOP. Status[9] : HS_DISCONNECT. Status[10] : HS_RX_DATA[0]. Status[11] : HS_RX_CHIRP. Status[12] : FL_LINESTATE0. Status[13] : FL_LINESTATE1. Status[14] : loop back test failed. Status[15] : loop back test finish.	
18h (103931h)	**REG103931**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS[15:8]	7:0	See description of '103930h'.	
19h (103932h)	**REG103932**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_LENGTH[7:0]	7:0	TX data length for internal pattern gen. (0~255 bytes).	
19h (103933h)	**REG103933**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_RESERVED[4:0]	7:3	Reserved register. Bit <11>: test packet contineous mode for measuring eye. Diagram only. The compare result is invalid. Bit <12>: receiving test packet mode.	

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PG_TX_FIXED_DATA	2	Select fixed data to transmit. 0: Normal. 1: Enable to transmit random data.	
	PG_TX_MODE	1	Select "test packet" to transmit. 0: Normal. 1: Test packet data.	
	PG_TX_GO	0	Tx data enable to transmit for internal pattern gen.	
1Ah (103934h)	**REG103934**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[7:0]	7:0	Pattern Gen TX initial data setting.	
1Ah (103935h)	**REG103935**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[15:8]	7:0	See description of '103934h'.	
1Bh (103936h)	**REG103936**	**7:0**	**Default : 0x01**	**Access : R/W**
	PG_TX_INC[7:0]	7:0	Pattern Gen TX data incremental value setting.	
1Bh (103937h)	**REG103937**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_INC[15:8]	7:0	See description of '103936h'.	
1Ch (103938h)	**REG103938**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	ASRST_ON	7	Asynchronous reset for new FL module.	
	DM1_STATUS	6	Port 1 DM line status.	
	DP1_STATUS	5	Port 1 DP line status.	
	DM_STATUS	4	Port 0 DM line status.	
	DP_STATUS	3	Port 0 DP line status.	
	SELPORT	2	Port select for usb_xcvr switch. 0: Selected port0. 1: Selected port1.	
	VIGEN_PDN	1	VIGEN_PDN.	
	EN_CK_192	0	Enable usb_xcvr 192MHz clock out.	
1Ch (103939h)	**REG103939**	**7:0**	**Default : 0x28**	**Access : R/W**
	RESERVED2[7:0]	7:0	Reserved register 2. Bit <8>: VBUS select for dummy dual port (reg_selport_vbus). Bit <15:9> reserved.	
1Dh (10393Ah)	**REG10393A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_SERDES[7:0]	7:0	Test port for serializer and deserializer.	
1Dh	**REG10393B**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI2 Register (Bank = 1039)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10393Bh)	REG_TEST1[7:0]	7:0	Test register for 65nm process.	
1Eh (10393Ch)	**REG10393C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CA_DATA[3:0]	7:4	Calibration detail data.	
	-	3	Reserved.	
	POWER_GOOD_STS	2	ATOP powergood status.	
	CA_END	1	Calibration end (status).	
	CA_START	0	Calibration start.	
1Eh (10393Dh)	**REG10393D**	**7:0**	**Default : 0x00**	**Access : RO**
	CA_DATA[11:4]	7:0	See description of '10393Ch'.	

UTMI1 Register (Bank = 103A)

UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (103A00h)	**REG103A00**	**7:0**	**Default : 0x05**	**Access : R/W**
	R_DM_PDEN	7	Override value to Enable FS/LS DM pull-down resistor. 0 = normal. 1 = pull down.	
	R_DP_PDEN	6	Override value to Enable FS/LS DP pull-down resistor. 0 = normal. 1 = pull down.	
	R_PUMODE	5	Override DP/DM pull-up resistor value control. 0 = Pull-up resistor ~ 900~1575 ohm. 1 = Pull-up resistor ~ 1425~3090 ohm.	
	DM_PUEN	4	Override value to Enable FS/LS DM pull-up resistor. 0 = normal. 1 = pull up.	
	DP_PUEN	3	Override value to Enable FS/LS DP pull-up resistor. 0 = normal. 1 = pull up.	
	REF_PDN	2	Override value to Power-down USB_XCVR reference block. 0 = normal. 1 = power down.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TERM_OVERRIDE	1	Enable FS/LS termination override mode. 0 = Disable. 1 = Enable override mode.	
	PDN_OVERRIDE	0	Enable USB_XCVR power-down control override mode. 0 = Disable. 1 = Enable override mode.	
00h (103A01h)	**REG103A01**	**7:0**	**Default : 0xFF**	**Access : R/W**
	REG_PDN	7	Override value to Power-down USB_XCVR build-in regulator block. 0 = normal. 1 = power down.	
	IREF_PDN	6	Override value to Power-down USB_XCVR HS current reference block. 0 = normal. 1 = power down.	
	VBUSDET_PDN	5	Override value to Power-down USB_XCVR VBUS detector block. 0 = normal. 1 = power down.	
	FL_XCVR_PDN	4	Override value to Power-down USB_XCVR FS/LS transceiver block. 0 = normal. 1 = power down.	
	HS_PREAMP_PDN	3	Override value to Power-down USB_XCVR HS pre-amplifier block. 0 = normal. 1 = power down.	
	HS_TED_PDN	2	Override value to Power-down USB_XCVR HS TED block. (squelch circuit). 0 = normal. 1 = power down.	
	PLL_PDN	1	Override value to Power-down USB_XCVR PLL block. 0 = normal. 1 = power down.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HS_DM_PDN	0	Override value to Power-down USB_XCVR HS de-serializer block. 0 = normal. 1 = power down.	
01h (103A02h)	**REG103A02**	**7:0**	**Default : 0x80**	**Access : R/W**
	BOND_SEL	7	Select internal regulator. 0 = Use external regulator. 1 = Use internal regulator.	
	HS_TX_TEN	6	Force enable HS_TX analog Parallel-to-Serial function.(No use). 0 = Normal. 1 = force enable current source.	
	FL_LOWIMODE	5	Full/Low speed receiver power saving mode. 0 = Normal. 1 = Enable Low current mode.	
	BITSTUFF_EN	4	Override value to control Bit-Stuff mode. 0 = Force Bit-Stuff disable. 1 = Force Bit-Stuff enable.	
	NRZI_EN	3	Override value to control NRZI mode. 0 = Force NRZI disable. 1 = Force NRZI enable.	
	CLK12_SEL	2	PLL 12MHz reference clock source select. 0 = From XTAL_IN.(12Mhz). 1 = From digital synthesizer.(48Mhz-N.f).	
	FSLS_SEL	1	Override value to select Full/Low speed USB_XCVR. 0 = Full speed mode. 1 = Low speed mode.	
	SEL_OVERRIDE	0	Source select and enable override control. (No use).	
01h (103A03h)	**REG103A03**	**7:0**	**Default : 0x90**	**Access : R/W**
	HS_RTERM_PDN	7	Power down option of high speed terminal resistor.	
	LINESTATE_SEL	6	Line state mode report selection in HS mode. 0 = Normal. 1 = select RX_CHIRP as line state.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EOP40_DET_DELAY_CNT[2:0]	5:3	HS EOP_40 window delay for disconnect detection. (1T = 1/120 MHz). 00 = no delay. 01 = delay 1T. 10 = delay 2T. 11 = delay 3T. (Default value is 2).	
	FL_SEL_OVERRIDE	2	Full/Low speed mode select override value. 0 = Normal. 1 = Controlled by register fs_ls_sel (bit-1).	
	NRZI_OVERRIDE	1	NRZI enable controlled by register. 0 = Normal. 1 = Controlled by nrzi_en (bit-3).	
	BITSTUFF_OVERRIDE	0	Bit-stuff enable controlled by register. 0 = Normal. 1 = Controlled by bitstuff_en (bit-4).	
02h (103A04h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (103A05h)	**REG103A05**	**7:0**	**Default : 0x30**	**Access : R/W**
	UTMI_TX_WAIT_CNT[3:0]	7:4	TX HS delay for min inter-packet 32 bit-time wait state. (1T = 1/120 MHz). 000 = zero wait state. 001 = 1T. .... 101 = 6T. 111 = 7T. (Default is 3).	
	TX_OUT_SEL_MULTI_PHASE[1:0]	3:2	UTMI TX OUT multi cycle phase selection. 00 = phase 0. 01 = phase 1. 10 = phase 2. 11 = phase 3.	
	TX_IN_SEL_MULTI_PHASE[1:0]	1:0	UTMI TX IN Multi cycle phase selection. 00 = phase 0. 01 = phase 1. 10 = phase 2. 11 = phase 3.	
03h	**REG103A06**	**7:0**	**Default : 0x20**	**Access : R/W**

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103A06h)	OTG_DUAL_ROLE	7	Enable OTG dual role mode. 0 = Register control. 1 = Normal function.(OTG mode).	
	HS_STAGE_SELECT[1:0]	6:5	RX HS data recovery reference stage control. 00 = 1 stage. 01 = 2 stage. 00 = 3 stage. 01 = 4 stage. (Default is 1).	
	TX_FL_LATENCY_DELAY_1	4	TX in Full/Low speed mode delay 1 DFF. 0 = normal (combinational out to analog). 1 = Enable (DFF out to analog).	
	TX_FL_EARLY_4	3	TX in fl mode 4 to 1 fifo bypass 1 DFF.(no use). 0 = Disable. 1 = Enable.	
	TX_FORCE_HS_CURRENT_ENABLE	2	Force HS TX current source enable. 0 = Normal. 1 = Force current source.	
	UTMI_TX_SW_RESET	1	UTMI TX software reset. 0 = Normal. 1 = Enable software reset.	
	RX_SWRESET	0	UTMI RX software reset. 0 = Normal. 1 = Enable software reset.	
03h (103A07h)	**REG103A07**	**7:0**	**Default : 0x30**	**Access : R/W**
	VBUSDET_TEST[1:0]	7:6	VBUS_VALID LEVEL SELECT (the effect of 5k load resistor is including). 00: 4.35V. 01: 4.13V. 10: 3.92V. 11: 4.56V.	
	TX_RESERVED[3:0]	5:2	[1:0] = clock_switch_sel (Default is 2'b00). [2] = cid_over_dis (Default is 1). [3] = vbus_over_dis (Default is 1).	
	CDR_MODE_SEL	1	RX HS data recovery voting mode select. 0 = old cdr mode. 1 = new cdr mode select to collect more RX edge information.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_RESET_FSM	0	Synchronous TX FSM software reset. 0 = Disable. 1 = reset TX internal FSM engine.	
04h (103A08h)	**REG103A08**	**7:0**	**Default : 0x83**	**Access : R/W**
	CLK_EXTRA_0_EN	7	pd_bg_current: Power down bandgap current.	
	CLKTEST_EN	6	Test mode enable including: UPLL reset control.	
	-	5:2	Reserved.	
	UTMI_CLK120_EN	1	Override value to enable UTMI 120M clock source. 0 = stop. 1 = Enable.	
	UTMI_CLK_EN	0	Override value to enable UTMI 30MHz and 60MHz clock source. 0 = stop. 1 = Enable.	
04h (103A09h)	**REG103A09**	**7:0**	**Default : 0x04**	**Access : R/W**
	HS_RX_ROBOUST_EN	7	Enable High speed Rx roboust feature.	
	-	6	Reserved.	
	CLK_274_EN	5	Enable 274MHz clock output.	
	CLK214_SYN_EN	4	Enable clock synthesizer.	
	FORCE_PLL_ON	3	Override enable to enable utmi pll by register. 0 = Normal. 1 = Force utmi pll always on.	
	CLK_CTL_OVERRIDE	2	Override enable to enable clock source by register. 0 = Normal. 1 = Force clock enable by register setting.	
	XTAL12_EN	1	Register to select the source of clk_uhc. 0 = 30MHz for UPLL. 1 = crystal clock.	
	CLK_EXTRA_1_EN	0	reg_all_pass: Enable ISI improvement.	
05h (103A0Ah)	**REG103A0A**	**7:0**	**Default : 0x40**	**Access : R/W**
	CLK_EXTRA_0_INV	7	Reserved.	
	CLKTEST_INV	6	Register control for UPLL divider reset (low active). 0 = Reset. 1 = Normal.	
	-	5:2	Reserved.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	UTMI_CLK120_INV	1	Inverse 120MHz clock source. 0 = Normal. 1 = Inverse clock.	
	UTMI_CLK_INV	0	Inverse 30MHz and 60MHz clock source. 0 = Normal. 1 = Inverse clock.	
05h (103A0Bh)	**REG103A0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CK_INV_RESERVED[6:0]	7:1	Reserved register. Bit <11:9>: HS_TX_CKI select. Bit <12>: enable old HS disconnect sampling mechanism. Bit <13> enable DP/DM swap mechanism. Bit <14>: disable drive port reset (for FL tranceiver only). Bit <15>: select the latch on HS data transfer interface.	
	CLK_EXTRA_1_INV	0	Inverse clock extra1. 0 = Normal. 1 = Inverse clock.	
06h (103A0Ch)	**REG103A0C**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAC_CLK_SEL[1:0]	7:6	MAC clock selection. Bit <6>: set to 1 represent dynamic switched clock for MAC. Set to 0 is the old FIFO access mechanism for MAC. Bit <7>: reserved.	
	TEST_CLOCK_SELECT[5:0]	5:0	UTMI test clock selection. 00h = clk_120mhz_utmi_z. 01h = clk_30mhz_utmi_z. 02h = clk_120_12_1p5_mhz_tx_fsm_z. 03h = clk_120_48_6_mhz_rx_fsm_z. 04h = clk_48_6_mhz_fs_ls_rx_cdr_z. 05h = clk_120_12_1p5_mhz_rx_decoder_z. 06h = clk_10khz_power_on_fsm_z. 07h = clk_1khz_pll_clk_ready_timer_z. 08h = clk_extra_ref_0_z. 09h = clk_extra_ref_1_z. Other = N.A.	
06h	**REG103A0D**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103A0Dh)	UTMI_CKINV_EN_SEL[1:0]	7:6	UTMI 30MHz inverse clock enable generated by 120MHz. 00 = select phase 0. 01 = select phase 1. 10 = select phase 2. 11 = select phase 3. (Default is 1).	
	UTMI_CK_EN_SEL[1:0]	5:4	UTMI 30MHz clock enable generated by 120MHz. 00 = select phase 0. 01 = select phase 1. 10 = select phase 2. 11 = select phase 3. (Default is 3). (refer to UTMI_CKINV_EN_SEL offset is 2).	
	CLK_EXTRA1_DIV_SELECT[1:0]	3:2	Reserved.	
	CLK_EXTRA0_DIV_SELECT	1	Reserved.	
	DOUBLE_DATA_RATE	0	The control option for enable double data rate transfer.	
07h	**REG103A0E**	**7:0**	**Default : 0x00**	**Access : RO**

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UTMI1 Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	UTMI_DIGITAL_STATUS[7:0]	7:0	UTMI digital part status report. 1. Status [0] : Error flag in elasticity buffer. 0 = normal. 1 = elasticity buffer error. 2. Status [1] : Sync pattern error detected status. 0 = normal. 1 = sync strip error. 3. Status [2] : EOP error detected status. 0 = normal. 1 = EOP error. 4. Status [3] :Bit-stuffer error status in Full/Low speed mode. 0 = normal. 1 = bit stuff error. 5. Status [4] : Underflow status in elasticity buffer. 0 = not underflow. 1 = underflow. 6. Status [5] : Overflow status in elasticity buffer. 0 = not overflow. 1 = overflow. 7. Status [6] : clock_ready. 8. Status [7] : UTMI interrupt status. 0 = no IRQ. 1 = IRQ active. 9. Status [8] : Enable Chirp function while UTMI as a device. 0 = normal. 1 = chirp. 10. Status [9] : Enable Chirp function while UTMI as a host. 0 = normal. 1 = chirp. 11. Status [10] : Disconnect status in host mode. 0 = connected.

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (103A0Fh)	**REG103A0F**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_DIGITAL_STATUS[15:8]	7:0	See description of '103A0Eh'.	
08h (103A10h)	**REG103A10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SE0_SET	7	Enable HS 45 ohm resistor on. 0 = Normal. 1 = Force 45 ohm resistor on.	
	UTMI_INT_CLR	6	Register control for high speed TX serializer enable in term resistor override mode. 1 = Enable. 0 = Disable.	
	FORCE_TX_NONBUSY	5	Force UTMI RX side always input tx_busy signal control. 0 = Normal. 1 = Force tx_busy is 0.	
	FORCE_RX_NONBUSY	4	Force UTMI TX side always input rx_busy signal control. 0 = Normal. 1 = Force rx_busy is 0.	
	TEST_BUS_SELECT[3:0]	3:0	UTMI test bus selection for debugging. 0000 = select test 0. 0001 = select test 1. 0010 = select test 2. ..... 1111 = select test 15. (refer to note 1).	
08h (103A11h)	**REG103A11**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_OVERRIDE	7	Enable HS tx controlled by regiseter. 0 = Normal. 1 = Enable override mode.	
	ERROR_FLAG_CLR	6	Write 1 & write 0 to clear error flag in digital status (address 7). 0: Disable. 1: Enable clear error flag.	
	PHY_MODE_ENABLE	5	Enable UTMI in Phy mode. 0 = Normal. 1 = set UTMI in/out ports from pad.	
	POWER_GOOD_RST	4	SW reset for power good signal. 0 = Normal. 1 = Software reset instead of powergood reset.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_OVERRIDE	3	Enable FL tx controlled by regiseter. 0 = Normal. 1 = Enable override mode.	
	TX_SE0	2	Override FL tx send SE0. 0 = Disable SE0. 1 = Force tx sending SE0.	
	TX_EN	1	Override FL tx enable. 0 = Disable tx. 1 = Force tx enable.	
	TX_DATA	0	Override FL tx data. 0 = transmit 0. 1 = transmit 0.	
09h (103A12h)	**REG103A12**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DEGLITCH_ENZ	7	Register to enable deglitch module. 0 = Enable vdd2low deglitch function. 1 = Disable.	
	VDD2LOW_RST_ENZ	6	Register to enable reset signal of vdd2low. 0 = enable to output vdd2low_rst signal. 1 = Normal.	
	DEGLITCH_PRD[5:0]	5:0	Register to set vdd2low degitch period.	
09h (103A13h)	**REG103A13**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_P1	7	Enable Port-1 debug port.	
	IB_RTERM_TEST[2:0]	6:4	HS RTERM current test.	
	REG_TEST[2:0]	3:1	REG_TEST_p1: Regulator test (port 1 only).	
	USBSYN_RST	0	SW reset for UTMI digital synthesizer. 0 = Normal. 1 = Softeare reset digital synthesizer module in UTMI.	
0Ah (103A14h)	**REG103A14**	**7:0**	**Default : 0x0B**	**Access : R/W**
	XCVRSEL[1:0]	7:6	Override value to set XCVRSEL value(MAC to UTMI). 00 = high speed. 01 = full speed. 10 = low speed. 11 = N.A.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPMODE[1:0]	5:4	Override value to set OPMODE value. (MAC to UTMI). 00 = mode 0. 01 = mode 1. 10 = mode 2. 11 = mode 3.	
	IDDIG	3	Override value to set IDDIG value.(UTMI to MAC). 0 = connected plug is a mini-A. 1 = connected plug is a mini-B.	
	SESSEND	2	Override value to set SESSEND value. (UTMI to MAC). 0 = Vbus > 0.8 V. 1 = Vbus < 0.2 V.	
	AVALID	1	Override value to set A-port value. (UTMI to MAC). 0 = Vbus < 0.8 V. 1 = Vbus > 2.0 V.	
	VBUSVALID	0	Override value to set VBUS VALID value. (UTMI to MAC). 0 = Vbus < 4.4 V. 1 = Vbus > 4.75 V.	
0Ah (103A15h)	**REG103A15**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_IEN_MASK_METHOD	7	Mask hs_tx_ien method.	
	HS_TX_IEN_MASK	6	Mask hs_tx_ien.	
	HOST_CHIRP_DET	5	HOST_CHIRP_DET.	
	USB_BOND_SET	4	Override value for option USB_BOND. 0 = Two port UTMI setting. 1 = One port UTMI setting.	
	USB_BOND_OVD	3	Override bonding option USB_BOND. 0 = Normal. 1 = bonding controlled by register.	
	SUSPENDM	2	Override value to control SUSPENDM. 0 = device in suspend mode. 1 = device in normal mode.	
	MACMODE_OVD	1	Override enable to control mac mode. 0 = Normal. 1 = Change Mac control signal from register.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TERMSEL	0	Override value to set TERMSEL value. (MAC to UTMI). 0 = high speed. 1 = full/low speed.	
0Bh (103A16h)	**REG103A16**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[7:0]	7:0	Digital synthesizer clock frequency setting. MPLL clock divided by N.f setting. N = 5 bits. F = 27 bits.	
0Bh (103A17h)	**REG103A17**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[15:8]	7:0	See description of '103A16h'.	
0Ch (103A18h)	**REG103A18**	**7:0**	**Default : 0xCC**	**Access : R/W**
	SYNTHESIZE_NF[23:16]	7:0	See description of '103A16h'.	
0Ch (103A19h)	**REG103A19**	**7:0**	**Default : 0x23**	**Access : R/W**
	SYNTHESIZE_NF[31:24]	7:0	See description of '103A16h'.	
10h	**REG103A20**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI1 Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	PLL_TEST[7:0]	7:0	1. PLL_TEST[0]: PLL reference input clock selection (accompanied with PLL_TEST[0]). {PLL_TEST[26], PLL_TEST[0]}. 00 = Naked crystal input. 01 = Reserved+K98. 10 = Synthesized clock. 11 = Buffered crystal input. 2. PLL_TEST[2:1]: PLL loop divider selection. 00 = / 40. 01 = / 20. 10 = / 10. 11 = / (PLL_TEST[7:3]) / 2. 3. PLL_TEST[7:3]: PLL loop divider control from 3 to 65 (N+1). 000000 = / 65. 000001 = NA. 000010 = / 3. 000011 = / 4. .. 111111 = / 64. 4. PLL_TEST[9:8]: PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, source select. 00 = FBCK33. 01 = REFCK33. 10 = FBCK18. 11 = CLK480 to digital. 5. PLL_TEST[11:10]:PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, post-divider dividing ratio selection. 00 = /1. 01 = /2. 10 = /4. 11 = /8. 6. PLL_TEST[13:12]:CLK480 to digital output phase selection. 00 = A0. 01 = A90. 10 = A0B. 11 = A90B.

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (103A21h)	**REG103A21**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[15:8]	7:0	See description of '103A20h'.	
11h (103A22h)	**REG103A22**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[23:16]	7:0	See description of '103A20h'.	
11h (103A23h)	**REG103A23**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[31:24]	7:0	See description of '103A20h'.	
12h (103A24h)	**REG103A24**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[39:32]	7:0	See description of '103A20h'.	
13h (103A26h)	**REG103A26**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TED_TEST[7:0]	7:0	1. HS_TED_TEST[1:0] : De-glitch time setting for Squelch. 00 = 4 high-speed bit time. 01 = 6 high-speed bit time. 10 = 8 high-speed bit time. 11 = 2 high-speed bit time. 2. HS_TED_TEST[3:2] :Squelch detector input offset selection. 00 = 0mV. 01 = +12mV. 10 = -12mV. 11 = 0mV. 3. HS_TED_TEST[7:4] : Reserved.	
13h (103A27h)	**REG103A27**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PREAMP_TEST[7:0]	7:0	1. HS_PREAMP_TEST[1:0] : Reserved. 2. HS_PREAMP_TEST[3:2] : High-speed receiver bias current selection. 00 = 40u. 01 = 30u. 10 = 60u. 11 = 50u. 3. HS_PREAMP_TEST[7:4] : Reserved.	
14h	**REG103A28**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI1 Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	FL_XCVR_TEST[7:0]	7:0	1. FL_XCVR_TEST[2:0] : Full/low-speed slew rate control capacitor fine tune. 000 = 1.2p. 001 = 1.3p. 010 = 1.4p. 011 = 1.5p. 100 = 0.8p. 101 = 0.9p. 110 = 1.0p. 111 = 1.1p. 2. FL_XCVR_TEST[5:3] : High-speed pull-down resistor fine tune. 000 = 100%. 001 = 97.5%. 010 = 97.5%. 011 = 95%. 100~111 = 80%. 3. FL_XCVR_TEST[7:6] :Full/low-speed pull down resistor fine tune. 00 = 19.35k. 01 = 17.3k. 10 = 21.45k. 11 = 19.35k. 4. FL_XCVR_TEST[9:8] : Full/low-speed pull down resistor fine tune. 00 = 1.2k. 01 = 1.3k. 10 = 1.17k. 11 = 1.19k. 5. FL_XCVR_TEST[10] : Full/low speed slew rate control current fine tune. 0 = current 1X. 1 = current 0.8X. 6. FL_XCVR_TEST[11] : Disable Full/low speed data re-timing by CLK120. 0 = Enabled. 1 = Disabled. 7.

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (103A29h)	**REG103A29**	**7:0**	**Default : 0x00**	**Access : R/W**
	FL_XCVR_TEST[15:8]	7:0	See description of '103A28h'.	
15h	**REG103A2A**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI1 Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	REF_TEST[7:0]	7:0	1. REF_TEST[1:0] : VSPOUT voltage control (for Squelch voltage threshold). 00 = 0.275V. 01 = 0.225V. 10 = 0.250V. 11 = 0.300V. 2. REF_TEST[3:2] : VSMOUT voltage control (for Squelch voltage threshold). 00 = 0.150V. 01 = 0.100V. 10 = 0.125V. 11 = 0.175V. 3. REF_TEST[5:4] : VCPOUT voltage control (for Disconnect voltage threshold). 00 = 0.70V. 01 = 0.60V. 10 = 0.65V. 11 = 0.75V. 4. REF_TEST[7:6] : VCMOUT voltage control (for Disconnect voltage threshold). 00 = 0.15V. 01 = 0.05V. 10 = 0.10V. 11 = 0.20V. 5. REF_TEST[9:8] : PGD comparator voltage threshold select (with hysteresis=100mV). 1.8V Threshold Vthh Vthl. 00 1.30V 1.20V. 01 1.25V 1.15V. 10 1.20V 1.10V. 11 1.15V 1.05V. 3.3V Threshold Vthh Vthl. 00 2.87V 2.63V. 01 2.74V 2.52V. 10 2.82V 2.58V. 11 2.71V 2.46V. 6. REF_TEST[10] : Enable Power-Good Detector to detect USB phy 3.3V power supply.

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (103A2Bh)	**REG103A2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	REF_TEST[15:8]	7:0	See description of '103A2Ah'.	
16h	**REG103A2C**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI1 Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	HS_TX_TEST[7:0]	7:0	1. HS_TX_TEST[2:0] : Reserved. 2. HS_TX_TEST[3] :Enable high-speed TX test clock output (accompanied with HS_TX_TEST[28]). 0 = Disable. 1 = Enable. 3. HS_TX_TEST[6:4] : High-speed TX output current adjust. 000 = 100%. 001 = 101.6%. 010 = 103.3%. 011 = 105.0%. 100 = 93.3%. 101 = 95.0%. 110 = 96.7%. 111 = 98.3%. 4. HS_TX_TEST[8:7] : High-speed TX pre-emphasis adjust. 00 = 10.0%. 01 = 10.8%. 10 = 8.33%. 5. HS_TX_TEST[9] : Power-down High-speed TX pre-emphasis bias current. 0 = Enable. 1 = Power-down. 6. HS_TX_TEST[10] : Power-down high-speed TX current bias current. 0 = Enable. 1 = Power-down. 7. HS_TX_TEST[13:11] : HS_RTERM bias current adjust. 000 = 6/6. 001 = 7/6. 010 = 8/6. 011 = 9/6. 100 = 2/6. 101 = 3/6. 110 = 4/6. 111 = 5/6.

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (103A2Dh)	**REG103A2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[15:8]	7:0	See description of '103A2Ch'.	
17h (103A2Eh)	**REG103A2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[23:16]	7:0	See description of '103A2Ch'.	
17h (103A2Fh)	**REG103A2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[31:24]	7:0	See description of '103A2Ch'.	
18h (103A30h)	**REG103A30**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS[7:0]	7:0	Status report for utmi atop. Status[0] : UTMI pll lock status. Status[1] : UTMI pll flag. Status[2] : UTMI pll flag. Status[3] : UTMI pll clock test status. Status[4] : Power good status. Status[5] : Vbus voltage valid status. Status[6] : OTG session end status (VBUSLO for FS only PHY type). Status[7] : Pad CID status. Status[8] : AVALID_ATOP. Status[9] : HS_DISCONNECT. Status[10] : HS_RX_DATA[0]. Status[11] : HS_RX_CHIRP. Status[12] : FL_LINESTATE0. Status[13] : FL_LINESTATE1. Status[14] : loop back test failed. Status[15] : loop back test finish.	
18h (103A31h)	**REG103A31**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS[15:8]	7:0	See description of '103A30h'.	
19h (103A32h)	**REG103A32**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_LENGTH[7:0]	7:0	TX data length for internal pattern gen. (0~255 bytes).	
19h (103A33h)	**REG103A33**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_RESERVED[4:0]	7:3	Reserved register. Bit <11>: test packet contineous mode for measuring eye. Diagram only. The compare result is invalid. Bit <12>: receiving test packet mode.	

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PG_TX_FIXED_DATA	2	Select fixed data to transmit. 0: Normal. 1: Enable to transmit random data.	
	PG_TX_MODE	1	Select "test packet" to transmit. 0: Normal. 1: Test packet data.	
	PG_TX_GO	0	Tx data enable to transmit for internal pattern gen.	
1Ah (103A34h)	**REG103A34**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[7:0]	7:0	Pattern Gen TX initial data setting.	
1Ah (103A35h)	**REG103A35**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[15:8]	7:0	See description of '103A34h'.	
1Bh (103A36h)	**REG103A36**	**7:0**	**Default : 0x01**	**Access : R/W**
	PG_TX_INC[7:0]	7:0	Pattern Gen TX data incremental value setting.	
1Bh (103A37h)	**REG103A37**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_INC[15:8]	7:0	See description of '103A36h'.	
1Ch (103A38h)	**REG103A38**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	ASRST_ON	7	Asynchronous reset for new FL module.	
	DM1_STATUS	6	Port 1 DM line status.	
	DP1_STATUS	5	Port 1 DP line status.	
	DM_STATUS	4	Port 0 DM line status.	
	DP_STATUS	3	Port 0 DP line status.	
	SELPORT	2	Port select for usb_xcvr switch. 0: Selected port0. 1: Selected port1.	
	VIGEN_PDN	1	VIGEN_PDN.	
	EN_CK_192	0	Enable usb_xcvr 192MHz clock out.	
1Ch (103A39h)	**REG103A39**	**7:0**	**Default : 0x28**	**Access : R/W**
	RESERVED2[7:0]	7:0	Reserved register 2. Bit <8>: VBUS select for dummy dual port (reg_selport_vbus). Bit <15:9> reserved.	
1Dh (103A3Ah)	**REG103A3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_SERDES[7:0]	7:0	Test port for serializer and deserializer.	
1Dh	**REG103A3B**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI1 Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103A3Bh)	REG_TEST1[7:0]	7:0	Test register for 65nm process.	
1Eh (103A3Ch)	**REG103A3C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CA_DATA[3:0]	7:4	Calibration detail data.	
	-	3	Reserved.	
	POWER_GOOD_STS	2	ATOP powergood status.	
	CA_END	1	Calibration end (status).	
	CA_START	0	Calibration start.	
1Eh (103A3Dh)	**REG103A3D**	**7:0**	**Default : 0x00**	**Access : RO**
	CA_DATA[11:4]	7:0	See description of '103A3Ch'.	

UTMI Register (Bank = 103A)

UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (103A80h)	**REG103A80**	**7:0**	**Default : 0x05**	**Access : R/W**
	R_DM_PDEN	7	Override value to Enable FS/LS DM pull-down resistor. 0 = normal. 1 = pull down.	
	R_DP_PDEN	6	Override value to Enable FS/LS DP pull-down resistor. 0 = normal. 1 = pull down.	
	R_PUMODE	5	Override DP/DM pull-up resistor value control. 0 = Pull-up resistor ~ 900~1575 ohm. 1 = Pull-up resistor ~ 1425~3090 ohm.	
	DM_PUEN	4	Override value to Enable FS/LS DM pull-up resistor. 0 = normal. 1 = pull up.	
	DP_PUEN	3	Override value to Enable FS/LS DP pull-up resistor. 0 = normal. 1 = pull up.	
	REF_PDN	2	Override value to Power-down USB_XCVR reference block. 0 = normal. 1 = power down.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TERM_OVERRIDE	1	Enable FS/LS termination override mode. 0 = Disable. 1 = Enable override mode.	
	PDN_OVERRIDE	0	Enable USB_XCVR power-down control override mode. 0 = Disable. 1 = Enable override mode.	
40h (103A81h)	**REG103A81**	**7:0**	**Default : 0xFF**	**Access : R/W**
	REG_PDN	7	Override value to Power-down USB_XCVR build-in regulator block. 0 = normal. 1 = power down.	
	IREF_PDN	6	Override value to Power-down USB_XCVR HS current reference block. 0 = normal. 1 = power down.	
	VBUSDET_PDN	5	Override value to Power-down USB_XCVR VBUS detector block. 0 = normal. 1 = power down.	
	FL_XCVR_PDN	4	Override value to Power-down USB_XCVR FS/LS transceiver block. 0 = normal. 1 = power down.	
	HS_PREAMP_PDN	3	Override value to Power-down USB_XCVR HS pre-amplifier block. 0 = normal. 1 = power down.	
	HS_TED_PDN	2	Override value to Power-down USB_XCVR HS TED block. (squelch circuit). 0 = normal. 1 = power down.	
	PLL_PDN	1	Override value to Power-down USB_XCVR PLL block. 0 = normal. 1 = power down.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HS_DM_PDN	0	Override value to Power-down USB_XCVR HS de-serializer block. 0 = normal. 1 = power down.	
41h (103A82h)	**REG103A82**	**7:0**	**Default : 0x80**	**Access : R/W**
	BOND_SEL	7	Select internal regulator. 0 = Use external regulator. 1 = Use internal regulator.	
	HS_TX_TEN	6	Force enable HS_TX analog Parallel-to-Serial function.(No use). 0 = Normal. 1 = force enable current source.	
	FL_LOWIMODE	5	Full/Low speed receiver power saving mode. 0 = Normal. 1 = Enable Low current mode.	
	BITSTUFF_EN	4	Override value to control Bit-Stuff mode. 0 = Force Bit-Stuff disable. 1 = Force Bit-Stuff enable.	
	NRZI_EN	3	Override value to control NRZI mode. 0 = Force NRZI disable. 1 = Force NRZI enable.	
	CLK12_SEL	2	PLL 12MHz reference clock source select. 0 = From XTAL_IN.(12Mhz). 1 = From digital synthesizer.(48Mhz-N.f).	
	FSLS_SEL	1	Override value to select Full/Low speed USB_XCVR. 0 = Full speed mode. 1 = Low speed mode.	
	SEL_OVERRIDE	0	Source select and enable override control. (No use).	
41h (103A83h)	**REG103A83**	**7:0**	**Default : 0x90**	**Access : R/W**
	HS_RTERM_PDN	7	Power down option of high speed terminal resistor.	
	LINESTATE_SEL	6	Line state mode report selection in HS mode. 0 = Normal. 1 = select RX_CHIRP as line state.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EOP40_DET_DELAY_CNT[2:0]	5:3	HS EOP_40 window delay for disconnect detection. (1T = 1/120 MHz). 00 = no delay. 01 = delay 1T. 10 = delay 2T. 11 = delay 3T. (Default value is 2).	
	FL_SEL_OVERRIDE	2	Full/Low speed mode select override value. 0 = Normal. 1 = Controlled by register fs_ls_sel (bit-1).	
	NRZI_OVERRIDE	1	NRZI enable controlled by register. 0 = Normal. 1 = Controlled by nrzi_en (bit-3).	
	BITSTUFF_OVERRIDE	0	Bit-stuff enable controlled by register. 0 = Normal. 1 = Controlled by bitstuff_en (bit-4).	
42h (103A84h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
42h (103A85h)	**REG103A85**	**7:0**	**Default : 0x30**	**Access : R/W**
	UTMI_TX_WAIT_CNT[3:0]	7:4	TX HS delay for min inter-packet 32 bit-time wait state. (1T = 1/120 MHz). 000 = zero wait state. 001 = 1T. .... 101 = 6T. 111 = 7T. (Default is 3).	
	TX_OUT_SEL_MULTI_PHASE[1:0]	3:2	UTMI TX OUT multi cycle phase selection. 00 = phase 0. 01 = phase 1. 10 = phase 2. 11 = phase 3.	
	TX_IN_SEL_MULTI_PHASE[1:0]	1:0	UTMI TX IN Multi cycle phase selection. 00 = phase 0. 01 = phase 1. 10 = phase 2. 11 = phase 3.	
43h	**REG103A86**	**7:0**	**Default : 0x20**	**Access : R/W**

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103A86h)	OTG_DUAL_ROLE	7	Enable OTG dual role mode. 0 = Register control. 1 = Normal function.(OTG mode).	
	HS_STAGE_SELECT[1:0]	6:5	RX HS data recovery reference stage control. 00 = 1 stage. 01 = 2 stage. 00 = 3 stage. 01 = 4 stage. (Default is 1).	
	TX_FL_LATENCY_DELAY_1	4	TX in Full/Low speed mode delay 1 DFF. 0 = normal (combinational out to analog). 1 = Enable (DFF out to analog).	
	TX_FL_EARLY_4	3	TX in fl mode 4 to 1 fifo bypass 1 DFF.(no use). 0 = Disable. 1 = Enable.	
	TX_FORCE_HS_CURRENT_ENABLE	2	Force HS TX current source enable. 0 = Normal. 1 = Force current source.	
	UTMI_TX_SW_RESET	1	UTMI TX software reset. 0 = Normal. 1 = Enable software reset.	
	RX_SWRESET	0	UTMI RX software reset. 0 = Normal. 1 = Enable software reset.	
43h (103A87h)	**REG103A87**	**7:0**	**Default : 0x30**	**Access : R/W**
	VBUSDET_TEST[1:0]	7:6	VBUS_VALID LEVEL SELECT (the effect of 5k load resistor is including). 00: 4.35V. 01: 4.13V. 10: 3.92V. 11: 4.56V.	
	TX_RESERVED[3:0]	5:2	[1:0] = clock_switch_sel (Default is 2'b00). [2] = cid_over_dis (Default is 1). [3] = vbus_over_dis (Default is 1).	
	CDR_MODE_SEL	1	RX HS data recovery voting mode select. 0 = old cdr mode. 1 = new cdr mode select to collect more RX edge information.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_RESET_FSM	0	Synchronous TX FSM software reset. 0 = Disable. 1 = reset TX internal FSM engine.	
44h (103A88h)	**REG103A88**	**7:0**	**Default : 0x83**	**Access : R/W**
	CLK_EXTRA_0_EN	7	pd_bg_current: Power down bandgap current.	
	CLKTEST_EN	6	Test mode enable including: UPLL reset control.	
	-	5:2	Reserved.	
	UTMI_CLK120_EN	1	Override value to enable UTMI 120M clock source. 0 = stop. 1 = Enable.	
	UTMI_CLK_EN	0	Override value to enable UTMI 30MHz and 60MHz clock source. 0 = stop. 1 = Enable.	
44h (103A89h)	**REG103A89**	**7:0**	**Default : 0x04**	**Access : R/W**
	HS_RX_ROBOUST_EN	7	Enable High speed Rx roboust feature.	
	-	6	Reserved.	
	CLK_274_EN	5	Enable 274MHz clock output.	
	CLK214_SYN_EN	4	Enable clock synthesizer.	
	FORCE_PLL_ON	3	Override enable to enable utmi pll by register. 0 = Normal. 1 = Force utmi pll always on.	
	CLK_CTL_OVERRIDE	2	Override enable to enable clock source by register. 0 = Normal. 1 = Force clock enable by register setting.	
	XTAL12_EN	1	Register to select the source of clk_uhc. 0 = 30MHz for UPLL. 1 = crystal clock.	
	CLK_EXTRA_1_EN	0	reg_all_pass: Enable ISI improvement.	
45h (103A8Ah)	**REG103A8A**	**7:0**	**Default : 0x40**	**Access : R/W**
	CLK_EXTRA_0_INV	7	Reserved.	
	CLKTEST_INV	6	Register control for UPLL divider reset (low active). 0 = Reset. 1 = Normal.	
	-	5:2	Reserved.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	UTMI_CLK120_INV	1	Inverse 120MHz clock source. 0 = Normal. 1 = Inverse clock.	
	UTMI_CLK_INV	0	Inverse 30MHz and 60MHz clock source. 0 = Normal. 1 = Inverse clock.	
45h (103A8Bh)	**REG103A8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CK_INV_RESERVED[6:0]	7:1	Reserved register. Bit <11:9>: HS_TX_CKI select. Bit <12>: enable old HS disconnect sampling mechanism. Bit <13> enable DP/DM swap mechanism. Bit <14>: disable drive port reset (for FL tranceiver only). Bit <15>: select the latch on HS data transfer interface.	
	CLK_EXTRA_1_INV	0	Inverse clock extra1. 0 = Normal. 1 = Inverse clock.	
46h (103A8Ch)	**REG103A8C**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAC_CLK_SEL[1:0]	7:6	MAC clock selection. Bit <6>: set to 1 represent dynamic switched clock for MAC. Set to 0 is the old FIFO access mechanism for MAC. Bit <7>: reserved.	
	TEST_CLOCK_SELECT[5:0]	5:0	UTMI test clock selection. 00h = clk_120mhz_utmi_z. 01h = clk_30mhz_utmi_z. 02h = clk_120_12_1p5_mhz_tx_fsm_z. 03h = clk_120_48_6_mhz_rx_fsm_z. 04h = clk_48_6_mhz_fs_ls_rx_cdr_z. 05h = clk_120_12_1p5_mhz_rx_decoder_z. 06h = clk_10khz_power_on_fsm_z. 07h = clk_1khz_pll_clk_ready_timer_z. 08h = clk_extra_ref_0_z. 09h = clk_extra_ref_1_z. Other = N.A.	
46h	**REG103A8D**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103A8Dh)	UTMI_CKINV_EN_SEL[1:0]	7:6	UTMI 30MHz inverse clock enable generated by 120MHz. 00 = select phase 0. 01 = select phase 1. 10 = select phase 2. 11 = select phase 3. (Default is 1).	
	UTMI_CK_EN_SEL[1:0]	5:4	UTMI 30MHz clock enable generated by 120MHz. 00 = select phase 0. 01 = select phase 1. 10 = select phase 2. 11 = select phase 3. (Default is 3). (refer to UTMI_CKINV_EN_SEL offset is 2).	
	CLK_EXTRA1_DIV_SELECT[1:0]	3:2	Reserved.	
	CLK_EXTRA0_DIV_SELECT	1	Reserved.	
	DOUBLE_DATA_RATE	0	The control option for enable double data rate transfer.	
47h	**REG103A8E**	**7:0**	**Default : 0x00**	**Access : RO**

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UTMI Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	UTMI_DIGITAL_STATUS[7:0]	7:0	UTMI digital part status report. 1. Status [0] : Error flag in elasticity buffer. 0 = normal. 1 = elasticity buffer error. 2. Status [1] : Sync pattern error detected status. 0 = normal. 1 = sync strip error. 3. Status [2] : EOP error detected status. 0 = normal. 1 = EOP error. 4. Status [3] :Bit-stuffer error status in Full/Low speed mode. 0 = normal. 1 = bit stuff error. 5. Status [4] : Underflow status in elasticity buffer. 0 = not underflow. 1 = underflow. 6. Status [5] : Overflow status in elasticity buffer. 0 = not overflow. 1 = overflow. 7. Status [6] : clock_ready. 8. Status [7] : UTMI interrupt status. 0 = no IRQ. 1 = IRQ active. 9. Status [8] : Enable Chirp function while UTMI as a device. 0 = normal. 1 = chirp. 10. Status [9] : Enable Chirp function while UTMI as a host. 0 = normal. 1 = chirp. 11. Status [10] : Disconnect status in host mode. 0 = connected.

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (103A8Fh)	**REG103A8F**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_DIGITAL_STATUS[15:8]	7:0	See description of '103A8Eh'.	
48h (103A90h)	**REG103A90**	**7:0**	**Default : 0x00**	**Access : R/W**
	SE0_SET	7	Enable HS 45 ohm resistor on. 0 = Normal. 1 = Force 45 ohm resistor on.	
	UTMI_INT_CLR	6	Register control for high speed TX serializer enable in term resistor override mode. 1 = Enable. 0 = Disable.	
	FORCE_TX_NONBUSY	5	Force UTMI RX side always input tx_busy signal control. 0 = Normal. 1 = Force tx_busy is 0.	
	FORCE_RX_NONBUSY	4	Force UTMI TX side always input rx_busy signal control. 0 = Normal. 1 = Force rx_busy is 0.	
	TEST_BUS_SELECT[3:0]	3:0	UTMI test bus selection for debugging. 0000 = select test 0. 0001 = select test 1. 0010 = select test 2. ..... 1111 = select test 15. (refer to note 1).	
48h (103A91h)	**REG103A91**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_OVERRIDE	7	Enable HS tx controlled by regiseter. 0 = Normal. 1 = Enable override mode.	
	ERROR_FLAG_CLR	6	Write 1 & write 0 to clear error flag in digital status (address 7). 0: Disable. 1: Enable clear error flag.	
	PHY_MODE_ENABLE	5	Enable UTMI in Phy mode. 0 = Normal. 1 = set UTMI in/out ports from pad.	
	POWER_GOOD_RST	4	SW reset for power good signal. 0 = Normal. 1 = Software reset instead of powergood reset.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_OVERRIDE	3	Enable FL tx controlled by regiseter. 0 = Normal. 1 = Enable override mode.	
	TX_SE0	2	Override FL tx send SE0. 0 = Disable SE0. 1 = Force tx sending SE0.	
	TX_EN	1	Override FL tx enable. 0 = Disable tx. 1 = Force tx enable.	
	TX_DATA	0	Override FL tx data. 0 = transmit 0. 1 = transmit 0.	
49h (103A92h)	**REG103A92**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DEGLITCH_ENZ	7	Register to enable deglitch module. 0 = Enable vdd2low deglitch function. 1 = Disable.	
	VDD2LOW_RST_ENZ	6	Register to enable reset signal of vdd2low. 0 = enable to output vdd2low_rst signal. 1 = Normal.	
	DEGLITCH_PRD[5:0]	5:0	Register to set vdd2low degitch period.	
49h (103A93h)	**REG103A93**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_P1	7	Enable Port-1 debug port.	
	IB_RTERM_TEST[2:0]	6:4	HS RTERM current test.	
	REG_TEST[2:0]	3:1	REG_TEST_p1: Regulator test (port 1 only).	
	USBSYN_RST	0	SW reset for UTMI digital synthesizer. 0 = Normal. 1 = Softeare reset digital synthesizer module in UTMI.	
4Ah (103A94h)	**REG103A94**	**7:0**	**Default : 0x0B**	**Access : R/W**
	XCVRSEL[1:0]	7:6	Override value to set XCVRSEL value(MAC to UTMI). 00 = high speed. 01 = full speed. 10 = low speed. 11 = N.A.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPMODE[1:0]	5:4	Override value to set OPMODE value. (MAC to UTMI). 00 = mode 0. 01 = mode 1. 10 = mode 2. 11 = mode 3.	
	IDDIG	3	Override value to set IDDIG value.(UTMI to MAC). 0 = connected plug is a mini-A. 1 = connected plug is a mini-B.	
	SESSEND	2	Override value to set SESSEND value. (UTMI to MAC). 0 = Vbus > 0.8 V. 1 = Vbus < 0.2 V.	
	AVALID	1	Override value to set A-port value. (UTMI to MAC). 0 = Vbus < 0.8 V. 1 = Vbus > 2.0 V.	
	VBUSVALID	0	Override value to set VBUS VALID value. (UTMI to MAC). 0 = Vbus < 4.4 V. 1 = Vbus > 4.75 V.	
4Ah (103A95h)	**REG103A95**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_IEN_MASK_METHOD	7	Mask hs_tx_ien method.	
	HS_TX_IEN_MASK	6	Mask hs_tx_ien.	
	HOST_CHIRP_DET	5	HOST_CHIRP_DET.	
	USB_BOND_SET	4	Override value for option USB_BOND. 0 = Two port UTMI setting. 1 = One port UTMI setting.	
	USB_BOND_OVD	3	Override bonding option USB_BOND. 0 = Normal. 1 = bonding controlled by register.	
	SUSPENDM	2	Override value to control SUSPENDM. 0 = device in suspend mode. 1 = device in normal mode.	
	MACMODE_OVD	1	Override enable to control mac mode. 0 = Normal. 1 = Change Mac control signal from register.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TERMSEL	0	Override value to set TERMSEL value. (MAC to UTMI). 0 = high speed. 1 = full/low speed.	
4Bh (103A96h)	**REG103A96**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[7:0]	7:0	Digital synthesizer clock frequency setting. MPLL clock divided by N.f setting. N = 5 bits. F = 27 bits.	
4Bh (103A97h)	**REG103A97**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[15:8]	7:0	See description of '103A96h'.	
4Ch (103A98h)	**REG103A98**	**7:0**	**Default : 0xCC**	**Access : R/W**
	SYNTHESIZE_NF[23:16]	7:0	See description of '103A96h'.	
4Ch (103A99h)	**REG103A99**	**7:0**	**Default : 0x23**	**Access : R/W**
	SYNTHESIZE_NF[31:24]	7:0	See description of '103A96h'.	
50h	**REG103AA0**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	PLL_TEST[7:0]	7:0	1. PLL_TEST[0]: PLL reference input clock selection (accompanied with PLL_TEST[0]). {PLL_TEST[26], PLL_TEST[0]}. 00 = Naked crystal input. 01 = Reserved+K98. 10 = Synthesized clock. 11 = Buffered crystal input. 2. PLL_TEST[2:1]: PLL loop divider selection. 00 = / 40. 01 = / 20. 10 = / 10. 11 = / (PLL_TEST[7:3]) / 2. 3. PLL_TEST[7:3]: PLL loop divider control from 3 to 65 (N+1). 000000 = / 65. 000001 = NA. 000010 = / 3. 000011 = / 4. .. 111111 = / 64. 4. PLL_TEST[9:8]: PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, source select. 00 = FBCK33. 01 = REFCK33. 10 = FBCK18. 11 = CLK480 to digital. 5. PLL_TEST[11:10]:PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, post-divider dividing ratio selection. 00 = /1. 01 = /2. 10 = /4. 11 = /8. 6. PLL_TEST[13:12]:CLK480 to digital output phase selection. 00 = A0. 01 = A90. 10 = A0B. 11 = A90B.

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (103AA1h)	**REG103AA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[15:8]	7:0	See description of '103AA0h'.	
51h (103AA2h)	**REG103AA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[23:16]	7:0	See description of '103AA0h'.	
51h (103AA3h)	**REG103AA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[31:24]	7:0	See description of '103AA0h'.	
52h (103AA4h)	**REG103AA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[39:32]	7:0	See description of '103AA0h'.	
53h (103AA6h)	**REG103AA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TED_TEST[7:0]	7:0	1. HS_TED_TEST[1:0] : De-glitch time setting for Squelch. 00 = 4 high-speed bit time. 01 = 6 high-speed bit time. 10 = 8 high-speed bit time. 11 = 2 high-speed bit time. 2. HS_TED_TEST[3:2] :Squelch detector input offset selection. 00 = 0mV. 01 = +12mV. 10 = -12mV. 11 = 0mV. 3. HS_TED_TEST[7:4] : Reserved.	
53h (103AA7h)	**REG103AA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PREAMP_TEST[7:0]	7:0	1. HS_PREAMP_TEST[1:0] : Reserved. 2. HS_PREAMP_TEST[3:2] : High-speed receiver bias current selection. 00 = 40u. 01 = 30u. 10 = 60u. 11 = 50u. 3. HS_PREAMP_TEST[7:4] : Reserved.	
54h	**REG103AA8**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	FL_XCVR_TEST[7:0]	7:0	1. FL_XCVR_TEST[2:0] : Full/low-speed slew rate control capacitor fine tune. 000 = 1.2p. 001 = 1.3p. 010 = 1.4p. 011 = 1.5p. 100 = 0.8p. 101 = 0.9p. 110 = 1.0p. 111 = 1.1p. 2. FL_XCVR_TEST[5:3] : High-speed pull-down resistor fine tune. 000 = 100%. 001 = 97.5%. 010 = 97.5%. 011 = 95%. 100~111 = 80%. 3. FL_XCVR_TEST[7:6] :Full/low-speed pull down resistor fine tune. 00 = 19.35k. 01 = 17.3k. 10 = 21.45k. 11 = 19.35k. 4. FL_XCVR_TEST[9:8] : Full/low-speed pull down resistor fine tune. 00 = 1.2k. 01 = 1.3k. 10 = 1.17k. 11 = 1.19k. 5. FL_XCVR_TEST[10] : Full/low speed slew rate control current fine tune. 0 = current 1X. 1 = current 0.8X. 6. FL_XCVR_TEST[11] : Disable Full/low speed data re-timing by CLK120. 0 = Enabled. 1 = Disabled. 7.

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
54h (103AA9h)	**REG103AA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	FL_XCVR_TEST[15:8]	7:0	See description of '103AA8h'.	
55h	**REG103AAA**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	REF_TEST[7:0]	7:0	1. REF_TEST[1:0] : VSPOUT voltage control (for Squelch voltage threshold). 00 = 0.275V. 01 = 0.225V. 10 = 0.250V. 11 = 0.300V. 2. REF_TEST[3:2] : VSMOUT voltage control (for Squelch voltage threshold). 00 = 0.150V. 01 = 0.100V. 10 = 0.125V. 11 = 0.175V. 3. REF_TEST[5:4] : VCPOUT voltage control (for Disconnect voltage threshold). 00 = 0.70V. 01 = 0.60V. 10 = 0.65V. 11 = 0.75V. 4. REF_TEST[7:6] : VCMOUT voltage control (for Disconnect voltage threshold). 00 = 0.15V. 01 = 0.05V. 10 = 0.10V. 11 = 0.20V. 5. REF_TEST[9:8] : PGD comparator voltage threshold select (with hysteresis=100mV). 1.8V Threshold Vthh Vthl. 00 1.30V 1.20V. 01 1.25V 1.15V. 10 1.20V 1.10V. 11 1.15V 1.05V. 3.3V Threshold Vthh Vthl. 00 2.87V 2.63V. 01 2.74V 2.52V. 10 2.82V 2.58V. 11 2.71V 2.46V. 6. REF_TEST[10] : Enable Power-Good Detector to detect USB phy 3.3V power supply.

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (103AABh)	**REG103AAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	REF_TEST[15:8]	7:0	See description of '103AAAh'.	
56h	**REG103AAC**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI Register (Bank = 103A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	HS_TX_TEST[7:0]	7:0	1. HS_TX_TEST[2:0] : Reserved. 2. HS_TX_TEST[3] :Enable high-speed TX test clock output (accompanied with HS_TX_TEST[28]). 0 = Disable. 1 = Enable. 3. HS_TX_TEST[6:4] : High-speed TX output current adjust. 000 = 100%. 001 = 101.6%. 010 = 103.3%. 011 = 105.0%. 100 = 93.3%. 101 = 95.0%. 110 = 96.7%. 111 = 98.3%. 4. HS_TX_TEST[8:7] : High-speed TX pre-emphasis adjust. 00 = 10.0%. 01 = 10.8%. 10 = 8.33%. 5. HS_TX_TEST[9] : Power-down High-speed TX pre-emphasis bias current. 0 = Enable. 1 = Power-down. 6. HS_TX_TEST[10] : Power-down high-speed TX current bias current. 0 = Enable. 1 = Power-down. 7. HS_TX_TEST[13:11] : HS_RTERM bias current adjust. 000 = 6/6. 001 = 7/6. 010 = 8/6. 011 = 9/6. 100 = 2/6. 101 = 3/6. 110 = 4/6. 111 = 5/6.

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
56h (103AADh)	**REG103AAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[15:8]	7:0	See description of '103AACh'.	
57h (103AAEh)	**REG103AAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[23:16]	7:0	See description of '103AACh'.	
57h (103AAFh)	**REG103AAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[31:24]	7:0	See description of '103AACh'.	
58h (103AB0h)	**REG103AB0**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS[7:0]	7:0	Status report for utmi atop. Status[0] : UTMI pll lock status. Status[1] : UTMI pll flag. Status[2] : UTMI pll flag. Status[3] : UTMI pll clock test status. Status[4] : Power good status. Status[5] : Vbus voltage valid status. Status[6] : OTG session end status (VBUSLO for FS only PHY type). Status[7] : Pad CID status. Status[8] : AVALID_ATOP. Status[9] : HS_DISCONNECT. Status[10] : HS_RX_DATA[0]. Status[11] : HS_RX_CHIRP. Status[12] : FL_LINESTATE0. Status[13] : FL_LINESTATE1. Status[14] : loop back test failed. Status[15] : loop back test finish.	
58h (103AB1h)	**REG103AB1**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS[15:8]	7:0	See description of '103AB0h'.	
59h (103AB2h)	**REG103AB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_LENGTH[7:0]	7:0	TX data length for internal pattern gen. (0~255 bytes).	
59h (103AB3h)	**REG103AB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_RESERVED[4:0]	7:3	Reserved register. Bit <11>: test packet contineous mode for measuring eye. Diagram only. The compare result is invalid. Bit <12>: receiving test packet mode.	

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PG_TX_FIXED_DATA	2	Select fixed data to transmit. 0: Normal. 1: Enable to transmit random data.	
	PG_TX_MODE	1	Select "test packet" to transmit. 0: Normal. 1: Test packet data.	
	PG_TX_GO	0	Tx data enable to transmit for internal pattern gen.	
5Ah (103AB4h)	**REG103AB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[7:0]	7:0	Pattern Gen TX initial data setting.	
5Ah (103AB5h)	**REG103AB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[15:8]	7:0	See description of '103AB4h'.	
5Bh (103AB6h)	**REG103AB6**	**7:0**	**Default : 0x01**	**Access : R/W**
	PG_TX_INC[7:0]	7:0	Pattern Gen TX data incremental value setting.	
5Bh (103AB7h)	**REG103AB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_INC[15:8]	7:0	See description of '103AB6h'.	
5Ch (103AB8h)	**REG103AB8**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	ASRST_ON	7	Asynchronous reset for new FL module.	
	DM1_STATUS	6	Port 1 DM line status.	
	DP1_STATUS	5	Port 1 DP line status.	
	DM_STATUS	4	Port 0 DM line status.	
	DP_STATUS	3	Port 0 DP line status.	
	SELPORT	2	Port select for usb_xcvr switch. 0: Selected port0. 1: Selected port1.	
	VIGEN_PDN	1	VIGEN_PDN.	
	EN_CK_192	0	Enable usb_xcvr 192MHz clock out.	
5Ch (103AB9h)	**REG103AB9**	**7:0**	**Default : 0x28**	**Access : R/W**
	RESERVED2[7:0]	7:0	Reserved register 2. Bit <8>: VBUS select for dummy dual port (reg_selport_vbus). Bit <15:9> reserved.	
5Dh (103ABAh)	**REG103ABA**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_SERDES[7:0]	7:0	Test port for serializer and deserializer.	
5Dh	**REG103ABB**	**7:0**	**Default : 0x00**	**Access : R/W**

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UTMI Register (Bank = 103A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103ABBh)	REG_TEST1[7:0]	7:0	Test register for 65nm process.	
5Eh (103ABCh)	**REG103ABC**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CA_DATA[3:0]	7:4	Calibration detail data.	
	-	3	Reserved.	
	POWER_GOOD_STS	2	ATOP powergood status.	
	CA_END	1	Calibration end (status).	
	CA_START	0	Calibration start.	
5Eh (103ABDh)	**REG103ABD**	**7:0**	**Default : 0x00**	**Access : RO**
	CA_DATA[11:4]	7:0	See description of '103ABCh'.	

SARADC Register (Bank = 103B)

SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (103B00h)	**REG103B00**	**7:0**	**Default : 0x01**	**Access : R/W**
	MUXSEL[2:0]	7:5	Positive siganl input select.	
	AUTO_SWITCH	4	Channel auto-switch.	
	FREERUN	3	Saradc FREERUN control.	
	ONESHOT	2	Saradc ONESHOT control.	
	PORZ	1	Saradc digital reset, low active. When PORZ=0, 1.2V logic in sar adc will be reset.	
	PD	0	Saradc power down. When PD = 1, sar adc power down.	
00h (103B01h)	**REG103B01**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE0[2:0]	7:5	3-bit spare cell.	
	SAMPLE_FLAG	4	Data sample flag.	
	MUXNSEL[2:0]	3:1	Negtive singal input select.	
	SAMPLE_RDY	0	Data sample ready.	
01h (103B02h)	**REG103B02**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CH3_AVG_MODE[1:0]	7:6	Channel 3 data-out select.	
	CH2_AVG_MODE[1:0]	5:4	Channel 2 data-out select.	
	CH1_AVG_MODE[1:0]	3:2	Channel 1 data-out select.	

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SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CH0_AVG_MODE[1:0]	1:0	Channel 0 data-out select. 2'b00 : no average. 2'b01 : 2 stage average. 2'b10 : 4 stage average. 2'b11 : 8 stage average.	
01h (103B03h)	**REG103B03**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CH7_AVG_MODE[1:0]	7:6	Channel 7 data-out select.	
	CH6_AVG_MODE[1:0]	5:4	Channel 6 data-out select.	
	CH5_AVG_MODE[1:0]	3:2	Channel 5 data-out select.	
	CH4_AVG_MODE[1:0]	1:0	Channel 4 data-out select.	
02h (103B04h)	**REG103B04**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS0_PRD[7:0]	7:0	Channel 0 oneshot pulse width = 4 * OS0_PRD (clk cycle).	
02h (103B05h)	**REG103B05**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS1_PRD[7:0]	7:0	Channel 1 oneshot pulse width.	
03h (103B06h)	**REG103B06**	**7:0**	**Default : 0x50**	**Access : R/W**
	OS2_PRD[7:0]	7:0	Channel 2 oneshot pulse width.	
03h (103B07h)	**REG103B07**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS3_PRD[7:0]	7:0	Channel 3 oneshot pulse width.	
04h (103B08h)	**REG103B08**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS4_PRD[7:0]	7:0	Channel 4 oneshot pulse width.	
04h (103B09h)	**REG103B09**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS5_PRD[7:0]	7:0	Channel 5 oneshot pulse width.	
05h (103B0Ah)	**REG103B0A**	**7:0**	**Default : 0x50**	**Access : R/W**
	OS6_PRD[7:0]	7:0	Channel 6 oneshot pulse width.	
05h (103B0Bh)	**REG103B0B**	**7:0**	**Default : 0x50**	**Access : R/W**
	OS7_PRD[7:0]	7:0	Channel 7 oneshot pulse width.	
06h (103B0Ch)	**REG103B0C**	**7:0**	**Default : 0x00**	**Access : RO**
	SAR_DOUT_DFT[7:0]	7:0	Saradc raw data out.	
06h (103B0Dh)	**REG103B0D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TEST[3:0]	7:4	Saradc TEST bits.	
	SAR_SAMP_DFT	3	Saradc raw samp.	
	SAR_EOC_DFT	2	Saradc raw eoc.	
	SAR_DOUT_DFT[9:8]	1:0	See description of '103B0Ch'.	
07h	**REG103B0E**	**7:0**	**Default : 0x00**	**Access : RO**

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SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103B0Eh)	CH0_DOUT[7:0]	7:0	Saradc channel 0 data out.	
07h (103B0Fh)	**REG103B0F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE7[15:10]	7:2	6-bit spare cell.	
	CH0_DOUT[9:8]	1:0	See description of '103B0Eh'.	
08h (103B10h)	**REG103B10**	**7:0**	**Default : 0x00**	**Access : RO**
	CH1_DOUT[7:0]	7:0	Saradc channel 1 data out.	
08h (103B11h)	**REG103B11**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE8[15:10]	7:2	6-bit spare cell.	
	CH1_DOUT[9:8]	1:0	See description of '103B10h'.	
09h (103B12h)	**REG103B12**	**7:0**	**Default : 0x00**	**Access : RO**
	CH2_DOUT[7:0]	7:0	Saradc channel 2 data out.	
09h (103B13h)	**REG103B13**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE9[15:10]	7:2	6-bit spare cell.	
	CH2_DOUT[9:8]	1:0	See description of '103B12h'.	
10h (103B20h)	**REG103B20**	**7:0**	**Default : 0x00**	**Access : RO**
	CH3_DOUT[7:0]	7:0	Saradc channel 3 data out.	
10h (103B21h)	**REG103B21**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE10[15:10]	7:2	6-bit spare cell.	
	CH3_DOUT[9:8]	1:0	See description of '103B20h'.	
11h (103B22h)	**REG103B22**	**7:0**	**Default : 0x00**	**Access : RO**
	CH4_DOUT[7:0]	7:0	Saradc channel 4 data out.	
11h (103B23h)	**REG103B23**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE11[15:10]	7:2	6-bit spare cell.	
	CH4_DOUT[9:8]	1:0	See description of '103B22h'.	
12h (103B24h)	**REG103B24**	**7:0**	**Default : 0x00**	**Access : RO**
	CH5_DOUT[7:0]	7:0	Saradc channel 5 data out.	
12h (103B25h)	**REG103B25**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE12[15:10]	7:2	6-bit spare cell.	
	CH5_DOUT[9:8]	1:0	See description of '103B24h'.	
13h (103B26h)	**REG103B26**	**7:0**	**Default : 0x00**	**Access : RO**
	CH6_DOUT[7:0]	7:0	Saradc channel 6 data out.	
13h (103B27h)	**REG103B27**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE13[15:10]	7:2	6-bit spare cell.	

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SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CH6_DOUT[9:8]	1:0	See description of '103B26h'.	
14h (103B28h)	**REG103B28**	**7:0**	**Default : 0x00**	**Access : RO**
	CH7_DOUT[7:0]	7:0	Saradc channel 7 data out.	
14h (103B29h)	**REG103B29**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE14[15:10]	7:2	6-bit spare cell.	
	CH7_DOUT[9:8]	1:0	See description of '103B28h'.	
15h (103B2Ah)	**REG103B2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CH_SEL[7:0]	7:0	Select enable channels when auto-switch.	
15h (103B2Bh)	**REG103B2B**	**7:0**	**Default : 0x00**	**Access : RO**
	SPARE15[6:0]	7:1	7-bit spare cell.	
	FLAG_AUXC1	0	PAD_AUXC1 flag. 1: PAD_AUXC1 voltage is too high. 0: Normal.	
16h (103B2Ch)	**REG103B2C**	**7:0**	**Default : 0x0F**	**Access : RO, R/W**
	STATE_OBV[3:0]	7:4	Dtop FSM oberve.	
	AUXI_CTRL[1:0]	3:2	AUX current control. 2'b00: 20uA. 2'b01: 40uA. 2'b10: 80uA. 2'b11: 160uA.	
	AUXI_SEL	1	AUX current output pad select. 1'b1: PAD_AUXC1. 1'b0: PAD_AUXC0.	
	PD_AUXI	0	Power down AUX current output. 1: Power down. 0: Output AUX current.	
16h (103B2Dh)	**REG103B2D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE16[3:0]	7:4	4-bit spare cell.	
	STATE_OBV[7:4]	3:0	See description of '103B2Ch'.	
17h (103B2Eh)	**REG103B2E**	**7:0**	**Default : 0xC3**	**Access : R/W**
	SPARE17[1:0]	7:6	10-bit spare cell.	

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SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	REFNSEL[2:0]	5:3	Saradc negative reference select. SAR_REFNSEL[1:0] = 00, select AVSS as negative reference. 01, select XN as negative reference. 10, select YN as negative reference. 11, select AVSS as negative reference.	
	REFSEL[2:0]	2:0	Saradc positive reference select. REFSEL[2]: reserved. REFSEL[1:0] = 00, select AVDD as positive reference. 01, select XP as positive reference. 10, select YP as positive reference. 11, select VREF2P0 as positive reference.	
17h (103B2Fh)	**REG103B2F**	**7:0**	**Default : 0x3F**	**Access : R/W**
	SPARE17[9:2]	7:0	See description of '103B2Eh'.	
18h (103B30h)	**REG103B30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GPS_CHNL[2:0]	2:0	Gps data out select.	
20h (103B40h)	**REG103B40**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH1_UPB[7:0]	7:0	Channel 1 upper bound.	
20h (103B41h)	**REG103B41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH1_UPB[9:8]	1:0	See description of '103B40h'.	
21h (103B42h)	**REG103B42**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH1_LOB[7:0]	7:0	Channel 1 lower bound.	
21h (103B43h)	**REG103B43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH1_LOB[9:8]	1:0	See description of '103B42h'.	
22h (103B44h)	**REG103B44**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH2_UPB[7:0]	7:0	Channel 2 upper bound.	
22h (103B45h)	**REG103B45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH2_UPB[9:8]	1:0	See description of '103B44h'.	
23h (103B46h)	**REG103B46**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH2_LOB[7:0]	7:0	Channel 2 lower bound.	
23h	**REG103B47**	**7:0**	**Default : 0x00**	**Access : R/W**

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SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103B47h)	-	7:2	Reserved.	
	SAR_CH2_LOB[9:8]	1:0	See description of '103B46h'.	
24h (103B48h)	**REG103B48**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH3_UPB[7:0]	7:0	Channel 3 upper bound.	
24h (103B49h)	**REG103B49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH3_UPB[9:8]	1:0	See description of '103B48h'.	
25h (103B4Ah)	**REG103B4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH3_LOB[7:0]	7:0	Channel 3 lower bound.	
25h (103B4Bh)	**REG103B4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH3_LOB[9:8]	1:0	See description of '103B4Ah'.	
26h (103B4Ch)	**REG103B4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH4_UPB[7:0]	7:0	Channel 4 upper bound.	
26h (103B4Dh)	**REG103B4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH4_UPB[9:8]	1:0	See description of '103B4Ch'.	
27h (103B4Eh)	**REG103B4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH4_LOB[7:0]	7:0	Channel 4 lower bound.	
27h (103B4Fh)	**REG103B4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH4_LOB[9:8]	1:0	See description of '103B4Eh'.	
28h (103B50h)	**REG103B50**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH5_UPB[7:0]	7:0	Channel 5 upper bound.	
28h (103B51h)	**REG103B51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH5_UPB[9:8]	1:0	See description of '103B50h'.	
29h (103B52h)	**REG103B52**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH5_LOB[7:0]	7:0	Channel 5 lower bound.	
29h (103B53h)	**REG103B53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH5_LOB[9:8]	1:0	See description of '103B52h'.	
2Ah	**REG103B54**	**7:0**	**Default : 0x00**	**Access : R/W**

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SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103B54h)	SAR_CH6_UPB[7:0]	7:0	Channel 6 upper bound.	
2Ah (103B55h)	**REG103B55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH6_UPB[9:8]	1:0	See description of '103B54h'.	
2Bh (103B56h)	**REG103B56**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH6_LOB[7:0]	7:0	Channel 6 lower bound.	
2Bh (103B57h)	**REG103B57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH6_LOB[9:8]	1:0	See description of '103B56h'.	
2Ch (103B58h)	**REG103B58**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH7_UPB[7:0]	7:0	Channel 7 upper bound.	
2Ch (103B59h)	**REG103B59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH7_UPB[9:8]	1:0	See description of '103B58h'.	
2Dh (103B5Ah)	**REG103B5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH7_LOB[7:0]	7:0	Channel 7 lower bound.	
2Dh (103B5Bh)	**REG103B5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH7_LOB[9:8]	1:0	See description of '103B5Ah'.	
2Eh (103B5Ch)	**REG103B5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH8_UPB[7:0]	7:0	Channel 8 upper bound.	
2Eh (103B5Dh)	**REG103B5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH8_UPB[9:8]	1:0	See description of '103B5Ch'.	
2Fh (103B5Eh)	**REG103B5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_CH8_LOB[7:0]	7:0	Channel 8 lower bound.	
2Fh (103B5Fh)	**REG103B5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_CH8_LOB[9:8]	1:0	See description of '103B5Eh'.	
30h (103B60h)	**REG103B60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	KEYPAD_LEVEL	3	Level of keypad.	
	-	2:0	Reserved.	

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SARADC Register (Bank = 103B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (103B61h)	**REG103B61**	**7:0**	**Default : 0x08**	**Access : R/W**
	SAR_TRAD	7	SAR_TRAD.	
	-	6:4	Reserved.	
	SAR_8CH_EN	3	1: Sar 8 channel. 0: Sar 4 channel.	
	-	2:0	Reserved.	
34h (103B68h)	**REG103B68**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SAR_INT_MASK[7:0]	7:0	Interrupt mask for sar_int. 0: Enable. 1: Disable.	
34h (103B69h)	**REG103B69**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SAR_INT_MASK[8]	0	See description of '103B68h'.	
35h (103B6Ah)	**REG103B6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_INT_CLR[7:0]	7:0	Interrupt clear for sar_int.	
35h (103B6Bh)	**REG103B6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SAR_INT_CLR[8]	0	See description of '103B6Ah'.	
36h (103B6Ch)	**REG103B6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_INT_FORCE[7:0]	7:0	Force interrupt for sar_int.	
36h (103B6Dh)	**REG103B6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SAR_INT_FORCE[8]	0	See description of '103B6Ch'.	
37h (103B6Eh)	**REG103B6E**	**7:0**	**Default : 0x00**	**Access : RO**
	SAR_INT_STATUS[7:0]	7:0	Status of sar_int.	
37h (103B6Fh)	**REG103B6F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SAR_INT_STATUS[8]	0	See description of '103B6Eh'.	

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PIU_NONPM Register (Bank = 103C)

PIU_NONPM Register (Bank = 103C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (103C18h)	**REG103C18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MIU0_SIZE	1	Miu size selection for 8051.	
	XD2MIU_BRDG_SW_RST	0	Xd2miu bridge sw reset, 1'b1 --> reset, 1'b0 --> not reset.	
0Dh (103C1Ah)	**REG103C1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BDMA_SW_RST	0	Software reset BDMA; 1 => reset.	
0Fh (103C1Eh)	**REG103C1E**	**7:0**	**Default : 0xAA**	**Access : R/W**
	SPI_PF_PASSWORD[7:0]	7:0	When booting from MCU51. 0xaaaa: MCU32,HE_MCU32 can access SPI Flash, but cannot access PF. !=0xaaaa: MCU32,HE_MCU32 can access PF Flash, but cannot access SPI Flash. When booting from HE_MCU32. Don't care.	
0Fh (103C1Fh)	**REG103C1F**	**7:0**	**Default : 0xAA**	**Access : R/W**
	SPI_PF_PASSWORD[15:8]	7:0	See description of '103C1Eh'.	

TVE0 Register (Bank = 103E)

TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (103E00h)	**REG103E00**	**7:0**	**Default : 0x01**	**Access : R/W**
	HSYNC_ST[7:0]	7:0	NTSC=1, NTSC443=1, NTSC-J=1, PAL_M=1, PAL_N=1, PAL_NC=1, B,D,G,H,I,J,K1,J=1.	
00h (103E01h)	**REG103E01**	**7:0**	**Default : 0x7E**	**Access : R/W**
	HSYNC_END[7:0]	7:0	NTSC=127, NTSC443=127, NTSC-J=127, PAL_M=127, PAL_N=134, PAL_NC=127, B,D,G,H,I,J,K1,J=127.	
01h (103E02h)	**REG103E02**	**7:0**	**Default : 0x94**	**Access : R/W**
	BURST_ST[7:0]	7:0	NTSC=148, NTSC443=148, NTSC-J=148, PAL_M=161, PAL_N=157, PAL_NC=157, B,D,G,H,I,J,K1,J=157.	
01h	**REG103E03**	**7:0**	**Default : 0xD7**	**Access : R/W**

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103E03h)	BURST_END[7:0]	7:0	NTSC=215, NTSC443=215, NTSC-J=215, PAL_M=228, PAL_N=231, PAL_NC=217, B,D,G,H,I,J,K1,J=217.	
02h (103E04h)	**REG103E04**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTEND_MD	7	Input source luma extend mode, 0: 4-tap filter (-1, 9, 9, -1), 1: repreat ;	
	DAC27_EN	6	0: Dac run 108MHZ, 1: 27MHz ;	
	CSRCUP4_MD[1:0]	5:4	00: 4-tap filter chroma scale up, 01: bilinear scale up, 10: repeat ;	
	LSRCUP4_MD[1:0]	3:2	00: 4-tap filter luma scale up, 01: bilinear scale up, 10: repeat ;	
	PHSRESET_MD[1:0]	1:0	00: Reset 0 degree per 8 frame, 01: reset 180 degree per frame, 10: reset 180 degree per 2 frame, 11: no reset ;	
02h (103E05h)	**REG103E05**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	HSYNC_COMPENSATE	3	Hsync compensate.	
	CEXTEND_MD	2	C extend mode.	
	DACA_SEL[1:0]	1:0	00: Daca, 01:dacb, 10:dacc, 11:dacd ;	
03h (103E06h)	**REG103E06**	**7:0**	**Default : 0x16**	**Access : R/W**
	FORCE_BLACK	7	Force black video ;	
	Y_DELAY_FINE[1:0]	6:5	Y dealy fine tune.	
	ITSTP	4	Internal test pattern ;	
	VTOTAL_SEL	3	Select 525 or 625 line ;NTSC=0, NTSC443=0, NTSC-J=0, PAL_M=0, PAL_N=1, PAL_NC=1, B,D,G,H,I,J,K1,J=1.	
	Y_DELAY[2:0]	2:0	Normal =init val.	
03h (103E07h)	**REG103E07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CBCR_SWAP_EN	1	Cb/cr swap enable ;	
	-	0	Reserved.	
04h (103E08h)	**REG103E08**	**7:0**	**Default : 0x00**	**Access : R/W**
	CONTRAST[7:0]	7:0	Luma CONTRAST gain, NTSC(800-282)/1024, PAL (800-252)/1024 ; NTSC=0x4c00, NTSC443=0x4c00,NTSC_J=0x5200,PAL=0x5000.	
04h (103E09h)	**REG103E09**	**7:0**	**Default : 0x4C**	**Access : R/W**
	CONTRAST[15:8]	7:0	See description of '103E08h'.	

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (103E0Ah)	**REG103E0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHSADJ[7:0]	7:0	Burst phase offset ;	
05h (103E0Bh)	**REG103E0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HUE[7:0]	7:0	Chroma HUE offset ;	
06h (103E0Ch)	**REG103E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PAL318_BSW	1	0: One hsync width in line #318 for PAL , 1: 1/2 hsync width in line #318 for PAL.	
	PAL_SWITCH_EN	0	PAL switch enable ;NTSC=0, NTSC443=0, NTSC-J=0, PAL_M=1, PAL_N=1, PAL_NC=1, B,D,G,H,I,J,K1,J=1.	
07h (103E0Eh)	**REG103E0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SOFT_RST	0	Software reset ;	
08h (103E10h)	**REG103E10**	**7:0**	**Default : 0x00**	**Access : R/W**
	LINE_OFFSET[7:0]	7:0	Line offset ;	
08h (103E11h)	**REG103E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LINE_OFFSET_MD	2	Line offset mode ;	
	LINE_OFFSET[9:8]	1:0	See description of '103E10h'.	
09h (103E12h)	**REG103E12**	**7:0**	**Default : 0x00**	**Access : R/W**
	HTOTAL[7:0]	7:0	NTSC: 858x2 PAL:864x2 ;NTSC=1716, NTSC443=1716, NTSC-J=1716, PAL_M=1716, PAL_N=1728, PAL_NC=1728, B,D,G,H,I,J,K1,J=1728.	
09h (103E13h)	**REG103E13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HTOTAL[10:8]	2:0	See description of '103E12h'.	
0Ah (103E14h)	**REG103E14**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRIGHT[7:0]	7:0	NTSC=0x8000, NTSC443=0x8000, NTSC-J=0x8000, PAL_M=0x8000, PAL_N=0x8000, PAL_NC=0x8000, B,D,G,H,I,J,K1,J=0x8000.	
0Ah (103E15h)	**REG103E15**	**7:0**	**Default : 0x80**	**Access : R/W**
	BRIGHT[15:8]	7:0	See description of '103E14h'.	
0Bh	**REG103E16**	**7:0**	**Default : 0x1F**	**Access : R/W**

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103E16h)	PHS_STEP1[7:0]	7:0	Burst phase step ; NTSC=0x21f07c1f, NTSC443=0x2a098acb, NTSC-J=0x21f07c1f, PAL_M=0x21e6EfE3, PAL_N=0x2a098acb, PAL_NC=0x21f69446, PAL_B,D,G,H,I,J,K1,J=0x2a098acb.	
0Bh (103E17h)	**REG103E17**	**7:0**	**Default : 0x7C**	**Access : R/W**
	PHS_STEP1[15:8]	7:0	See description of '103E16h'.	
0Ch (103E18h)	**REG103E18**	**7:0**	**Default : 0xF0**	**Access : R/W**
	PHS_STEP1[23:16]	7:0	See description of '103E16h'.	
0Ch (103E19h)	**REG103E19**	**7:0**	**Default : 0x21**	**Access : R/W**
	PHS_STEP1[31:24]	7:0	See description of '103E16h'.	
0Dh (103E1Ah)	**REG103E1A**	**7:0**	**Default : 0xD0**	**Access : R/W**
	PHS_STEP2[7:0]	7:0	Lower stage fraction ;NTSC=0xd0, NTSC443=0x52e, NTSC-J=0xd0, PAL_M=0x990, PAL_N=0x52e, PAL_NC=0xC2E, B,D,G,H,I,J,K1,J=0x52e.	
0Dh (103E1Bh)	**REG103E1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHS_STEP2[15:8]	7:0	See description of '103E1Ah'.	
0Eh (103E1Ch)	**REG103E1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHS_STEP3[7:0]	7:0	625 stage fraction ;NTSC=0x0, NTSC443=0x1b2, NTSC-J=0x0, PAL_M=0x0, PAL_N=0x1b2, PAL_NC=0x1B2, B,D,G,H,I,J,K1,J=0x1b2.	
0Eh (103E1Dh)	**REG103E1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PHS_STEP3[9:8]	1:0	See description of '103E1Ch'.	
0Fh (103E1Eh)	**REG103E1E**	**7:0**	**Default : 0x05**	**Access : R/W**
	LFIR_COEF0[7:0]	7:0	Luma filter coef0.	
0Fh (103E1Fh)	**REG103E1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF0[12:8]	4:0	See description of '103E1Eh'.	
10h (103E20h)	**REG103E20**	**7:0**	**Default : 0xF8**	**Access : R/W**
	LFIR_COEF1[7:0]	7:0	Luma filter coef1.	
10h	**REG103E21**	**7:0**	**Default : 0x1F**	**Access : R/W**

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103E21h)	-	7:5	Reserved.	
	LFIR_COEF1[12:8]	4:0	See description of '103E20h'.	
11h (103E22h)	**REG103E22**	**7:0**	**Default : 0xF8**	**Access : R/W**
	LFIR_COEF2[7:0]	7:0	Luma filter coef2.	
11h (103E23h)	**REG103E23**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF2[12:8]	4:0	See description of '103E22h'.	
12h (103E24h)	**REG103E24**	**7:0**	**Default : 0x23**	**Access : R/W**
	LFIR_COEF3[7:0]	7:0	Luma filter coef3.	
12h (103E25h)	**REG103E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF3[12:8]	4:0	See description of '103E24h'.	
13h (103E26h)	**REG103E26**	**7:0**	**Default : 0xE4**	**Access : R/W**
	LFIR_COEF4[7:0]	7:0	Luma filter coef4.	
13h (103E27h)	**REG103E27**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF4[12:8]	4:0	See description of '103E26h'.	
14h (103E28h)	**REG103E28**	**7:0**	**Default : 0xD3**	**Access : R/W**
	LFIR_COEF5[7:0]	7:0	Luma filter coef5.	
14h (103E29h)	**REG103E29**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF5[12:8]	4:0	See description of '103E28h'.	
15h (103E2Ah)	**REG103E2A**	**7:0**	**Default : 0x77**	**Access : R/W**
	LFIR_COEF6[7:0]	7:0	Luma filter coef6.	
15h (103E2Bh)	**REG103E2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF6[12:8]	4:0	See description of '103E2Ah'.	
16h (103E2Ch)	**REG103E2C**	**7:0**	**Default : 0xCE**	**Access : R/W**
	LFIR_COEF7[7:0]	7:0	Luma filter coef7.	
16h (103E2Dh)	**REG103E2D**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF7[12:8]	4:0	See description of '103E2Ch'.	
17h	**REG103E2E**	**7:0**	**Default : 0x1B**	**Access : R/W**

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103E2Eh)	LFIR_COEF8[7:0]	7:0	Luma filter coef8.	
17h (103E2Fh)	**REG103E2F**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF8[12:8]	4:0	See description of '103E2Eh'.	
18h (103E30h)	**REG103E30**	**7:0**	**Default : 0x44**	**Access : R/W**
	LFIR_COEF9[7:0]	7:0	Luma filter coef9.	
18h (103E31h)	**REG103E31**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF9[12:8]	4:0	See description of '103E30h'.	
19h (103E32h)	**REG103E32**	**7:0**	**Default : 0x1A**	**Access : R/W**
	LFIR_COEF10[7:0]	7:0	Luma filter coef10.	
19h (103E33h)	**REG103E33**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	LFIR_COEF10[12:8]	4:0	See description of '103E32h'.	
1Ah (103E34h)	**REG103E34**	**7:0**	**Default : 0xF3**	**Access : R/W**
	CFIR_COEF0[7:0]	7:0	Chroma filter coef0.	
1Ah (103E35h)	**REG103E35**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF0[11:8]	3:0	See description of '103E34h'.	
1Bh (103E36h)	**REG103E36**	**7:0**	**Default : 0xDA**	**Access : R/W**
	CFIR_COEF1[7:0]	7:0	Chroma filter coef1.	
1Bh (103E37h)	**REG103E37**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF1[11:8]	3:0	See description of '103E36h'.	
1Ch (103E38h)	**REG103E38**	**7:0**	**Default : 0xBE**	**Access : R/W**
	CFIR_COEF2[7:0]	7:0	Chroma filter coef2.	
1Ch (103E39h)	**REG103E39**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF2[11:8]	3:0	See description of '103E38h'.	
1Dh (103E3Ah)	**REG103E3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CFIR_COEF3[7:0]	7:0	Chroma filter coef3.	
1Dh (103E3Bh)	**REG103E3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CFIR_COEF3[11:8]	3:0	See description of '103E3Ah'.	
1Eh (103E3Ch)	**REG103E3C**	**7:0**	**Default : 0xCC**	**Access : R/W**
	CFIR_COEF4[7:0]	7:0	Chroma filter coef4.	
1Eh (103E3Dh)	**REG103E3D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF4[11:8]	3:0	See description of '103E3Ch'.	
1Fh (103E3Eh)	**REG103E3E**	**7:0**	**Default : 0x23**	**Access : R/W**
	CFIR_COEF5[7:0]	7:0	Chroma filter coef5.	
1Fh (103E3Fh)	**REG103E3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF5[11:8]	3:0	See description of '103E3Eh'.	
20h (103E40h)	**REG103E40**	**7:0**	**Default : 0xBB**	**Access : R/W**
	CFIR_COEF6[7:0]	7:0	Chroma filter coef6.	
20h (103E41h)	**REG103E41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF6[11:8]	3:0	See description of '103E40h'.	
21h (103E42h)	**REG103E42**	**7:0**	**Default : 0x7D**	**Access : R/W**
	CFIR_COEF7[7:0]	7:0	Chroma filter coef7.	
21h (103E43h)	**REG103E43**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF7[11:8]	3:0	See description of '103E42h'.	
22h (103E44h)	**REG103E44**	**7:0**	**Default : 0x42**	**Access : R/W**
	CFIR_COEF8[7:0]	7:0	Chroma filter coef8.	
22h (103E45h)	**REG103E45**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF8[11:8]	3:0	See description of '103E44h'.	
23h (103E46h)	**REG103E46**	**7:0**	**Default : 0xD5**	**Access : R/W**
	CFIR_COEF9[7:0]	7:0	Chroma filter coef9.	
23h (103E47h)	**REG103E47**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF9[11:8]	3:0	See description of '103E46h'.	
24h (103E48h)	**REG103E48**	**7:0**	**Default : 0x0C**	**Access : R/W**
	CFIR_COEF10[7:0]	7:0	Chroma filter coef10.	

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (103E49h)	**REG103E49**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	CFIR_COEF10[11:8]	3:0	See description of '103E48h'.	
25h (103E4Ah)	**REG103E4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	AV_ST[7:0]	7:0	NTSC=256, NTSC443=256, NTSC-J=256, PAL_M=250, PAL_N=254, PAL_NC=279, B,D,G,H,I,J,K1,J=279.	
25h (103E4Bh)	**REG103E4B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	AV_ST[10:8]	2:0	See description of '103E4Ah'.	
26h (103E4Ch)	**REG103E4C**	**7:0**	**Default : 0x8D**	**Access : R/W**
	AV_END[7:0]	7:0	NTSC=1677, NTSC443=1677, NTSC-J=1677, PAL_M=1676, PAL_N=1686, PAL_NC=1686, B,D,G,H,I,J,K1,J=1686.	
26h (103E4Dh)	**REG103E4D**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:3	Reserved.	
	AV_END[10:8]	2:0	See description of '103E4Ch'.	
27h (103E4Eh)	**REG103E4E**	**7:0**	**Default : 0x2A**	**Access : R/W**
	PAD_LEVEL[7:0]	7:0	NTSC=42, NTSC443=42, NTSC-J=0, PAL_M=42, PAL_N=42, PAL_NC=0, B,D,G,H,I,J,K1,J=0.	
27h (103E4Fh)	**REG103E4F**	**7:0**	**Default : 0x10**	**Access : R/W**
	SYNC_TIP_LEVEL[7:0]	7:0	NTSC=16, NTSC443=16, NTSC-J=16, PAL_M=16, PAL_N=16, PAL_NC=16, B,D,G,H,I,J,K1,J=16.	
28h (103E50h)	**REG103E50**	**7:0**	**Default : 0xF0**	**Access : R/W**
	BLANK_LEVEL[7:0]	7:0	NTSC=240, NTSC443=240, NTSC-J=240, PAL_M=240, PAL_N=240, PAL_NC=252, B,D,G,H,I,J,K1,J=252.	
28h (103E51h)	**REG103E51**	**7:0**	**Default : 0x38**	**Access : R/W**
	SYNC_STEP[7:0]	7:0	NTSC=56, NTSC443=56, NTSC-J=56, PAL_M=56, PAL_N=40, PAL_NC=40, B,D,G,H,I,J,K1,J=40.	
29h (103E52h)	**REG103E52**	**7:0**	**Default : 0x13**	**Access : R/W**
	BURST_STEP[7:0]	7:0	NTSC=0x13, NTSC443=0x13, NTSC-J=0x13, PAL_M=0x13, PAL_N=0x14, PAL_NC=0x14, B,D,G,H,I,J,K1,J=0x14.	
29h (103E53h)	**REG103E53**	**7:0**	**Default : 0x70**	**Access : R/W**
	BURST_AMP[7:0]	7:0	NTSC=0x70, NTSC443=0x70, NTSC-J=0x70, PAL_M=0x54, PAL_N=0x54, PAL_NC=0x54, B,D,G,H,I,J,K1,J=0x54.	

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Ah (103E54h)	**REG103E54**	**7:0**	**Default : 0x41**	**Access : R/W**
	SAT_U[7:0]	7:0	U saturation gain, 0.855 * (800 - 282)/1024 ; NTSC,NTSC443=0x41,NTSC_J=0x46,PAL=0x44.	
2Ah (103E55h)	**REG103E55**	**7:0**	**Default : 0x5B**	**Access : R/W**
	SAT_V[7:0]	7:0	V saturation gain, 1.205*(800 - 282)/1024 ;NTSC,NTSC443=0x5B,NTSC-J=0x62, PAL=0x60.	
2Dh (103E5Ah)	**REG103E5A**	**7:0**	**Default : 0x20**	**Access : R/W**
	Y_CLAMP[7:0]	7:0	Y clamping.	
2Dh (103E5Bh)	**REG103E5B**	**7:0**	**Default : 0x33**	**Access : R/W**
	AV_ST_EARLY[3:0]	7:4	Active video start early.	
	-	3:2	Reserved.	
	Y_CLAMP[9:8]	1:0	See description of '103E5Ah'.	
2Fh (103E5Eh)	**REG103E5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HF_ST[7:0]	7:0	H frame start (<= reg_av_st) for over scan.	
2Fh (103E5Fh)	**REG103E5F**	**7:0**	**Default : 0x01**	**Access : R/W**
	RESER00[4:0]	7:3	Reserve00.	
	HF_ST[10:8]	2:0	See description of '103E5Eh'.	
30h (103E60h)	**REG103E60**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESER01[7:0]	7:0	Reserve01.	
30h (103E61h)	**REG103E61**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESER01[15:8]	7:0	See description of '103E60h'.	
31h (103E62h)	**REG103E62**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESER02[7:0]	7:0	Reserve02.	
31h (103E63h)	**REG103E63**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESER02[15:8]	7:0	See description of '103E62h'.	
32h (103E64h)	**REG103E64**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESER03[7:0]	7:0	Reserve03.	
32h (103E65h)	**REG103E65**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESER03[15:8]	7:0	See description of '103E64h'.	
33h (103E66h)	**REG103E66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESER04[7:0]	7:0	Reserve04.	
33h	**REG103E67**	**7:0**	**Default : 0x00**	**Access : R/W**

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TVE0 Register (Bank = 103E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103E67h)	RESER04[15:8]	7:0	See description of '103E66h'.	
3Eh (103E7Ch)	**REG103E7C**	**7:0**	**Default : 0x03**	**Access : R/W**
	START_PIXNUM[7:0]	7:0	Start pixel number for syn video source. = reg_hf_st + 3.	
3Eh (103E7Dh)	**REG103E7D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	START_PIXNUM[10:8]	2:0	See description of '103E7Ch'.	
3Fh (103E7Eh)	**REG103E7E**	**7:0**	**Default : 0x17**	**Access : R/W**
	START_LINENUM[7:0]	7:0	Start line number for syn video source. PAL, NTSC = 23. PAL_M = 20.	
3Fh (103E7Fh)	**REG103E7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	START_TVE_HARDWARE	3	Hardware mode trigger TVE.	
	START_TVE_SOFTWARE	2	Software mode trigger TVE.	
	START_LINENUM[9:8]	1:0	See description of '103E7Eh'.	
40h (103E80h)	**REG103E80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VEOUT_YSEL[1:0]	3:2	Sync source sel; 00:CVBS; 01:Y ; 1X: only sync.	
	VEOUT_SEL[1:0]	1:0	00: CVBS, Y, C; 01:CVBS, Y, Cb, Cr; 10: CVBS, R, G, B ;	
72h (103EE4h)	**REG103EE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAL525_1STST[7:0]	7:0	Pal 525 normal line start 1st field ;	
72h (103EE5h)	**REG103EE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PAL525_1STST[9:8]	1:0	See description of '103EE4h'.	
73h (103EE6h)	**REG103EE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAL525_2NDST[7:0]	7:0	Pal 525 normal line start 2nd field ;	
73h (103EE7h)	**REG103EE7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PAL525_2NDST[9:8]	1:0	See description of '103EE6h'.	

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TVE1 Register (Bank = 103F)

TVE1 Register (Bank = 103F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
77h (103FEEh)	**REG103FEE**	**7:0**	**Default : 0x84**	**Access : R/W**
	MID_LINE1[7:0]	7:0	Mid line.	
77h (103FEFh)	**REG103FEF**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	MID_LINE1[10:8]	2:0	See description of '103FEEh'.	
78h (103FF0h)	**REG103FF0**	**7:0**	**Default : 0x8B**	**Access : R/W**
	MID_LINE2[7:0]	7:0	Mid line.	
78h (103FF1h)	**REG103FF1**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	MID_LINE2[10:8]	2:0	See description of '103FF0h'.	
79h (103FF3h)	**REG103FF3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	BLANK_STEP_EN	4	Blank rise step enable.	
	-	3:0	Reserved.	
7Ah (103FF4h)	**REG103FF4**	**7:0**	**Default : 0x90**	**Access : R/W**
	BLANK_STEP_LEVEL[7:0]	7:0	Blank rise step value.	
7Ah (103FF5h)	**REG103FF5**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	BLANK_STEP_LEVEL[11:8]	3:0	See description of '103FF4h'.	
7Bh (103FF6h)	**REG103FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_EMPTY_CNT[7:0]	7:0	Fifo empty count per line.	
7Bh (103FF7h)	**REG103FF7**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	CLEAR_FIFO_EMPTY	5	CLEAR_FIFO_EMPTY.	
	FIFO_EMPTY	4	FIFO_EMPTY.	
	-	3	Reserved.	
	FIFO_EMPTY_CNT[10:8]	2:0	See description of '103FF6h'.	

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MPIF Register (Bank = 1104)

MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (110400h)	**REG110400**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MPIF_LC1A_IDX[2:0]	6:4	MPIF Logical Channel 1a index.	
	MPIF_LC1A_SID[1:0]	3:2	MPIF Logical Channel 1a Slave ID.	
	MPIF_LC1A_RW	1	MPIF Logical Channel 1a read/write.	
	MPIF_LC1A_VLD	0	MPIF Logical Channel 1a valid.	
00h (110401h)	**REG110401**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC1A_DATA[7:0]	7:0	MPIF Logical Channel 1a data.	
	MPIF_LC1A_DATA[7:0]	7:0	MPIF Logical Channel 1a data.	
01h (110402h)	**REG110402**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2A_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 times. 2: 2 times. 3: 3 times.	
	-	5	Reserved.	
	MPIF_LC2A_CHK	4	MPIF Logical Channel 2a check enable.	
	MPIF_LC2A_SID[1:0]	3:2	MPIF Logical Channel 2a Slave ID.	
	MPIF_LC2A_RW	1	MPIF Logical Channel 2a read/write.	
	MPIF_LC2A_VLD	0	MPIF Logical Channel 2a valid.	
02h (110404h)	**REG110404**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2A_ADR[7:0]	7:0	MPIF Logical Channel 2a address.	
02h (110405h)	**REG110405**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2A_ADR[15:8]	7:0	See description of '110404h'.	
03h (110406h)	**REG110406**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MPIF_LC2A_DATA[7:0]	7:0	MPIF Logical Channel 2a data.	
	STS_MPIF_LC2A_DATA[7:0]	7:0	MPIF Logical Channel 2a data.	
03h (110407h)	**REG110407**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MPIF_LC2A_DATA[15:8]	7:0	See description of '110406h'.	
	STS_MPIF_LC2A_DATA[15:8]	7:0	See description of '110406h'.	
04h	**REG110408**	**7:0**	**Default : 0x00**	**Access : R/W**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110408h)	MPIF_LC2B_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 times. 2: 2 times. 3: 3 times.	
	-	5	Reserved.	
	MPIF_LC2B_CHK	4	MPIF Logical Channel 2b check enable.	
	MPIF_LC2B_SID[1:0]	3:2	MPIF Logical Channel 2b Slave ID.	
	MPIF_LC2B_RW	1	MPIF Logical Channel 2b read/write.	
	MPIF_LC2B_VLD	0	MPIF Logical Channel 2b valid.	
05h (11040Ah)	**REG11040A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2B_ADR[7:0]	7:0	MPIF Logical Channel 2b address.	
05h (11040Bh)	**REG11040B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2B_ADR[15:8]	7:0	See description of '11040Ah'.	
06h (11040Ch)	**REG11040C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC2B_DATA[7:0]	7:0	MPIF Logical Channel 2b data.	
	MPIF_LC2B_DATA[7:0]	7:0	MPIF Logical Channel 2b data.	
06h (11040Dh)	**REG11040D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC2B_DATA[15:8]	7:0	See description of '11040Ch'.	
	MPIF_LC2B_DATA[15:8]	7:0	See description of '11040Ch'.	
07h (11040Eh)	**REG11040E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 times. 2: 2 times. 3: 3 times.	
	MPIF_LC3A_RETRX	5	MPIF Logical Channel 3a re-transmit/receive packet indicator.	
	MPIF_LC3A_CHK	4	MPIF Logical Channel 3a check enable.	
	MPIF_LC3A_SID[1:0]	3:2	MPIF Logical Channel 3a Slave ID.	
	MPIF_LC3A_RW	1	MPIF Logical Channel 3a read/write.	
	MPIF_LC3A_VLD	0	MPIF Logical Channel 3a valid.	
07h (11040Fh)	**REG11040F**	**7:0**	**Default : 0x40**	**Access : R/W**
	MPIF_LC3A_WCNT[3:0]	7:4	MPIF Logical Channel 3a max wait number.	

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MPIF_LC3A_RX_NWMIU	3	MPIF Logical Channel 3a not wait miu done.	
	MPIF_LC3A_FMODE	2	MPIF Logical Channel 3a fast read/write mode.	
	MPIF_LC3A_MIUSEL	1	MPIF Logical Channel 3a MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_LC3A_SRC	0	MPIF Logical Channel 3a source/destination selection. 0: To/from RIU. 1: To/from MIU.	
08h (110410h)	**REG110410**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_PKTLEN[7:0]	7:0	MPIF Logical Channel 3a packet total length.	
08h (110411h)	**REG110411**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_PKTLEN[15:8]	7:0	See description of '110410h'.	
09h (110412h)	**REG110412**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[7:0]	7:0	MPIF Logical Channel 3a data.	
	MPIF_LC3A_DATA[7:0]	7:0	MPIF Logical Channel 3a data.	
09h (110413h)	**REG110413**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[15:8]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[15:8]	7:0	See description of '110412h'.	
0Ah (110414h)	**REG110414**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[23:16]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[23:16]	7:0	See description of '110412h'.	
0Ah (110415h)	**REG110415**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[31:24]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[31:24]	7:0	See description of '110412h'.	
0Bh (110416h)	**REG110416**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[39:32]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[39:32]	7:0	See description of '110412h'.	
0Bh (110417h)	**REG110417**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[47:40]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[47:40]	7:0	See description of '110412h'.	
0Ch (110418h)	**REG110418**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[55:48]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[55:48]	7:0	See description of '110412h'.	
0Ch	**REG110419**	**7:0**	**Default : 0x00**	**Access : RO, WO**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110419h)	STS_MPIF_LC3A_DATA[63:56]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[63:56]	7:0	See description of '110412h'.	
0Dh (11041Ah)	**REG11041A**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[71:64]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[71:64]	7:0	See description of '110412h'.	
0Dh (11041Bh)	**REG11041B**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[79:72]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[79:72]	7:0	See description of '110412h'.	
0Eh (11041Ch)	**REG11041C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[87:80]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[87:80]	7:0	See description of '110412h'.	
0Eh (11041Dh)	**REG11041D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[95:88]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[95:88]	7:0	See description of '110412h'.	
0Fh (11041Eh)	**REG11041E**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[103:96]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[103:96]	7:0	See description of '110412h'.	
0Fh (11041Fh)	**REG11041F**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[111:104]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[111:104]	7:0	See description of '110412h'.	
10h (110420h)	**REG110420**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[119:112]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[119:112]	7:0	See description of '110412h'.	
10h (110421h)	**REG110421**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[127:120]	7:0	See description of '110412h'.	
	MPIF_LC3A_DATA[127:120]	7:0	See description of '110412h'.	
11h (110422h)	**REG110422**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_MADR[7:0]	7:0	MPIF Logical Channel 3a data to/from MIU base address.	
11h (110423h)	**REG110423**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_MADR[15:8]	7:0	See description of '110422h'.	
12h (110424h)	**REG110424**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_MADR[23:16]	7:0	See description of '110422h'.	
12h	**REG110425**	**7:0**	**Default : 0x00**	**Access : R/W**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110425h)	MPIF_LC3A_MADR[31:24]	7:0	See description of '110422h'.	
13h (110426h)	**REG110426**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 times. 2: 2 times. 3: 3 times.	
	MPIF_LC3B_RETRX	5	MPIF Logical Channel 3b re-transmit/receive packet indicator.	
	MPIF_LC3B_CHK	4	MPIF Logical Channel 3b check enable.	
	MPIF_LC3B_SID[1:0]	3:2	MPIF Logical Channel 3b Slave ID.	
	MPIF_LC3B_RW	1	MPIF Logical Channel 3b read/write.	
	MPIF_LC3B_VLD	0	MPIF Logical Channel 3b valid.	
13h (110427h)	**REG110427**	**7:0**	**Default : 0x40**	**Access : R/W**
	MPIF_LC3B_WCNT[3:0]	7:4	MPIF Logical Channel 3b max wait number.	
	MPIF_LC3B_RX_NWMIU	3	MPIF Logical Channel 3b not wait miu done.	
	MPIF_LC3B_FMODE	2	MPIF Logical Channel 3b fast read/write mode.	
	MPIF_LC3B_MIUSEL	1	MPIF Logical Channel 3b MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_LC3B_SRC	0	MPIF Logical Channel 3b source/destination selection. 0: To/from RIU. 1: To/from MIU.	
14h (110428h)	**REG110428**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_PKTLEN[7:0]	7:0	MPIF Logical Channel 3b packet total length.	
14h (110429h)	**REG110429**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_PKTLEN[15:8]	7:0	See description of '110428h'.	
15h (11042Ah)	**REG11042A**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[7:0]	7:0	MPIF Logical Channel 3b data/ SPI data for RIU path.	
	MPIF_LC3B_DATA[7:0]	7:0	MPIF Logical Channel 3b data/ SPI data for RIU path.	
15h (11042Bh)	**REG11042B**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[15:8]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[15:8]	7:0	See description of '11042Ah'.	

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (11042Ch)	**REG11042C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[23:16]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[23:16]	7:0	See description of '11042Ah'.	
16h (11042Dh)	**REG11042D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[31:24]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[31:24]	7:0	See description of '11042Ah'.	
17h (11042Eh)	**REG11042E**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[39:32]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[39:32]	7:0	See description of '11042Ah'.	
17h (11042Fh)	**REG11042F**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[47:40]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[47:40]	7:0	See description of '11042Ah'.	
18h (110430h)	**REG110430**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[55:48]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[55:48]	7:0	See description of '11042Ah'.	
18h (110431h)	**REG110431**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[63:56]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[63:56]	7:0	See description of '11042Ah'.	
19h (110432h)	**REG110432**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[71:64]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[71:64]	7:0	See description of '11042Ah'.	
19h (110433h)	**REG110433**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[79:72]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[79:72]	7:0	See description of '11042Ah'.	
1Ah (110434h)	**REG110434**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[87:80]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[87:80]	7:0	See description of '11042Ah'.	
1Ah (110435h)	**REG110435**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[95:88]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[95:88]	7:0	See description of '11042Ah'.	
1Bh (110436h)	**REG110436**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[103:96]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[103:96]	7:0	See description of '11042Ah'.	

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Bh (110437h)	**REG110437**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[111:104]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[111:104]	7:0	See description of '11042Ah'.	
1Ch (110438h)	**REG110438**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[119:112]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[119:112]	7:0	See description of '11042Ah'.	
1Ch (110439h)	**REG110439**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[127:120]	7:0	See description of '11042Ah'.	
	MPIF_LC3B_DATA[127:120]	7:0	See description of '11042Ah'.	
1Dh (11043Ah)	**REG11043A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[7:0]	7:0	MPIF Logical Channel 3b data to/from MIU base address.	
1Dh (11043Bh)	**REG11043B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[15:8]	7:0	See description of '11043Ah'.	
1Eh (11043Ch)	**REG11043C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[23:16]	7:0	See description of '11043Ah'.	
1Eh (11043Dh)	**REG11043D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[31:24]	7:0	See description of '11043Ah'.	
1Fh (11043Eh)	**REG11043E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 times. 2: 2 times. 3: 3 times.	
	-	5:4	Reserved.	
	MPIF_LC4A_SID[1:0]	3:2	MPIF Logical Channel 4a Slave ID.	
	MPIF_LC4A_RW	1	MPIF Logical Channel 4a read/write.	
	MPIF_LC4A_VLD	0	MPIF Logical Channel 4a valid.	
1Fh (11043Fh)	**REG11043F**	**7:0**	**Default : 0x80**	**Access : R/W**
	MPIF_LC4A_WCNT[3:0]	7:4	MPIF Logical Channel 4a max wait number.	
	MPIF_LC4A_GRANULAR[1:0]	3:2	MPIF Logical Channel 4a breakpoint. 00: 1x256 bytes. 01: 2x256 bytes. 10: 3x256 bytes. 11: 4x256 bytes.	

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MPIF_LC4A_MIUSEL	1	MPIF Logical Channel 4a MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_LC4A_RX_NWMIU	0	MPIF Logical Channel 4a not wait miu done.	
20h (110440h)	**REG110440**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_STMLEN[7:0]	7:0	MPIF Logical Channel 4a stream total length (byte unit).	
20h (110441h)	**REG110441**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_STMLEN[15:8]	7:0	See description of '110440h'.	
21h (110442h)	**REG110442**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[7:0]	7:0	MPIF Logical Channel 4a data to/from MIU base address.	
21h (110443h)	**REG110443**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[15:8]	7:0	See description of '110442h'.	
22h (110444h)	**REG110444**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[23:16]	7:0	See description of '110442h'.	
22h (110445h)	**REG110445**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[31:24]	7:0	See description of '110442h'.	
23h (110446h)	**REG110446**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MPIF_4WSPI_DUPLEX	2	MPIF 4-wire SPI duplex enable. Note: Only valid for read command.	
	MPIF_4WSPI_RW	1	MPIF 4-wire SPI read/write.	
	MPIF_4WSPI_VLD	0	MPIF 4-wire SPI valid.	
24h (110448h)	**REG110448**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MPIF_3WSPI_RW	1	MPIF 3-wire SPI read/write.	
	MPIF_3WSPI_VLD	0	MPIF 3-wire SPI valid.	
25h (11044Ah)	**REG11044A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_TT[1:0]	7:6	MPIF SPI trailing cycle.	
	MPIF_SPI_TL[1:0]	5:4	MPIF SPI leading cycle.	
	MPIF_SPI_CPOL	3	MPIF SPI clock polarity.	
	MPIF_SPI_CPHA	2	MPIF SPI clock phase.	
	MPIF_SPI_SID[1:0]	1:0	MPIF SPI Slave ID.	
25h	**REG11044B**	**7:0**	**Default : 0x01**	**Access : R/W**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11044Bh)	-	7	Reserved.	
	MPIF_SPI_RX_NWMIU	6	MPIF SPI not wait miu done.	
	MPIF_SPI_SEP_IO	5	MPIF SPI separate IO mode.	
	MPIF_SPI_MIUSEL	4	MPIF SPI MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_SPI_SRC	3	MPIF SPI source/destination selection. 0: To/from RIU. 1: To/from MIU.	
	MPIF_SPI_CMD_LEN[2:0]	2:0	MPIF SPI command length. "000" - 0 byte. "001" - 1 bytes. "010" - 2 bytes. "011" - 3 bytes. "100" - 4 bytes. "101" - 5 bytes. "110" - 6 bytes. "111" - 7 bytes.	
26h (11044Ch)	**REG11044C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[7:0]	7:0	MPIF SPI command value.	
26h (11044Dh)	**REG11044D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[15:8]	7:0	See description of '11044Ch'.	
27h (11044Eh)	**REG11044E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[23:16]	7:0	See description of '11044Ch'.	
27h (11044Fh)	**REG11044F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[31:24]	7:0	See description of '11044Ch'.	
28h (110450h)	**REG110450**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_DAT_LEN[7:0]	7:0	MPIF SPI data total length (byte unit).	
28h (110451h)	**REG110451**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_DAT_LEN[15:8]	7:0	See description of '110450h'.	
29h (110452h)	**REG110452**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_MADR[7:0]	7:0	MPIF SPI MIU base address.	
29h (110453h)	**REG110453**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_MADR[15:8]	7:0	See description of '110452h'.	
2Ah	**REG110454**	**7:0**	**Default : 0x00**	**Access : R/W**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110454h)	MPIF_SPI_MADR[23:16]	7:0	See description of '110452h'.	
2Ah (110455h)	**REG110455**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_MADR[31:24]	7:0	See description of '110452h'.	
2Bh (110456h)	**REG110456**	**7:0**	**Default : 0x00**	**Access : RO**
	MPIF_LC4A_BUSY	7	MPIF Logical Channel 4a busy flag.	
	MPIF_LC3B_BUSY	6	MPIF Logical Channel 3b busy flag.	
	MPIF_LC3A_BUSY	5	MPIF Logical Channel 3a busy flag.	
	MPIF_LC2B_BUSY	4	MPIF Logical Channel 2b busy flag.	
	MPIF_LC2A_BUSY	3	MPIF Logical Channel 2a busy flag.	
	MPIF_LC1A_BUSY	2	MPIF Logical Channel 1a busy flag.	
	MPIF_3WSPI_BUSY	1	MPIF 3-wire SPI busy flag.	
	MPIF_4WSPI_BUSY	0	MPIF 4-wire SPI busy flag.	
2Ch (110458h)	**REG110458**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_INT_ENABLE[7:0]	7:0	MPIF Interrupt event enable. [0]: 4-wire SPI trx done. [1]: 3-wire SPI trx done. [2]: Logical Channel 1a trx done. [3]: Logical Channel 2a trx done. [4]: Logical Channel 2b trx done. [5]: Logical Channel 3a trx done. [6]: Logical Channel 3b trx done. [7]: Logical Channel 4a trx done. [8]: Logical Channel 2a trx error. [9]: Logical Channel 2b trx error. [10]: Logical Channel 3a trx error. [11]: Logical Channel 3b trx error. [12]: Logical Channel 4a trx error. [13]: Busy time out. [14]: Slave request.	
2Ch (110459h)	**REG110459**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MPIF_INT_ENABLE[14:8]	6:0	See description of '110458h'.	
2Dh (11045Ah)	**REG11045A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_DONE	7	Logical Channel 4a trx done.	
	MPIF_LC3B_DONE	6	Logical Channel 3b trx done.	
	MPIF_LC3A_DONE	5	Logical Channel 3a trx done.	

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MPIF_LC2B_DONE	4	Logical Channel 2b trx done.	
	MPIF_LC2A_DONE	3	Logical Channel 2a trx done.	
	MPIF_LC1A_DONE	2	Logical Channel 1a trx done.	
	MPIF_3WSPI_DONE	1	3-wire SPI trx done.	
	MPIF_4WSPI_DONE	0	4-wire SPI trx done.	
2Dh (11045Bh)	**REG11045B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	MPIF_SLAVE_REQ	6	Slave request.	
	MPIF_BUSY_TIMEOUT	5	MPIF busy time out.	
	MPIF_LC4A_ERR	4	Logical Channel 4a trx error.	
	MPIF_LC3B_ERR	3	Logical Channel 3b trx error.	
	MPIF_LC3A_ERR	2	Logical Channel 3a trx error.	
	MPIF_LC2B_ERR	1	Logical Channel 2b trx error.	
	MPIF_LC2A_ERR	0	Logical Channel 2a trx error.	
2Eh (11045Ch)	**REG11045C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_TIMEOUT[7:0]	7:0	MPIF wait time limit for busy de-assert.	
2Eh (11045Dh)	**REG11045D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_TIMEOUT[15:8]	7:0	See description of '11045Ch'.	
2Fh	**REG11045E**	**7:0**	**Default : 0x00**	**Access : RO**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11045Eh)	STS_BUSY_TO[7:0]	7:0	Busy time out status. [4:0]: command id. "00000" - MPIF_1A_R. "00001" - MPIF_1A_W. "00010" - MPIF_2A_R. "00011" - MPIF_2A_W. "00100" - MPIF_2A_RC. "00101" - MPIF_2A_WC. "00110" - MPIF_2B_R. "00111" - MPIF_2B_W. "01000" - MPIF_2B_RC. "01001" - MPIF_2B_WC. "01010" - MPIF_3A_R. "01011" - MPIF_3A_W. "01100" - MPIF_3A_RC. "01101" - MPIF_3A_WC. "01110" - MPIF_3B_R. "01111" - MPIF_3B_W. "10000" - MPIF_3B_RC. "10001" - MPIF_3B_WC. "10010" - MPIF_4A_R. "10011" - MPIF_4A_W. [9:8]: slave id.	
2Fh (11045Fh)	**REG11045F**	**7:0**	**Default : 0x00**	**Access : RO**
	STS_BUSY_TO[15:8]	7:0	See description of '11045Eh'.	
30h (110460h)	**REG110460**	**7:0**	**Default : 0x01**	**Access : R/W**
	MPIF_SLV0_DW[1:0]	7:6	Slave 0 data width. 0: 1. 1: 2. 2: 4. 3: 8.	
	MPIF_WAIT_CYCLE[1:0]	5:4	MPIF wait ACK/NAK cycle. 0: 0T. 1: 1T. 2: 2T. 3: 3T.	

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MPIF_TR_CYCLE[1:0]	3:2	MPIF read/write turn around cycle (MSB=h31.[3]). 0: 0T. 1: 1T. 2: 2T. 3: 3T. 4: 4T. 5: 5T. 6: 6T. 7: 7T.	
	-	1	Reserved.	
	MPIF_SWRSTN	0	MPIF software reset, active low.	
30h (110461h)	**REG110461**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_CMD_DW[1:0]	7:6	Slave 3 data width. 0: 1. 1: 2. 2: 4. 3: 8.	
	MPIF_SLV3_DW[1:0]	5:4	Slave 3 data width. 0: 1. 1: 2. 2: 4. 3: 8.	
	MPIF_SLV2_DW[1:0]	3:2	Slave 2 data width. 0: 1. 1: 2. 2: 4. 3: 8.	
	MPIF_SLV1_DW[1:0]	1:0	Slave 1 data width. 0: 1. 1: 2. 2: 4. 3: 8.	
31h (110462h)	**REG110462**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR_LC4X_ERRCNT	7	Clear Logical Channel 4A error counter.	
	CLR_LC3X_ERRCNT	6	Clear Logical Channel 3A/3B error counter.	
	CLR_LC2X_ERRCNT	5	Clear Logical Channel 2A/2B error counter.	
	-	4	Reserved.	

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MPIF_TR_CYCLE_B2	3	MPIF read/write turn around cycle MSB bit.	
	MPIF_WWTR_CYCLE[2:0]	2:0	MPIF write/write turn around cycle for LC3A/LC3B/LC4A. 0: 0T. 1: 1T. 2: 2T. 3: 3T. 4: 4T. 5: 5T. 6: 6T. 7: 7T.	
31h (110463h)	**REG110463**	**7:0**	**Default : 0x04**	**Access : R/W**
	LC3X_NOCHK_TOG_EN	7	Enable LC3X_NOCHK toggle bit enable.	
	MPIF_EXTRDCMD_CYCLE[2:0]	6:4	MPIF RX command state extend cycle.	
	-	3	Reserved.	
	MPIF_MIU_W4WLAST_DONE	2	MPIF_MIU_W4WLAST_DONE.	
	MPIF_MIU_PRI1	1	MPIF MIU interface 1 priority.	
	MPIF_MIU_PRI0	0	MPIF MIU interface 0 priority.	
32h (110464h)	**REG110464**	**7:0**	**Default : 0x40**	**Access : R/W**
	CLK_DLY[3:0]	7:4	PIF_CLK delay selection.	
	MPIF_BYPASS_DLY	3	MPIF Bypass delay chain.	
	MPIF_BSY_SYNC_EN	2	MPIF Busy Sync Enable.	
	SYNC_8B	1	MPIF RX via Feedback path sync boundary. 0: 4 byte boundary. 1: 8 byte boundary.	
	RX_FB_ON	0	MPIF RX via Feedback path.	
32h (110465h)	**REG110465**	**7:0**	**Default : 0x44**	**Access : R/W**
	DI0_DLY[3:0]	7:4	PIF_DI0 delay selection.	
	CSN_DLY[3:0]	3:0	PIF_CSN delay selection.	
33h (110466h)	**REG110466**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MPIF_SYNC_LEN[2:0]	2:0	MPIF Sync pattern length. 0: 1 bit. .. 7: 8 bits.	
33h	**REG110467**	**7:0**	**Default : 0x55**	**Access : R/W**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110467h)	MPIF_SYNC_PAT[7:0]	7:0	MPIF Sync pattern, LSB first.	
34h (110468h)	**REG110468**	**7:0**	**Default : 0x00**	**Access : RO**
	STS_SPI_UCPLT_TRX_LEN[7:0]	7:0	MPIF SPI transmit/receive un-complete data length.	
34h (110469h)	**REG110469**	**7:0**	**Default : 0x00**	**Access : RO**
	STS_SPI_UCPLT_TRX_LEN[15:8]	7:0	See description of '110468h'.	
35h (11046Ah)	**REG11046A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MPIF_DUMMY_WR_LEN	3	MPIF MIU dummy write length. 0: 2. 1: 4.	
	MPIF_DUMMY_WRITE_EN	2	MPIF MIU dummy write enable.	
	MPIF_MIUWR_CLR_OB	1	Clear MIU write out of range status.	
	MPIF_MIU_MASK_WR	0	MPIF MIU write request mask.	
35h (11046Bh)	**REG11046B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	STS_MIUWR_OB	0	MPIF MIU write address out of range.	
36h (11046Ch)	**REG11046C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[7:0]	7:0	MPIF MIU write address lower bound.	
36h (11046Dh)	**REG11046D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[15:8]	7:0	See description of '11046Ch'.	
37h (11046Eh)	**REG11046E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[23:16]	7:0	See description of '11046Ch'.	
37h (11046Fh)	**REG11046F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[31:24]	7:0	See description of '11046Ch'.	
38h (110470h)	**REG110470**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[7:0]	7:0	MPIF MIU write address upper bound.	
38h (110471h)	**REG110471**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[15:8]	7:0	See description of '110470h'.	
39h (110472h)	**REG110472**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[23:16]	7:0	See description of '110470h'.	
39h (110473h)	**REG110473**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[31:24]	7:0	See description of '110470h'.	
3Ah	**REG110474**	**7:0**	**Default : 0x00**	**Access : R/W**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110474h)	MPIF_D_GPO[3:0]	7:4	MPIF data pins uased as GPO value.	
	MPIF_D_GPO_EN[3:0]	3:0	MPIF data pins uased as GPO enable.	
3Ah (110475h)	**REG110475**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_CS_GPO[3:0]	7:4	MPIF cs pins uased as GPO value.	
	MPIF_CS_GPO_EN[3:0]	3:0	MPIF cs pins uased as GPO enable.	
3Bh (110476h)	**REG110476**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MPIF_THROTTLE_SIZE[1:0]	5:4	MPIF clock throttle boundary in data phase. 0: 4 bytes boundary. 1: 8 bytes boundary. 2: 16 bytes boundary. 3: 32 bytes boundary.	
	-	3:2	Reserved.	
	MPIF_THROTTLE_RATE[1:0]	1:0	MPIF clock throttle rate. 0: 0 cycle. 1: 1 cycle. 2: 2 cycle. 3: 3 cycle.	
3Eh (11047Ch)	**REG11047C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPARE[7:0]	7:0	MPIF spare registers.	
3Eh (11047Dh)	**REG11047D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPARE[15:8]	7:0	See description of '11047Ch'.	
3Fh (11047Eh)	**REG11047E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_SPARE[23:16]	7:0	See description of '11047Ch'.	
3Fh (11047Fh)	**REG11047F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_SPARE[31:24]	7:0	See description of '11047Ch'.	
40h (110480h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
41h ~ 4Bh (110482h ~ 110496h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
4Ch (110498h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
4Dh	**-**	**7:0**	**Default : -**	**Access : -**

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MPIF Register (Bank = 1104)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11049Ah)	-	-	Reserved.	
4Eh (11049Ch)	**REG11049C**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7	Reserved.	
	MPIF_DYNAMIC_CLK_MIU_EN	6	MPIF dynamic clk_miu gating enable.	
	MPIF_DYNAMIC_CLK_MPIF_EN	5	MPIF dynamic clk_mpif gating enable.	
	MPIF_DYNAMIC_GATE_EN	4	MPIF dynamic clock gating enable.	
	CLK_MPIF_SRC_DLY[2:0]	3:1	Clk_mpif delay selection.	
	CLK_MPIF_SRC_BYPASS_DLY	0	Bypass clk_mpif delay.	

UART1 Register (Bank = 1106)

UART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (110600h)	**REG110600**	**7:0**	**Default : 0x00**	**Access : R/W**
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; Note that Writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; Note that any incoming data are lost whenFIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h	**REG110604**	**7:0**	**Default : 0x00**	**Access : R/W**

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UART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110604h)	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Boud rate = (serial clock freq.) / (16 * divisor).	
04h	**REG110608**	**7:0**	**Default : 0x00**	**Access : R/W**
(110608h)	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00" - FIFO empty; "01" - 2 characters in the FIFO; "10" - FIFO 1/4 full; "11" - FIFO 1/2 full; Bit [7:6]: Receiver FIFO Interrupt trigger level. "00" - 1 character in the FIFO; "01" - FIFO 1/4 full; "10" - FIFO 1/2 full; "11" - FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt idenfy. "110" - character timeout. "011" - Receiver Line Status. "010" - Receiver Data Available. "001" - Transmitter Holding Register empty. "000" - Modem Status.	

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UART1 Register (Bank = 1106)

Index (Absolute)	Mnemonic	Bit	Description	
06h (11060Ch)	**REG11060C**	**7:0**	**Default : 0x03**	**Access : R/W**
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.	
	-	6:5	Reserved.	
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.	
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.	
	LCR_STOP_BITS	2	Specify the number of stop bits. "0" - 1 stop bit; "1" - 1.5 stop bits when 5-bit character length selected and 2 bits otherwise.	
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00" - 5 bits; "01" - 6 bits; "10" - 7 bits; "11" - 8 bits.	
08h (110610h)	**REG110610**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN. RTS-> CTS.	
	-	3:2	Reserved.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0" - RTS is "1"; "1" - RTS is "0".	
	-	0	Reserved.	
0Ah (110614h)	**REG110614**	**7:0**	**Default : 0x00**	**Access : RO**
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO;	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO; Gen a Transmitter Holding Register Empty interrupt.	
	-	4	Reserved.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	

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UART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (110618h)	**REG110618**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	-	3:1	Reserved.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1" - the "CTS" line has changed its state. Clear when reading;	
0Eh (11061Ch)	**REG11061C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	USR_BUSY	0	UART busy.	
14h (110628h)	**REG110628**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RSTZ	0	Software reset UART; 0: enable.	

UART2 Register (Bank = 1106)

UART2 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (110640h)	**REG110640**	**7:0**	**Default : 0x00**	**Access : R/W**
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; Note that Writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; Note that any incoming data are lost whenFIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
22h	**REG110644**	**7:0**	**Default : 0x00**	**Access : R/W**

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UART2 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110644h)	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Boud rate = (serial clock freq.) / (16 * divisor).	
24h	**REG110648**	**7:0**	**Default : 0x00**	**Access : R/W**
(110648h)	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00" - FIFO empty; "01" - 2 characters in the FIFO; "10" - FIFO 1/4 full; "11" - FIFO 1/2 full; Bit [7:6]: Receiver FIFO Interrupt trigger level. "00" - 1 character in the FIFO; "01" - FIFO 1/4 full; "10" - FIFO 1/2 full; "11" - FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt idenfy. "110" - character timeout. "011" - Receiver Line Status. "010" - Receiver Data Available. "001" - Transmitter Holding Register empty. "000" - Modem Status.	

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UART2 Register (Bank = 1106)

Index (Absolute)	Mnemonic	Bit	Description	
26h (11064Ch)	**REG11064C**	**7:0**	**Default : 0x03**	**Access : R/W**
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.	
	-	6:5	Reserved.	
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.	
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.	
	LCR_STOP_BITS	2	Specify the number of stop bits. "0" - 1 stop bit; "1" - 1.5 stop bits when 5-bit character length selected and 2 bits otherwise.	
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00" - 5 bits; "01" - 6 bits; "10" - 7 bits; "11" - 8 bits.	
28h (110650h)	**REG110650**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN. RTS-> CTS.	
	-	3:2	Reserved.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0" - RTS is "1"; "1" - RTS is "0".	
	-	0	Reserved.	
2Ah (110654h)	**REG110654**	**7:0**	**Default : 0x00**	**Access : RO**
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO;	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO; Gen a Transmitter Holding Register Empty interrupt.	
	-	4	Reserved.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	

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UART2 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
2Ch (110658h)	**REG110658**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	-	3:1	Reserved.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1" - the "CTS" line has changed its state. Clear when reading;	
2Eh (11065Ch)	**REG11065C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	USR_BUSY	0	UART busy.	
34h (110668h)	**REG110668**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RSTZ	0	Software reset UART; 0: enable.	

FUART Register (Bank = 1106)

FUART Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (110680h)	**REG110680**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_SW_RST	7	RX Engine software reset. 0: De-assert. 1: Assert.	
	TX_SW_RST	6	TX Engine software reset. 0: De-assert. 1: Assert.	
	RX_ENDINA	5	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	TX_ENDINA	4	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	

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FUART Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RX_URDMA_EN	3	URDMA RX Hardware Enable. 0: Disable. 1: Enable.	
	TX_URDMA_EN	2	URDMA TX Hardware Enable. 0: Disable. 1: Enable.	
	URDMA_MODE	1	URDMA Mode selects, when mode enable, URDMA hardware will replace MCU to access UART, otherwise MCU still control UART directly. 0: Disable. 1: Enable.	
	SW_RST	0	URDMA software reset. 0: De-assert. 1: Assert.	
40h (110681h)	**REG110681**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	RX_BUSY	5	RX controller in BUSY state.	
	TX_BUSY	4	TX controller in BUSY state.	
	RX_OP_MODE	3	RX controller operation mode. 0: Default. 1: Stop RX DMA activity when threshold interrupt occurs, until update RX_BUF_BASE.	
	-	2:0	Reserved.	
41h (110682h)	**REG110682**	**7:0**	**Default : 0x40**	**Access : R/W**
	INTR_THRESHOLD[7:0]	7:0	Interrupt threshold, to configure interrupt MCU period. Setting how much. Data received from UART, and alert MCU, byte unit.	
41h (110683h)	**REG110683**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INTR_THRESHOLD[11:8]	3:0	See description of '110682h'.	
42h (110684h)	**REG110684**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_H[7:0]	7:0	Configure TX buffer base address[26:16] in DRAM, 8byte unit.	
42h (110685h)	**REG110685**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TX_BUF_BASE_H[10:8]	2:0	See description of '110684h'.	

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FUART Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (110686h)	**REG110686**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[7:0]	7:0	Configure TX buffer base address[15:0] in DRAM, 8byte unit.	
43h (110687h)	**REG110687**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[15:8]	7:0	See description of '110686h'.	
44h (110688h)	**REG110688**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_SIZE[7:0]	7:0	Configure TX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
44h (110689h)	**REG110689**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TX_BUF_SIZE[12:8]	4:0	See description of '110688h'.	
45h (11068Ah)	**REG11068A**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[7:0]	7:0	Read TX buffer read pointer from URDMA, byte unit.	
45h (11068Bh)	**REG11068B**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[15:8]	7:0	See description of '11068Ah'.	
46h (11068Ch)	**REG11068C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[7:0]	7:0	Update TX buffer write pointer to URDMA, byte unit.	
46h (11068Dh)	**REG11068D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[15:8]	7:0	See description of '11068Ch'.	
47h (11068Eh)	**REG11068E**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	TX_TIMEOUT[3:0]	3:0	Configure TX time out value, to clean TX buffer data and send to UART. 2^(TX_TIMEOUT) Cycle unit.	
48h (110690h)	**REG110690**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_H[7:0]	7:0	Configure RX buffer base address[26:16] in DRAM, 8byte unit.	
48h (110691h)	**REG110691**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RX_BUF_BASE_H[10:8]	2:0	See description of '110690h'.	
49h (110692h)	**REG110692**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[7:0]	7:0	Configure RX buffer base address[15:0] in DRAM, 8byte unit.	

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FUART Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
49h (110693h)	**REG110693**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[15:8]	7:0	See description of '110692h'.	
4Ah (110694h)	**REG110694**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_SIZE[7:0]	7:0	Configure RX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
4Ah (110695h)	**REG110695**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RX_BUF_SIZE[12:8]	4:0	See description of '110694h'.	
4Bh (110696h)	**REG110696**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[7:0]	7:0	Read RX buffer write pointer from URDMA, byte unit.	
4Bh (110697h)	**REG110697**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[15:8]	7:0	See description of '110696h'.	
4Ch (110698h)	**REG110698**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	RX_TIMEOUT[3:0]	3:0	Configure RX time out value, to clean UART RX FIFO and write to DRAM. 2^(RX_TIMEOUT) Cycle unit.	
4Dh (11069Ah)	**REG11069A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RX_MCU_INTR	7	Identify rx controller to MCU interrupt event, this bit is logical OR of RX_INTR1~2 flag, and clear by RX_INTR_CLR.	
	RESERVE2	6	Reserve.	
	RX_INTR2	5	Identify Rx interrupt is cause by interrupt threshold function.	
	RX_INTR1	4	Identify Rx interrupt is cause by timeout function.	
	RESERVE1	3	Reserve.	
	RX_INTR2_EN	2	Rx interrupt threshold function enable.	
	RX_INTR1_EN	1	Rx timeout interrupt function enable.	
	RX_INTR_CLR	0	MCU clear rx control interrupt signal. Once write and auto clear.	
4Dh (11069Bh)	**REG11069B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TX_MCU_INTR	7	Identify tx controller to MCU interrupt event.	
	RESERVE3[4:0]	6:2	Reserve.	
	TX_INTR_EN	1	TX controller to MCU interrupt enable.	

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FUART Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_INTR_CLR	0	MCU clear tx control interrupt signal. Once write and auto clear.	
4Eh (11069Ch)	**REG11069C**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[7:0]	7:0	Reserve.	
4Eh (11069Dh)	**REG11069D**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[15:8]	7:0	See description of '11069Ch'.	
4Fh (11069Eh)	**REG11069E**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[7:0]	7:0	Reserve.	
4Fh (11069Fh)	**REG11069F**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[15:8]	7:0	See description of '11069Eh'.	
50h (1106A0h)	**REG1106A0**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	RESERVE6[4:0]	7:3	Reserve.	
	PREFCH_CLK_GATE1	2	Gated clock MINF post-write module. 0: Clock enable. 1: Clock gated.	
	PREFCH_CLK_GATE	1	Gated clock MINF pre-fetch module. 0: Clock enable. 1: Clock gated.	
	MINF_SW_RSTZ	0	MINF pre-fetch / post-write module SW reset. 0: SW reset. 1: Normal.	
50h (1106A1h)	**REG1106A1**	**7:0**	**Default : 0x00**	**Access : RO**
	POSTWR_BUSY	7	Identify MINF post write in busy state.	
	RESERVE6[11:5]	6:0	See description of '1106A0h'.	
51h (1106A2h)	**REG1106A2**	**7:0**	**Default : 0x46**	**Access : R/W**
	PREFCH_PATCH	7	SW patch control bit.	
	PREFCH_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	PREFCH_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	PREFCH_PRI	3	Define DRAM access priority.	

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FUART Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PREFCH_RASTRD	2	MINF pre-fetch fast read enable.	
	PREFCH_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	PREFCH_CLR	0	SW clear MINF pre-fetch buffer. 0: Normal. 1: Clear.	
51h (1106A3h)	**REG1106A3**	**7:0**	**Default : 0x46**	**Access : R/W**
	POSTWR_FLUSH1_PATCH	7	SW flush path.	
	POSTWR_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	POSEWR_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	POSTWR_PRI	3	Define DRAM access priority.	
	POSTWR_FLUSH1	2	SW flush path.	
	POSTWR_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	POSTWR_FLUSH	0	SW flush MINF post write buffer. 0: Normal. 1: Flush.	

FUART1 Register (Bank = 1106)

FUART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (1106C0h)	**REG1106C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_SW_RST	7	RX Engine software reset. 0: De-assert. 1: Assert.	

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FUART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_SW_RST	6	TX Engine software reset. 0: De-assert. 1: Assert.	
	RX_ENDINA	5	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	TX_ENDINA	4	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	RX_URDMA_EN	3	URDMA RX Hardware Enable. 0: Disable. 1: Enable.	
	TX_URDMA_EN	2	URDMA TX Hardware Enable. 0: Disable. 1: Enable.	
	URDMA_MODE	1	URDMA Mode selects, when mode enable, URDMA hardware will replace MCU to access UART, otherwise MCU still control UART directly. 0: Disable. 1: Enable.	
	SW_RST	0	URDMA software reset. 0: De-assert. 1: Assert.	
60h (1106C1h)	**REG1106C1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	RX_BUSY	5	RX controller in BUSY state.	
	TX_BUSY	4	TX controller in BUSY state.	
	RX_OP_MODE	3	RX controller operation mode. 0: Default. 1: Stop RX DMA activity when threshold interrupt occurs, until update RX_BUF_BASE.	
	-	2:0	Reserved.	
61h (1106C2h)	**REG1106C2**	**7:0**	**Default : 0x40**	**Access : R/W**
	INTR_THRESHOLD[7:0]	7:0	Interrupt threshold, to configure interrupt MCU period. Setting how much. Data received from UART, and alert MCU, byte unit.	
61h	**REG1106C3**	**7:0**	**Default : 0x00**	**Access : R/W**

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FUART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1106C3h)	-	7:4	Reserved.	
	INTR_THRESHOLD[11:8]	3:0	See description of '1106C2h'.	
62h (1106C4h)	**REG1106C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_H[7:0]	7:0	Configure TX buffer base address[26:16] in DRAM, 8byte unit.	
62h (1106C5h)	**REG1106C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TX_BUF_BASE_H[10:8]	2:0	See description of '1106C4h'.	
63h (1106C6h)	**REG1106C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[7:0]	7:0	Configure TX buffer base address[15:0] in DRAM, 8byte unit.	
63h (1106C7h)	**REG1106C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[15:8]	7:0	See description of '1106C6h'.	
64h (1106C8h)	**REG1106C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_SIZE[7:0]	7:0	Configure TX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
64h (1106C9h)	**REG1106C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TX_BUF_SIZE[12:8]	4:0	See description of '1106C8h'.	
65h (1106CAh)	**REG1106CA**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[7:0]	7:0	Read TX buffer read pointer from URDMA, byte unit.	
65h (1106CBh)	**REG1106CB**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[15:8]	7:0	See description of '1106CAh'.	
66h (1106CCh)	**REG1106CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[7:0]	7:0	Update TX buffer write pointer to URDMA, byte unit.	
66h (1106CDh)	**REG1106CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[15:8]	7:0	See description of '1106CCh'.	
67h (1106CEh)	**REG1106CE**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	TX_TIMEOUT[3:0]	3:0	Configure TX time out value, to clean TX buffer data and send to UART. 2^(TX_TIMEOUT) Cycle unit.	
68h	**REG1106D0**	**7:0**	**Default : 0x00**	**Access : R/W**

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FUART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1106D0h)	RX_BUF_BASE_H[7:0]	7:0	Configure RX buffer base address[26:16] in DRAM, 8byte unit.	
68h (1106D1h)	**REG1106D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RX_BUF_BASE_H[10:8]	2:0	See description of '1106D0h'.	
69h (1106D2h)	**REG1106D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[7:0]	7:0	Configure RX buffer base address[15:0] in DRAM, 8byte unit.	
69h (1106D3h)	**REG1106D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[15:8]	7:0	See description of '1106D2h'.	
6Ah (1106D4h)	**REG1106D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_SIZE[7:0]	7:0	Configure RX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
6Ah (1106D5h)	**REG1106D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RX_BUF_SIZE[12:8]	4:0	See description of '1106D4h'.	
6Bh (1106D6h)	**REG1106D6**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[7:0]	7:0	Read RX buffer write pointer from URDMA, byte unit.	
6Bh (1106D7h)	**REG1106D7**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[15:8]	7:0	See description of '1106D6h'.	
6Ch (1106D8h)	**REG1106D8**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	RX_TIMEOUT[3:0]	3:0	Configure RX time out value, to clean UART RX FIFO and write to DRAM. 2^(RX_TIMEOUT) Cycle unit.	
6Dh (1106DAh)	**REG1106DA**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RX_MCU_INTR	7	Identify rx controller to MCU interrupt event, this bit is logical OR of RX_INTR1~2 flag, and clear by RX_INTR_CLR.	
	RESERVE2	6	Reserve.	
	RX_INTR2	5	Identify Rx interrupt is cause by interrupt threshold function.	
	RX_INTR1	4	Identify Rx interrupt is cause by timeout function.	

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FUART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RESERVE1	3	Reserve.	
	RX_INTR2_EN	2	Rx interrupt threshold function enable.	
	RX_INTR1_EN	1	Rx timeout interrupt function enable.	
	RX_INTR_CLR	0	MCU clear rx control interrupt signal. Once write and auto clear.	
6Dh (1106DBh)	**REG1106DB**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TX_MCU_INTR	7	Identify tx controller to MCU interrupt event.	
	RESERVE3[4:0]	6:2	Reserve.	
	TX_INTR_EN	1	TX controller to MCU interrupt enable.	
	TX_INTR_CLR	0	MCU clear tx control interrupt signal. Once write and auto clear.	
6Eh (1106DCh)	**REG1106DC**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[7:0]	7:0	Reserve.	
6Eh (1106DDh)	**REG1106DD**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[15:8]	7:0	See description of '1106DCh'.	
6Fh (1106DEh)	**REG1106DE**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[7:0]	7:0	Reserve.	
6Fh (1106DFh)	**REG1106DF**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[15:8]	7:0	See description of '1106DEh'.	
70h (1106E0h)	**REG1106E0**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	RESERVE6[4:0]	7:3	Reserve.	
	PREFCH_CLK_GATE1	2	Gated clock MINF post-write module. 0: Clock enable. 1: Clock gated.	
	PREFCH_CLK_GATE	1	Gated clock MINF pre-fetch module. 0: Clock enable. 1: Clock gated.	
	MINF_SW_RSTZ	0	MINF pre-fetch / post-write module SW reset. 0: SW reset. 1: Normal.	
70h (1106E1h)	**REG1106E1**	**7:0**	**Default : 0x00**	**Access : RO**
	POSTWR_BUSY	7	Identify MINF post write in busy state.	
	RESERVE6[11:5]	6:0	See description of '1106E0h'.	
71h	**REG1106E2**	**7:0**	**Default : 0x46**	**Access : R/W**

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FUART1 Register (Bank = 1106)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1106E2h)	PREFCH_PATCH	7	SW patch control bit.	
	PREFCH_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	PREFCH_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	PREFCH_PRI	3	Define DRAM access priority.	
	PREFCH_RASTRD	2	MINF pre-fetch fast read enable.	
	PREFCH_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	PREFCH_CLR	0	SW clear MINF pre-fetch buffer. 0: Normal. 1: Clear.	
71h (1106E3h)	**REG1106E3**	**7:0**	**Default : 0x46**	**Access : R/W**
	POSTWR_FLUSH1_PATCH	7	SW flush path.	
	POSTWR_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	POSEWR_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	POSTWR_PRI	3	Define DRAM access priority.	
	POSTWR_FLUSH1	2	SW flush path.	
	POSTWR_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	POSTWR_FLUSH	0	SW flush MINF post write buffer. 0: Normal. 1: Flush.	

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GE1 Register (Bank = 1107)

GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (110700h)	**REG110700**	**7:0**	**Default : 0x01**	**Access : R/W**
	EN_GE_DCK	7	Enable Destination Color Key. 0: Disable. 1: Enable.	
	EN_GE_SCK	6	Enable Source Color Key. 0: Disable. 1: Enable.	
	EN_GE_ROP	5	Enable ROP2. 0: Disable (equal to setting GE_ROP2 = 4'hc). 1: Enable.	
	EN_GE_ABL_DCK	4	Enable Alpha Destination Color Key. 0: Disable. 1: Enable.	
	EN_GE_ABL_SCK	3	Enable Alpha Source Color Key. 0: Disable. 1: Enable.	
	EN_GE_ABL	2	Enable Alpha Blending. 0: Disable. 1: Enable.	
	EN_GE_DITHER	1	Enable Dither. 0: Disable. 1: Enable.	
	EN_GE	0	Enable Graphics Engine (Unqueue). 0: Disable and reset to initial state. 1: Enable.	
00h (110701h)	**REG110701**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_GE_DSTAC	4	Enable Destination Alpha Compare. 0: Disable. 1: Enable.	
	EN_GE_ALPHA_CMP	3	Enable Alpha Compare. 0: Disable. 1: Enable.	
	EN_GE_DFB	2	Enable DFB alpha blending function. 0: Disable. 1: Enable.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EN_GE_RN	1	Enable Random Noise. 0: Disable. 1: Enable.	
	EN_GE_LPT	0	Enable Line Pattern Test. 0: Disable. 1: Enable.	
01h (110702h)	**REG110702**	**7:0**	**Default : 0x01**	**Access : R/W**
	EN_GE_LENGTH_LIMIT	7	Enable MIU Length Limitation (unqueue). 0: Disable. 1: Enable.	
	EN_GE_ITC	6	Enable Italic Font. 0: Disable. 1: Enable.	
	EN_GE_CLIP_CHK	5	Enable Clipping Check. 0: Disable. 1: Enable.	
	EN_GE_STBB	4	Enable Stretch BitBlt. 0: Disable (force to Do Non Stretch BitBlt). 1: Enable (Do Stretch BitBlt if GE_STBB_DX = 1.0 or GE_STBB_DY = 1.0; Do Non Stretch BitBlt if GE_STBB_DX = 1.0 and GE_STBB_DY = 1.0).	
	-	3:2	Reserved.	
	EN_GE_VCMQ	1	Enable Virtual Command Queue (unqueue). 0: Disable. 1: Enable.	
	EN_GE_CMQ	0	Enable Command Queue (unqueue). 0: Disable. 1: Enable.	
01h (110703h)	**REG110703**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_GE_CLKGATE	7	Enable Dynamic Clock Gating (unqueue). 0: Disable. 1: Enable.	
	-	6:5	Reserved.	
	EN_GE_CLR_MIU_INVALID	4	Clear Invalid MIU Flag (unqueue). 0: Disable. 1: Enable.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EN_GE_MIU1_PMA	3	Enable MIU1 protection (unqueue). 0: Disable. 1: Enable.	
	EN_GE_MIU0_PMA	2	Enable MIU0 protection (unqueue). 0: Disable. 1: Enable.	
	-	1:0	Reserved.	
02h (110704h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (110705h)	**REG110705**	**7:0**	**Default : 0x3F**	**Access : R/W**
	GE_LENGTH_MODE	7	GE MIU Length Limit Mode (unqueue). 0: Fix Mode. 1: Auto Change Mode.	
	GE_LENGTH_AUTO_POL	6	Polarity of Varient Mode (unqueue).	
	GE_LENGTH_TH[5:0]	5:0	GE MIU most access count (unqueue).	
03h (110706h)	**REG110706**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_W_TH[3:0]	7:4	Virtual Command Write Queue Threshold (unqueue).	
	GE_STBB_TH[3:0]	3:0	Reading Source Threshold.	
03h (110707h)	**REG110707**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_VCMQ_R_TH[3:0]	3:0	Virtual Command Read Queue Threshold (unqueue).	
04h ~ 07h (110708h ~ 11070Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
08h (110710h)	**REG110710**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU0_PMA_LTH[7:0]	7:0	MIU 0 Protection Memory Address Range Low Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
08h (110711h)	**REG110711**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU0_PMA_LTH[15:8]	7:0	See description of '110710h'.	
09h (110712h)	**REG110712**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU0_PMA_LTH[23:16]	7:0	See description of '110710h'.	
09h	**REG110713**	**7:0**	**Default : 0x80**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110713h)	GE_MIU0_PMA_MODE	7	In the miu0 protection range (unqueue). 0: The address in this range is invalid. 1: The address in this range is valid.	
	-	6:5	Reserved.	
	GE_MIU0_PMA_LTH[28:24]	4:0	See description of '110710h'.	
0Ah (110714h)	**REG110714**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU0_PMA_HTH[7:0]	7:0	MIU 0 Protection Memory Address Range High Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
0Ah (110715h)	**REG110715**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU0_PMA_HTH[15:8]	7:0	See description of '110714h'.	
0Bh (110716h)	**REG110716**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU0_PMA_HTH[23:16]	7:0	See description of '110714h'.	
0Bh (110717h)	**REG110717**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	GE_MIU0_PMA_HTH[28:24]	4:0	See description of '110714h'.	
0Ch (110718h)	**REG110718**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU1_PMA_LTH[7:0]	7:0	MIU 1 Protection Memory Address Range Low Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
0Ch (110719h)	**REG110719**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU1_PMA_LTH[15:8]	7:0	See description of '110718h'.	
0Dh (11071Ah)	**REG11071A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_MIU1_PMA_LTH[23:16]	7:0	See description of '110718h'.	
0Dh (11071Bh)	**REG11071B**	**7:0**	**Default : 0x80**	**Access : R/W**
	GE_MIU1_PMA_MODE	7	In the miu1 protection range (unqueue). 0: The address in this range is invalid. 1: The address in this range is valid.	
	-	6:5	Reserved.	
	GE_MIU1_PMA_LTH[28:24]	4:0	See description of '110718h'.	
0Eh (11071Ch)	**REG11071C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU1_PMA_HTH[7:0]	7:0	MIU 1 Protection Memory Address Range High Threshold. This Unit is Byte (16 byte alignment) (unqueue).	
0Eh (11071Dh)	**REG11071D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_MIU1_PMA_HTH[15:8]	7:0	See description of '11071Ch'.	
0Fh	**REG11071E**	**7:0**	**Default : 0xFF**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11071Eh)	GE_MIU1_PMA_HTH[23:16]	7:0	See description of '11071Ch'.	
0Fh (11071Fh)	**REG11071F**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	GE_MIU1_PMA_HTH[28:24]	4:0	See description of '11071Ch'.	
10h (110720h)	**REG110720**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	GE_ROP2[3:0]	3:0	Raster Operation ROP2.	
11h (110722h)	**REG110722**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_ABL_COEF[3:0]	3:0	Coefficient of Alpha Blending. Csrc is the source color. Cdst is the destination or background color. Asrc is the alpha value of source. Adst is the alpha value of destination. Aconst is the constant alpha value. If the dfb enable is on, the register will disable. 0: Csrc. 1: Csrc * Aconst + Cdst * (1 - Aconst). 2: Csrc * Asrc + Cdst * (1 - Asrc). 3: Csrc * Adst + Cdst * (1 - Adst). 4: ((Asrc * Aconst) * Csrc + (1-(Asrc *Aconst)) * Cdst). 5: ((Asrc * Aconst) * Csrc + Adst * Cdst * (1-(Asrc * Aconst))) / ((Asrc * Aconst) + Adst * (1- Asrc * Aconst)). 6: ((Asrc * Aconst) * Csrc * (1-Adst) + Adst * Cdst) / (Asrc * Aconst) * (1-Adst) + Adst). 7: Csrc * Aconst. 8: Cdst. 9: Csrc * (1 - Aconst) + Cdst * Aconst. a: Csrc * (1 - Asrc) + Cdst * Asrc. b: Csrc * (1 - Adst) + Cdst * Adst. c: (Csrc * Adst * Asrc * Aconst + Cdst * Adst * (1 - Asrc * Aconst)) / (Adst * Asrc * Aconst + Adst * (1 - Asrc * Aconst). d: (Cdst * Asrc * Aconst * Adst + Csrc * Asrc * Aconst * (1 - Adst)) / (Asrc * Aconst * (1 - Adst) + Asrc * Aconst * Adst). e: ((1 - Adst) * Csrc * Asrc * Aconst + Adst * Cdst * (1 - Asrc * Aconst)) / (Asrc * Aconst * (1 - Adst) + Adst * (1 - Asrc * Aconst)). f: Csrc * (1 - Aconst). Others: Reserved.	
11h (110723h)	**REG110723**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GE_ABL_1555[7:0]	7:0	Alpha value of ARGB1555.	
12h (110725h)	**REG110725**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_DB_ABL[3:0]	3:0	Alpha value of writing to Destination after Alpha Color Key. If the dfb is enable, this register will disable. 0: Aconst (DFB). 1: Asrc. 2: Adst. 3: Asrc * Aconst. 4: Asrc * Aconst * Adst. 5: Adst * (1 - Asrc * Aconst). 6: Asrc * Aconst * (1 - Adst). 7: Asrc * Aconst * (1 - Adst) + Adst. 8: 1 - Aconst (DFB). 9: 1 - Asrc. a: 1 - Adst. b: Adst * Asrc * Aconst + Adst * (1 - Asrc * Aconst) A atop B. c: Asrc * Aconst * Adst + Asrc * Aconst * (1 - Adst) B atop A. d: (1 - Adst) * Asrc * Aconst + Adst * (1 - Asrc * Aconst) A xor B. e: Asrc * Asrc * Aconst + Adst * (1 - Asrc * Aconst). f: Asrc * (1 - Asrc * Aconst) + Adst * Asrc * Aconst. Others: Reserved.	
13h (110726h)	**REG110726**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ABL_CONST[7:0]	7:0	Constant Alpha Register for Alpha Blending.	
14h (110728h)	**REG110728**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[7:0]	7:0	Source Color Key High Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
14h (110729h)	**REG110729**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[15:8]	7:0	See description of '110728h'.	
15h (11072Ah)	**REG11072A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[23:16]	7:0	See description of '110728h'.	
15h (11072Bh)	**REG11072B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[31:24]	7:0	See description of '110728h'.	
16h	**REG11072C**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11072Ch)	GE_SCK_LTH[7:0]	7:0	Source Color Key Low Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
16h (11072Dh)	**REG11072D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[15:8]	7:0	See description of '11072Ch'.	
17h (11072Eh)	**REG11072E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[23:16]	7:0	See description of '11072Ch'.	
17h (11072Fh)	**REG11072F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[31:24]	7:0	See description of '11072Ch'.	
18h (110730h)	**REG110730**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[7:0]	7:0	Destination Color Key High Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
18h (110731h)	**REG110731**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[15:8]	7:0	See description of '110730h'.	
19h (110732h)	**REG110732**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[23:16]	7:0	See description of '110730h'.	
19h (110733h)	**REG110733**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[31:24]	7:0	See description of '110730h'.	
1Ah (110734h)	**REG110734**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[7:0]	7:0	Destination Color Key Low Threshold. The index mode of 8-bit or 16-bit, high threshold and low threshold must be the same. [7:0] 8-bit Palette. [15:0] 16-bit Index Mode. [31:0] ARGB8888.	
1Ah (110735h)	**REG110735**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[15:8]	7:0	See description of '110734h'.	
1Bh (110736h)	**REG110736**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[23:16]	7:0	See description of '110734h'.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Bh (110737h)	**REG110737**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[31:24]	7:0	See description of '110734h'.	
1Ch (110738h)	**REG110738**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_DSTAC_MODE	5	Destination Alpha Compare Mode. 0: If the destination alpha is in the threshold, and GE won't do the alpha operation. 1: If the destination isn't in the Threshold, GE won't do the alpha operation.	
	GE_ALPHA_CMP_MODE	4	Alpha Compare Mode. 0: Maximum Alpha of Source and Destination. 1: Minimum Alpha of Source and Destination.	
	GE_ABL_DCK_OP_MODE	3	Destination Alpha Key Operation Mode. 0: If the color is not equal to the destination color key, the color will be replaced by the source color. 1: If the color is equal to the source color key, the color will be replaced by the source color.	
	GE_ABL_SCK_OP_MODE	2	Source Alpha Key Operation Mode. 0: If the color is equal to the source color key, the color will be replaced by the destination color. 1: If the color is not equal to the source color key, the color will be replaced by the destination color.	
	GE_DCK_OP_MODE	1	Destination Color Key Operation Mode. 0: If the color is not equal to the destination color key, the color will be replaced by the source color. 1: If the color is equal to the destination color key, the color will be replaced by the source color.	
	GE_SCK_OP_MODE	0	Source Color Key Operation Mode. 0: If the color is equal to the source color key, the color will be replaced by the destination color. 1: If the color is not equal to the source color key, the color will be replaced by the destination color.	
1Dh (11073Ah)	**REG11073A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTAC_HTH[7:0]	7:0	Destination Alpha Compare Value High Threshold.	
1Dh (11073Bh)	**REG11073B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTAC_LTH[7:0]	7:0	Destination Alpha Comparison Value Low Threshold.	
1Eh	**REG11073C**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11073Ch)	GE_IRQ_MASK[1:0]	7:6	Interrupt Mask.	
	-	5:0	Reserved.	
1Eh (11073Dh)	**REG11073D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	IRQ_RAW_STATUS[1:0]	7:6	Status of Interrupt on IP Side.	
	IRQ_FINAL_STATUS[1:0]	5:4	Status of Interrupt on CPU Side.	
	GE_IRQ_CLR[1:0]	3:2	Interrupt Clear.	
	GE_IRQ_FORCE[1:0]	1:0	Force Interrupt Enable.	
1Fh (11073Eh)	**REG11073E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_YUV_FM[1:0]	7:6	YUV destination 422 format. 0: CbY1CrY0. 1: CrY1CbY0. 2: Y1CbY0Cr. 3: Y1CrY0Cb.	
	GE_SB_YUV_FM[1:0]	5:4	YUV source 422 format. 0: CbY1CrY0. 1: CrY1CbY0. 2: Y1CbY0Cr. 3: Y1CrY0Cb.	
	GE_YUV_IN	3	UV input range. 0: 0~255. 1: -128~127.	
	GE_YUV_RANGE	2	YUV output range. 0: 0~255. 1: Y: 16~235, UV: 16~240.	
	GE_YUV_FILTER	1	UV 1 1 filter. 0: Disable. 1: Enable.	
	GE_DC_CSC_FM	0	Color Space Conversion Format for Decode (RGB to YUV). 0: Computer Mode (Y: 16~235, UV: 0~240). 1: CSC to 0~255. Others: Reserved.	
1Fh (11073Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h	**REG110740**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110740h)	GE_SB_BASE[7:0]	7:0	Base Address of Graphics Engine Source Buffer (unit = byte). The start of Source Buffer storage must be pixel aligned.	
20h (110741h)	**REG110741**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_BASE[15:8]	7:0	See description of '110740h'.	
21h (110742h)	**REG110742**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_BASE[23:16]	7:0	See description of '110740h'.	
21h (110743h)	**REG110743**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_MIU_SEL	7	Source Buffer MIU selection. 0: MIU0. 1: MIU1.	
	-	6:5	Reserved.	
	GE_SB_BASE[28:24]	4:0	See description of '110740h'.	
26h (11074Ch)	**REG11074C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[7:0]	7:0	Base Address of Graphics Engine Destination Buffer (unit = byte). The Destination Buffer storage must be pixel aligned.	
26h (11074Dh)	**REG11074D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[15:8]	7:0	See description of '11074Ch'.	
27h (11074Eh)	**REG11074E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[23:16]	7:0	See description of '11074Ch'.	
27h (11074Fh)	**REG11074F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_MIU_SEL	7	Destination Buffer MIU selection. 0: MIU0. 1: MIU1.	
	-	6:5	Reserved.	
	GE_DB_BASE[28:24]	4:0	See description of '11074Ch'.	
28h (110750h)	**REG110750**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_BASE[7:0]	7:0	Base Address of Virtual Command Queue (unqueue). The Unit of Base is Byte. The Destination Buffer storage must be 64bit alignment. [2:0] will be ignored.	
28h (110751h)	**REG110751**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_BASE[15:8]	7:0	See description of '110750h'.	
29h	**REG110752**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110752h)	GE_VCMQ_BASE[23:16]	7:0	See description of '110750h'.	
29h (110753h)	**REG110753**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_VCMQ_MIU_SEL	7	Virtual Command Queue MIU selection (unqueue). 0: MIU0. 1: MIU1.	
	-	6:5	Reserved.	
	GE_VCMQ_BASE[28:24]	4:0	See description of '110750h'.	
2Ah (110754h)	**REG110754**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_VCMQ_SIZE[2:0]	2:0	Size of Virtual Command Queue (unqueue). 0: 8k. 1: 16k. 2: 32k. 3: 64k. 4: 128k. 5: 256k. 6: 512k. 7: 1024k.	
2Ah (110755h)	**REG110755**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTBLEND[3:0]	7:4	Destination Blend. 0: ZERO [Adst * 0, Cdst * 0]. 1: ONE [Adst * 1, Cdst * 1]. 2: SRCCOLOR [Adst * Asrc, Cdst * Csrc]. 3: INVSRCCOLOR [Adst * (1 - Asrc), Cdst * (1 - Csrc)]. 4: SRCALPHA [Adst * Asrc, Cdst * Asrc]. 5: INVSRCALPHA [Adst * (1 - Asrc), Cdst * (1- Asrc)]. 6: DESTALPHA [Adst * Adst, Cdst * Adst]. 7: INVDESTALPHA [Adst * (1 - Adst), Cdst * (1 - Adst)]. 8: DESTCOLOR [Adst * Adst, Cdst * Cdst]. 9: INVDESTCOLOR [Adst * (1 - Adst), Cdst * (1 - Cdst)]. 10: SRCALPHASAT [Adst * 1, Cdst * min(Asrc, (1 - Adst))].	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_SRCBLEND[3:0]	3:0	Source Blend. 0: ZERO [Asrc * 0, Csrc * 0]. 1: ONE [Asrc * 1, Csrc * 1]. 2: SRCCOLOR [Asrc * Asrc, Csrc * Csrc]. 3: INVSRCCOLOR [Asrc * (1 - Asrc), Csrc * (1 - Csrc)]. 4: SRCALPHA [Asrc * Asrc, Csrc * Asrc]. 5: INVSRCALPHA [Asrc * (1 - Asrc), Csrc * (1- Asrc)]. 6: DESTALPHA [Asrc * Adst, Csrc * Adst]. 7: INVDESTALPHA [Asrc * (1 - Adst), Csrc * (1 - Adst)]. 8: DESTCOLOR [Asrc * Adst, Csrc * Cdst]. 9: INVDESTCOLOR [Asrc * (1 - Adst), Csrc * (1 - Cdst)]. 10: SRCALPHASAT [Asrc * 1, Csrc * min(Asrc, (1 - Adst))].	
2Bh (110756h)	**REG110756**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DEMUL	7	Csrc is the source color. Cdst is the destination color. 0: [Asrc, Csrc]. 1: [Asrc / Asrc, Csrc / Asrc].	
	GE_XOR	6	Asrc is the source alpha. Adst is the destination alpha. Csrc is the source color. Cdst is the destination color. 0: [Adst, Cdst]. 1: [Asrc^Adst, Csrc^Cdst].	
	GE_DST_PREMUL	5	Csrc is the source color. Adst is the alpha value of destination. 0: Cdst. 1: Cdst * Adst.	
	GE_SRC_PRECOL	4	Csrc is the source color. Aconst is the constant alpha value. 0: Csrc. 1: Csrc * Aconst.	
	GE_SRC_PREMUL	3	Asrc is the alpha value of source. Csrc is the source color. 0: Csrc. 1: Csrc * Asrc.	
	GE_COLORIZE	2	Csrc is the source color. Cconst is the constant color value. 0: Csrc. 1: Csrc * Cconst.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_ALPHACH	1	Asrc is the alpha value of source. Aconst is the constant alpha value. Asmask is the source mask alpha. If coloralpha and source mask are all disable, this register is nouse. 0: Aconst. 1: Asrc * Aconst or Asrc * Asmask.	
	GE_COLORALPHA	0	Asrc is the alpha value of source. Aconst is the constant alpha value. 0: Asrc. 1: Asrc * Aconst (alphach enable) or Aconst (alphach disable).	
2Bh (110757h)	**REG110757**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_B_CONST[7:0]	7:0	Constant blue.	
2Ch (110758h)	**REG110758**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_G_CONST[7:0]	7:0	Constant green.	
2Ch (110759h)	**REG110759**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_R_CONST[7:0]	7:0	Constant red.	
2Dh (11075Ah)	**REG11075A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_B[7:0]	7:0	256 Pallette Table Blue.	
2Dh (11075Bh)	**REG11075B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_G[7:0]	7:0	256 Pallette Table Green.	
2Eh (11075Ch)	**REG11075C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_R[7:0]	7:0	256 Pallette Table Red.	
2Eh (11075Dh)	**REG11075D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_A[7:0]	7:0	256 Pallette Table Alpha.	
2Fh (11075Eh)	**REG11075E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_P256_INDEX[7:0]	7:0	Index of 256 Pallette Table.	
2Fh (11075Fh)	**REG11075F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GE_P256_RW	0	256 Pallette Table read/write.	
30h (110760h)	**REG110760**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_PIT[7:0]	7:0	Pitch of Graphics Engine Source Buffer (unit = byte). In I1, I2, and I4 modes: the pitch must be 8-bit aligned. In other modes: the pitch must be 32-bit aligned.	

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GE1 Register (Bank = 1107)

Index (Absolute)	Mnemonic	Bit	Description	
30h (110761h)	**REG110761**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_SB_PIT[13:8]	5:0	See description of '110760h'.	
31h (110762h)	**REG110762**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[7:0]	7:0	Tag Register.	
31h (110763h)	**REG110763**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[15:8]	7:0	See description of '110762h'.	
32h (110764h)	**REG110764**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[23:16]	7:0	See description of '110762h'.	
32h (110765h)	**REG110765**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[31:24]	7:0	See description of '110762h'.	
33h (110766h)	**REG110766**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_PIT[7:0]	7:0	Pitch of Graphics Engine Destination Buffer (unit = byte). The pitch must be 32-bit aligned.	
33h (110767h)	**REG110767**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_DB_PIT[13:8]	5:0	See description of '110766h'.	
34h (110768h)	**REG110768**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_SB_FM[4:0]	4:0	Format of Graphics Engine Source Buffer. 0: 1 bit, Intensity 1. 1: 2 bits, Intensity 2. 2: 4 bits, Intensity 4. 4: 8 bits, Palette 8. 5: RGB332[7:0]. 6: 16 bits, FaBaFgBg2266[15:0]. 7: 16 bits, 1ABFgBg12355[15:0]. 8: 16 bits, RGB565[15:0]. 9: 16 bits, ARGB1555[15:0]. a: 16 bits, ARGB4444[15:0]. e: 16 bits, YUYV422[15:0]. f: 32 bits, ARGB8888[31:0]. 10: RGBA5551[15:0]. 11: RGBA4444[15:0]. 1f: ABGR8888[31:0]. Others: Reserved.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
34h (110769h)	**REG110769**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_DB_FM[4:0]	4:0	Format of Graphics Engine Destination Buffer. 4: 8 bits, Palette 8. 5: RGB332. 6: 16 bits, FaBaFgBg2266[15:0]. 7: 16 bits, 1ABFgBg12355[15:0]. 8: 16 bits, RGB565[15:0]. 9: 16 bits, 0RGB1555[15:0]. a: 16 bits, ARGB4444[15:0]. c: 16 bits, ARGB1555[15:0]. e: 16 bits, YUYV422[15:0]. f: ARGB8888[31:0]. 10: RGBA5551[15:0]. 11: RGBA4444[15:0]. 1f: ABGR8888[31:0]. Others: Reserved.	
35h (11076Ah)	**REG11076A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[7:0]	7:0	Intensity 0 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
35h (11076Bh)	**REG11076B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[15:8]	7:0	See description of '11076Ah'.	
36h (11076Ch)	**REG11076C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[23:16]	7:0	See description of '11076Ah'.	
36h (11076Dh)	**REG11076D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[31:24]	7:0	See description of '11076Ah'.	
37h	**REG11076E**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11076Eh)	GE_I1_C[7:0]	7:0	Intensity 1 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
37h (11076Fh)	**REG11076F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[15:8]	7:0	See description of '11076Eh'.	
38h (110770h)	**REG110770**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[23:16]	7:0	See description of '11076Eh'.	
38h (110771h)	**REG110771**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[31:24]	7:0	See description of '11076Eh'.	
39h (110772h)	**REG110772**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[7:0]	7:0	Intensity 2 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
39h (110773h)	**REG110773**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[15:8]	7:0	See description of '110772h'.	
3Ah (110774h)	**REG110774**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[23:16]	7:0	See description of '110772h'.	
3Ah (110775h)	**REG110775**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[31:24]	7:0	See description of '110772h'.	
3Bh (110776h)	**REG110776**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[7:0]	7:0	Intensity 3 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
3Bh	**REG110777**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110777h)	GE_I3_C[15:8]	7:0	See description of '110776h'.	
3Ch (110778h)	**REG110778**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[23:16]	7:0	See description of '110776h'.	
3Ch (110779h)	**REG110779**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[31:24]	7:0	See description of '110776h'.	
3Dh (11077Ah)	**REG11077A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[7:0]	7:0	Intensity 4 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
3Dh (11077Bh)	**REG11077B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[15:8]	7:0	See description of '11077Ah'.	
3Eh (11077Ch)	**REG11077C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[23:16]	7:0	See description of '11077Ah'.	
3Eh (11077Dh)	**REG11077D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[31:24]	7:0	See description of '11077Ah'.	
3Fh (11077Eh)	**REG11077E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[7:0]	7:0	Intensity 5 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
3Fh (11077Fh)	**REG11077F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[15:8]	7:0	See description of '11077Eh'.	
40h (110780h)	**REG110780**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[23:16]	7:0	See description of '11077Eh'.	
40h (110781h)	**REG110781**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[31:24]	7:0	See description of '11077Eh'.	
41h	**REG110782**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110782h)	GE_I6_C[7:0]	7:0	Intensity 6 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
41h (110783h)	**REG110783**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[15:8]	7:0	See description of '110782h'.	
42h (110784h)	**REG110784**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[23:16]	7:0	See description of '110782h'.	
42h (110785h)	**REG110785**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[31:24]	7:0	See description of '110782h'.	
43h (110786h)	**REG110786**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[7:0]	7:0	Intensity 7 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
43h (110787h)	**REG110787**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[15:8]	7:0	See description of '110786h'.	
44h (110788h)	**REG110788**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[23:16]	7:0	See description of '110786h'.	
44h (110789h)	**REG110789**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[31:24]	7:0	See description of '110786h'.	
45h (11078Ah)	**REG11078A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[7:0]	7:0	Intensity 8 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
45h	**REG11078B**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11078Bh)	GE_I8_C[15:8]	7:0	See description of '11078Ah'.	
46h (11078Ch)	**REG11078C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[23:16]	7:0	See description of '11078Ah'.	
46h (11078Dh)	**REG11078D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[31:24]	7:0	See description of '11078Ah'.	
47h (11078Eh)	**REG11078E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[7:0]	7:0	Intensity 9 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
47h (11078Fh)	**REG11078F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[15:8]	7:0	See description of '11078Eh'.	
48h (110790h)	**REG110790**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[23:16]	7:0	See description of '11078Eh'.	
48h (110791h)	**REG110791**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[31:24]	7:0	See description of '11078Eh'.	
49h (110792h)	**REG110792**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[7:0]	7:0	Intensity 10 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
49h (110793h)	**REG110793**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[15:8]	7:0	See description of '110792h'.	
4Ah (110794h)	**REG110794**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[23:16]	7:0	See description of '110792h'.	
4Ah (110795h)	**REG110795**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[31:24]	7:0	See description of '110792h'.	
4Bh	**REG110796**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110796h)	GE_I11_C[7:0]	7:0	Intensity 11 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
4Bh (110797h)	**REG110797**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[15:8]	7:0	See description of '110796h'.	
4Ch (110798h)	**REG110798**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[23:16]	7:0	See description of '110796h'.	
4Ch (110799h)	**REG110799**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[31:24]	7:0	See description of '110796h'.	
4Dh (11079Ah)	**REG11079A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[7:0]	7:0	Intensity 12 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
4Dh (11079Bh)	**REG11079B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[15:8]	7:0	See description of '11079Ah'.	
4Eh (11079Ch)	**REG11079C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[23:16]	7:0	See description of '11079Ah'.	
4Eh (11079Dh)	**REG11079D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[31:24]	7:0	See description of '11079Ah'.	
4Fh (11079Eh)	**REG11079E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[7:0]	7:0	Intensity 13 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
4Fh	**REG11079F**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11079Fh)	GE_I13_C[15:8]	7:0	See description of '11079Eh'.	
50h (1107A0h)	**REG1107A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[23:16]	7:0	See description of '11079Eh'.	
50h (1107A1h)	**REG1107A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[31:24]	7:0	See description of '11079Eh'.	
51h (1107A2h)	**REG1107A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[7:0]	7:0	Intensity 14 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
51h (1107A3h)	**REG1107A3**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[15:8]	7:0	See description of '1107A2h'.	
52h (1107A4h)	**REG1107A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[23:16]	7:0	See description of '1107A2h'.	
52h (1107A5h)	**REG1107A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[31:24]	7:0	See description of '1107A2h'.	
53h (1107A6h)	**REG1107A6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[7:0]	7:0	Intensity 15 color for Graphics Engine Source Buffer in I format. [31:0] ARGB8888. [15:0] 1BA1A2FgBg (123433). [15:0] 1ABFgBg (12355). [15:0] FaBaFgBg (2266). [7:0] 8-bit Palette.	
53h (1107A7h)	**REG1107A7**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[15:8]	7:0	See description of '1107A6h'.	
54h (1107A8h)	**REG1107A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[23:16]	7:0	See description of '1107A6h'.	
54h (1107A9h)	**REG1107A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[31:24]	7:0	See description of '1107A6h'.	
55h (1107AAh)	**REG1107AA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_CLIP_LEFT[7:0]	7:0	2D Clipping Window Left Setting (11).	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (1107ABh)	**REG1107AB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_LEFT[11:8]	3:0	See description of '1107AAh'.	
56h (1107ACh)	**REG1107AC**	**7:0**	**Default : 0xD0**	**Access : R/W**
	GE_CLIP_RIGHT[7:0]	7:0	2D Clipping Window Right Setting (11).	
56h (1107ADh)	**REG1107AD**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_RIGHT[11:8]	3:0	See description of '1107ACh'.	
57h (1107AEh)	**REG1107AE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_CLIP_TOP[7:0]	7:0	2D Clipping Window Top Setting (11).	
57h (1107AFh)	**REG1107AF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_TOP[11:8]	3:0	See description of '1107AEh'.	
58h (1107B0h)	**REG1107B0**	**7:0**	**Default : 0x40**	**Access : R/W**
	GE_CLIP_BOT[7:0]	7:0	2D Clipping Window Bottom Setting (11).	
58h (1107B1h)	**REG1107B1**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	GE_CLIP_BOT[11:8]	3:0	See description of '1107B0h'.	
59h (1107B2h)	**REG1107B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_TYPE[1:0]	7:6	Strech Bitblt with Color Key Type. 0: Do nothing. 1: Nearest When the Color Key happened. 2: Replace the Key to Custom Color. 3: Reserved.	
	-	5:2	Reserved.	
	GE_ROT[1:0]	1:0	Coordinate Rotation Degree (Clockwise). 0: 0. 1: 90. 2: 180. 3: 270.	
5Ch (1107B8h)	**REG1107B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_B[7:0]	7:0	Stretch Bitblt Replace Blue.	
5Ch (1107B9h)	**REG1107B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_G[7:0]	7:0	Stretch Bitblt Replace Green.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Dh (1107BAh)	**REG1107BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_R[7:0]	7:0	Stretch Bitblt Replace Blue.	
5Dh (1107BBh)	**REG1107BB**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_SCK_A[7:0]	7:0	Stretch Bitblt Replace Alpha.	
5Eh (1107BCh)	**REG1107BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_INI_DX[7:0]	7:0	Initial Delta X for Stretch BitBlt (s.12).	
5Eh (1107BDh)	**REG1107BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_INI_DX[12:8]	4:0	See description of '1107BCh'.	
5Fh (1107BEh)	**REG1107BE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_INI_DY[7:0]	7:0	Initial Delta Y for Stretch BitBlt (s.12).	
5Fh (1107BFh)	**REG1107BF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_INI_DY[12:8]	4:0	See description of '1107BEh'.	
60h (1107C0h)	**REG1107C0**	**7:0**	**Default : 0x40**	**Access : R/W**
	GE_PRI_S_X_DIR	7	For Rectangle Fill and BitBlt: Primitive Drawing Direction in X Coordinates for Source. If the source direction is not equal to the destination direction, it means X mirror. 0: Positive Direction: From Left to Right. 1: Negative Direction: From Right to Left.	
	GE_PRIM_TYPE[2:0]	6:4	Primitive Type of 2D Graphics. A write to this register will cause an engine fire. 1: Line. 3: Rectangle Fill. 4: BitBlt. 7: Freeze. Others: Reserved.	
	-	3:0	Reserved.	
60h (1107C1h)	**REG1107C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_PATCH	7	Stretch BitBlt Patch Pixel Type. 0: Add zeros. 1: Duplicate last pixel or first pixel.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_STBB_TYPE	6	Stretch BitBlt Type. 0: Bilinear Mode. 1: Nearest Mode (8-bit palette and 16-bit index must use this mode).	
	GE_RECT_CV	5	Rectangle Fill Vertical Color Type. 0: Constant Color Fill. 1: Gradient Color Fill.	
	GE_RECT_CH	4	Rectangle Fill Horizontal Color Type. 0: Constant Color Fill. 1: Gradient Color Fill.	
	GE_LINE_C_TYPE	3	Color Type Setting for Line Drawing. 0: Constant Color Line Draw. 1: Gradient Color Line Draw.	
	GE_PRI_Y_DIR	2	For Rectangle Fill and BitBlt: Primitive Drawing Direction in Y Coordinates for Destination. 0: Positive Direction: From Top to Bottom. 1: Negative Direction: From Top to Bottom.	
	GE_PRI_X_DIR	1	For Rectangle Fill and BitBlt: Primitive Drawing Direction in X Coordinates for Destination. For Line Drawing: Primitive Drawing Direction in Major Coordinates defined in GE_LINE_MAJOR. 0: Positive Direction: From Left to Right. 1: Negative Direction: From Right to Left.	
	GE_PRI_S_Y_DIR	0	For Rectangle Fill and BitBlt: Primitive Drawing Direction in Y Coordinates for Destination. 0: Positive Direction: From Top to Bottom. 1: Negative Direction: From Bottom to Top.	
61h (1107C2h)	**REG1107C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_LINE_DELTA[6:0]	7:1	Delta value of minor direction for Line Drawing. X delta value for BitBlt (s1.12).	
	-	0	Reserved.	
61h	**REG1107C3**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1107C3h)	GE_LINE_MAJOR	7	Major Direction Setting for Line Drawing. 0: X is the major direction. 1: Y is the major direction.	
	GE_LINE_DELTA[13:7]	6:0	See description of '1107C2h'.	
62h (1107C4h)	**REG1107C4**	**7:0**	**Default : 0x3F**	**Access : R/W**
	GE_LPT_RPF[1:0]	7:6	Line Pattern Repeat Factor. 00: Repeat Factor = 1. 01: Repeat Factor = 2. 10: Repeat Factor = 3. 11: Repeat Factor = 4.	
	GE_LPT[5:0]	5:0	Line Pattern. [5:0] Line Pattern. LSB will be used first.	
62h (1107C5h)	**REG1107C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GE_LINE_LAST	1	Line Last Pixel Control. 0: Do not draw the last pixel of line. 1: Draw the last pixel of line.	
	GE_LPT_RST	0	Line Pattern Reset Control. Writing 1 to this bit will cause a Line Pattern Reset. After the reset, HW will automatically set this bit back to 0. 0: Do not reset Line Pattern for Line Drawing. 1: Reset Line Pattern for Line Drawing.	
63h (1107C6h)	**REG1107C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_LINE_LENGTH[7:0]	7:0	Line Length.	
63h (1107C7h)	**REG1107C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_LINE_LENGTH[11:8]	3:0	See description of '1107C6h'.	
64h (1107C8h)	**REG1107C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_DX[7:0]	7:0	Delta X for Stretch BitBlt (1.12).	
64h (1107C9h)	**REG1107C9**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_DX[12:8]	4:0	See description of '1107C8h'.	
65h (1107CAh)	**REG1107CA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_DY[7:0]	7:0	Delta Y for Stretch BitBlt (1.12).	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
65h (1107CBh)	**REG1107CB**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_DY[12:8]	4:0	See description of '1107CAh'.	
66h (1107CCh)	**REG1107CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ITC_DIS[7:0]	7:0	Initial distance of the italic font.	
66h (1107CDh)	**REG1107CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ITC_LINE[7:0]	7:0	Initial line of the italic font.	
67h (1107CEh)	**REG1107CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_ITC_DELTA[4:0]	4:0	Delta value of Italic BitBlt (s1.3).	
68h (1107D0h)	**REG1107D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V0_X[7:0]	7:0	X0, Coordinate X of Primitive Vertex 0. (unit: pixel limit:4079).	
68h (1107D1h)	**REG1107D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V0_X[11:8]	3:0	See description of '1107D0h'.	
69h (1107D2h)	**REG1107D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V0_Y[7:0]	7:0	Y0, Coordinate Y of Primitive Vertex 0. (unit: pixel limit:4095).	
69h (1107D3h)	**REG1107D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V0_Y[11:8]	3:0	See description of '1107D2h'.	
6Ah (1107D4h)	**REG1107D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V1_X[7:0]	7:0	X1, Coordinate X of Primitive Vertex 1. (unit: pixel limit: 4079).	
6Ah (1107D5h)	**REG1107D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V1_X[11:8]	3:0	See description of '1107D4h'.	
6Bh (1107D6h)	**REG1107D6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V1_Y[7:0]	7:0	Y1, Coordinate Y of Primitive Vertex 1. (unit:pixel limit: 4095).	
6Bh (1107D7h)	**REG1107D7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V1_Y[11:8]	3:0	See description of '1107D6h'.	

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Ch (1107D8h)	**REG1107D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V2_X[7:0]	7:0	X2, Coordinate X of Primitive Vertex 2. (unit:pixel limit 4079).	
6Ch (1107D9h)	**REG1107D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V2_X[11:8]	3:0	See description of '1107D8h'.	
6Dh (1107DAh)	**REG1107DA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V2_Y[7:0]	7:0	Y2, Coordinate Y of Primitive Vertex 2. (unit:pixel limit: 4095).	
6Dh (1107DBh)	**REG1107DB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V2_Y[11:8]	3:0	See description of '1107DAh'.	
6Eh (1107DCh)	**REG1107DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_S_W[7:0]	7:0	BitBlt Source Width (limit: 4080).	
6Eh (1107DDh)	**REG1107DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_STBB_S_W[11:8]	3:0	See description of '1107DCh'.	
6Fh (1107DEh)	**REG1107DE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_S_H[7:0]	7:0	BitBlt Source Height (limit: 4080).	
6Fh (1107DFh)	**REG1107DF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_STBB_S_H[11:8]	3:0	See description of '1107DEh'.	
70h (1107E0h)	**REG1107E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_ST[7:0]	7:0	Bst, Start Value of Primitive B Color. 1BAAFgBg123433 FgBg. 1ABFgBg12355 Bg. Palette 8.	
70h (1107E1h)	**REG1107E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_ST[7:0]	7:0	Gst, Start Value of Primitive G Color. 1BAAFgBg123433 A. 1ABFgBg12355 Fg.	
71h	**REG1107E2**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1107E2h)	GE_PRI_R_ST[7:0]	7:0	Rst, Start Value of Primitive R Color. 1BAAFgBg123433 BA. 1ABFgBg12355 AB.	
71h (1107E3h)	**REG1107E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_ST[7:0]	7:0	Ast, Start Value of Primitive Alpha Factor. 1BAAFgBg123433 1. 1ABFgBg12355 1.	
72h (1107E4h)	**REG1107E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DX[7:0]	7:0	Rdx, Primitive Parameter delta R in X direction for Rectangle Fill. Primitive Parameter delta R for Line Draw (s7.12).	
72h (1107E5h)	**REG1107E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DX[15:8]	7:0	See description of '1107E4h'.	
73h (1107E6h)	**REG1107E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_R_DX[19:16]	3:0	See description of '1107E4h'.	
74h (1107E8h)	**REG1107E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DY[7:0]	7:0	Rdy, Primitive Parameter delta R in Y direction for Rectangle Draw (s7.12).	
74h (1107E9h)	**REG1107E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DY[15:8]	7:0	See description of '1107E8h'.	
75h (1107EAh)	**REG1107EA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_R_DY[19:16]	3:0	See description of '1107E8h'.	
76h (1107ECh)	**REG1107EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DX[7:0]	7:0	Gdx, Primitive Parameter delta G in X direction for Rectangle Fill. Primitive Parameter delta G for Line Draw (s7.12).	
76h (1107EDh)	**REG1107ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DX[15:8]	7:0	See description of '1107ECh'.	
77h (1107EEh)	**REG1107EE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_G_DX[19:16]	3:0	See description of '1107ECh'.	
78h	**REG1107F0**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1107F0h)	GE_PRI_G_DY[7:0]	7:0	Gdy, Primitive Parameter delta G in Y direction for Rectangle Fill (s7.12).	
78h (1107F1h)	**REG1107F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DY[15:8]	7:0	See description of '1107F0h'.	
79h (1107F2h)	**REG1107F2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_G_DY[19:16]	3:0	See description of '1107F0h'.	
7Ah (1107F4h)	**REG1107F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DX[7:0]	7:0	Bdx, Primitive Parameter delta B in X direction for Rectangle Fill. Primitive Parameter delta B for Line Draw (s7.12).	
7Ah (1107F5h)	**REG1107F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DX[15:8]	7:0	See description of '1107F4h'.	
7Bh (1107F6h)	**REG1107F6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_B_DX[19:16]	3:0	See description of '1107F4h'.	
7Ch (1107F8h)	**REG1107F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DY[7:0]	7:0	Bdy, Primitive Parameter delta B in Y direction for Rectangle Fill (s7.12).	
7Ch (1107F9h)	**REG1107F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DY[15:8]	7:0	See description of '1107F8h'.	
7Dh (1107FAh)	**REG1107FA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_B_DY[19:16]	3:0	See description of '1107F8h'.	
7Eh (1107FCh)	**REG1107FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DX[7:0]	7:0	Adx, Primitive Parameter delta A in X direction for Rectangle Fill. Primitive Parameter delta A for Line Draw (s4.11).	
7Eh (1107FDh)	**REG1107FD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DX[15:8]	7:0	See description of '1107FCh'.	
7Fh (1107FEh)	**REG1107FE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DY[7:0]	7:0	Ady, Primitive Parameter delta A in Y direction for Rectangle Fill (s4.11).	
7Fh	**REG1107FF**	**7:0**	**Default : 0x00**	**Access : R/W**

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GE1 Register (Bank = 1107)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(1107FFh)	GE_PRI_A_DY[15:8]	7:0	See description of '1107FEh'.

ANA_MISC Register (Bank = 110C)

ANA_MISC Register (Bank = 110C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (110C00h)	**REG110C00**	**7:0**	**Default : 0x40**	**Access : R/W**
	MPLL_TEST[7:0]	7:0	MPLL test controls for test mode;	
00h (110C01h)	**REG110C01**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPLL_TEST[15:8]	7:0	See description of '110C00h'.	
01h (110C02h)	**REG110C02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MPLL_IN_SELECT	0	Input clock selection: While TEST[5]=1'b1, 1'b0 1.0V clock input; 1'b1 3.3V clock input after internal level shift to 1.0V;	
01h (110C03h)	**REG110C03**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:3	Reserved.	
	MPLL_CLK_ADC432M_PD	2	Disable MPLL_CLK_DP432M clock out, active low;	
	-	1	Reserved.	
	MPLL_PD	0	MPLL power down control, active low;	
02h (110C04h)	**REG110C04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MPLL_INPUT_DIV_FIRST[1:0]	5:4	MPLL input-divider control: 2'b00: /1; <-- default. 2'b01: /2; 2'b10: /4; 2'b11: /8:	
	-	3:0	Reserved.	
02h (110C05h)	**REG110C05**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	

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ANA_MISC Register (Bank = 110C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MPLL_LOOP_DIV_FIRST[1:0]	1:0	MPLL fisrt loop-divider control: 2'b00: /1; 2'b01: /2; 2'b10: /4; <-- default. 2'b11: /8:	
03h (110C06h)	**REG110C06**	**7:0**	**Default : 0x1B**	**Access : R/W**
	MPLL_LOOP_DIV_SECOND[7:0]	7:0	MPLL second loop-divider control: 8'h00: /1; 8'h01: /1; 8'h02: /4; 8'h03: /3 ... 8'h7F: /127; Others are not acceptable;	
03h (110C07h)	**REG110C07**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	MPLL_OUTPUT_DIV_FIRST[1:0]	5:4	MPLL output-divider control: 2'b00: /1; 2'b01: /2; <-- default. 2'b10: /4; 2'b11: /8:	
	-	3:1	Reserved.	
	MPLL_VCO_DIV2_DIS	0	Disable VCO output clock divided by 2; for MIPS set 1'b1.	
04h (110C08h)	**REG110C08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MPLL_ICP_ICTRL[1:0]	5:4	Charge-Pump current control: 2'h00: Icp x 4. 2'h01: Icp x 3. 2'h10: Icp x 2. 2'h11: Icp x1.	
	-	3:1	Reserved.	
	MPLL_TEST_EN	0	Enable test clocks out, default 1'b0;	
04h (110C09h)	**REG110C09**	**7:0**	**Default : 0x80**	**Access : RO, R/W**
	MPLL_CML_TX_PD	7	Disable mpll_cml_tx.	
	-	6	Reserved.	
	MPLL_HIGH_FLAG	5	MPLL Lock Flag of MPLL_TOP. (high active).	
	MPLL_LOCK	4	MPLL Lock of MPLL_TOP.	
	-	3:1	Reserved.	

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ANA_MISC Register (Bank = 110C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MPLL_ENFRUN	0	Enable VCO free-run with offset, default disable;	
10h (110C20h)	**REG110C20**	**7:0**	**Default : 0x40**	**Access : R/W**
	MIPSPLL_TEST[7:0]	7:0	MPLL test controls for test mode;	
10h (110C21h)	**REG110C21**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIPSPLL_TEST[15:8]	7:0	See description of '110C20h'.	
11h (110C22h)	**REG110C22**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MIPSPLL_IN_SELECT	0	Input clock selection: While TEST[5]=1'b1, 1'b0 1.0V clock input; 1'b1 3.3V clock input after internal level shift to 1.0V;	
11h (110C23h)	**REG110C23**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	MIPSPLL_VCO_DIV5_EN	4	Enable MPLL VCO_DIV5.	
	MIPSPLL_OCCCLK_EN	3	Enable MPLL OCCCLK.	
	-	2:1	Reserved.	
	MIPSPLL_PD	0	MPLL power down control, active low;	
12h (110C24h)	**REG110C24**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MIPSPLL_INPUT_DIV_FIRST[1:0]	5:4	MPLL input-divider control: 2'b00: /1; <-- default. 2'b01: /2; 2'b10: /4; 2'b11: /8:	
	-	3:0	Reserved.	
12h (110C25h)	**REG110C25**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	MIPSPLL_LOOP_DIV_FIRST[1:0]	1:0	MPLL fisrt loop-divider control: 2'b00: /1; 2'b01: /2; 2'b10: /4; <-- default. 2'b11: /8:	
13h	**REG110C26**	**7:0**	**Default : 0x3C**	**Access : R/W**

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ANA_MISC Register (Bank = 110C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110C26h)	MIPSPLL_LOOP_DIV_SECOND[7:0]	7:0	MPLL second loop-divider control: 8'h00: /1; 8'h01: /1; 8'h02: /4; 8'h03: /3 ... 8'h7F: /127; Others are not acceptable;	
13h (110C27h)	**REG110C27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MIPSPLL_OUTPUT_DIV_FIRST[1:0]	5:4	MPLL output-divider control: 2'b00: /1; 2'b01: /2; <-- default. 2'b10: /4; 2'b11: /8:	
	-	3:1	Reserved.	
	MIPSPLL_VCO_DIV2_DIS	0	Disable VCO output clock divided by 2; for MIPS set 1'b1.	
14h (110C28h)	**REG110C28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MIPSPLL_ICP_ICTRL[1:0]	5:4	Charge-Pump current control: 2'h00: Icp x 4. 2'h01: Icp x 3. 2'h10: Icp x 2. 2'h11: Icp x1.	
	-	3:1	Reserved.	
	MIPSPLL_TEST_EN	0	Enable test clocks out, default 1'b0;	
14h (110C29h)	**REG110C29**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	MIPSPLL_HIGH_FLAG	5	MPLL Lock Flag of MPLL_TOP. (high active).	
	MIPSPLL_LOCK	4	MPLL Lock of MPLL_TOP.	
	-	3:1	Reserved.	
	MIPSPLL_ENFRUN	0	Enable VCO free-run with offset, default disable;	
50h (110CA0h)	**REG110CA0**	**7:0**	**Default : 0x40**	**Access : R/W**
	MIPSPLL_TEST1[7:0]	7:0	MPLL test controls for test mode;	
50h (110CA1h)	**REG110CA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIPSPLL_TEST1[15:8]	7:0	See description of '110CA0h'.	
51h	**REG110CA2**	**7:0**	**Default : 0x01**	**Access : R/W**

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ANA_MISC Register (Bank = 110C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110CA2h)	-	7:1	Reserved.	
	MIPSPLL_IN_SELECT1	0	Input clock selection: While TEST[5]=1'b1, 1'b0 1.0V clock input; 1'b1 3.3V clock input after internal level shift to 1.0V;	
51h (110CA3h)	**REG110CA3**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	MIPSPLL_VCO_DIV5_EN1	4	Enable MPLL VCO_DIV5.	
	MIPSPLL_OCCCLK_EN1	3	Enable MPLL OCCCLK.	
	-	2:1	Reserved.	
	MIPSPLL_PD1	0	MPLL power down control, active low;	
52h (110CA4h)	**REG110CA4**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MIPSPLL_INPUT_DIV_FIRST1[1:0]	5:4	MPLL input-divider control: 2'b00: /1; <-- default. 2'b01: /2; 2'b10: /4; 2'b11: /8:	
	-	3:0	Reserved.	
52h (110CA5h)	**REG110CA5**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	MIPSPLL_LOOP_DIV_FIRST1[1:0]	1:0	MPLL fisrt loop-divider control: 2'b00: /1; 2'b01: /2; 2'b10: /4; <-- default. 2'b11: /8:	
53h (110CA6h)	**REG110CA6**	**7:0**	**Default : 0x3C**	**Access : R/W**
	MIPSPLL_LOOP_DIV_SECOND1[7:0]	7:0	MPLL second loop-divider control: 8'h00: /1; 8'h01: /1; 8'h02: /4; 8'h03: /3 ... 8'h7F: /127; Others are not acceptable;	
53h (110CA7h)	**REG110CA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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ANA_MISC Register (Bank = 110C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MIPSPLL_OUTPUT_DIV_FIRST1[1:0]	5:4	MPLL output-divider control: 2'b00: /1; 2'b01: /2; <-- default. 2'b10: /4; 2'b11: /8:	
	-	3:1	Reserved.	
	MIPSPLL_VCO_DIV2_DIS1	0	Disable VCO output clock divided by 2; for MIPS set 1'b1.	
54h (110CA8h)	**REG110CA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MIPSPLL_ICP_ICTRL1[1:0]	5:4	Charge-Pump current control: 2'h00: Icp x 4. 2'h01: Icp x 3. 2'h10: Icp x 2. 2'h11: Icp x1.	
	-	3:1	Reserved.	
	MIPSPLL_TEST_EN1	0	Enable test clocks out, default 1'b0;	
54h (110CA9h)	**REG110CA9**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	MIPSPLL_HIGH_FLAG1	5	MPLL Lock Flag of MPLL_TOP. (high active).	
	MIPSPLL_LOCK1	4	MPLL Lock of MPLL_TOP.	
	-	3:1	Reserved.	
	MIPSPLL_ENFRUN1	0	Enable VCO free-run with offset, default disable;	

MIU_ATOP Register (Bank = 110D)

MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (110D00h)	**REG110D00**	**7:0**	**Default : 0x58**	**Access : R/W**
	-	7	Reserved.	
	DDRPLL_CLKIN_DIV2_EN	6		
	SEL_LPDDR2	5		
	GPIO_MODE	4		

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIO_OENZ	3		
	PKG_SEL[2:0]	2:0	1: BGA, 0:QFP.	
00h (110D01h)	**REG110D01**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_00[2:0]	7:5		
	ODT_01_EN[1:0]	4:3		
	ODT_00_EN[1:0]	2:1		
	SEL_INTERNAL_DQS	0		
01h (110D02h)	**REG110D02**	**7:0**	**Default : 0xAA**	**Access : R/W**
	CKO_STATE[7:0]	7:0	Set the clock waveform: 8x mode: 10101010. 4x mode: 11001100.	
01h (110D03h)	**REG110D03**	**7:0**	**Default : 0xAA**	**Access : R/W**
	DQS_STATE[7:0]	7:0	Set the DQS waveform: 8x mode: 10101010. 4x mode: 11001100.	
02h (110D04h)	**REG110D04**	**7:0**	**Default : 0x30**	**Access : R/W**
	DQS_PRE_STATE[7:0]	7:0	Set the DQS preamble waveform.	
02h (110D05h)	**REG110D05**	**7:0**	**Default : 0x00**	**Access : R/W**
	DQ_OENZ_EN[3:0]	7:4		
	ODT_11_EN[1:0]	3:2		
	ODT_10_EN[1:0]	1:0		
03h (110D06h)	**REG110D06**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_03[7:0]	7:0		
03h (110D07h)	**REG110D07**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_03[15:8]	7:0	See description of '110D06h'.	
04h (110D08h)	**REG110D08**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_04_0[0]	7	Reserved.	
	RX_EN[6:0]	6:0		
04h (110D09h)	**REG110D09**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_04_1[1:0]	7:6	Enable ddrpll stop clk.	
	SEL_DQ_8BIT_MODE[1:0]	5:4		
	RESERVED_04_0[4:1]	3:0	See description of '110D08h'.	
05h (110D0Ah)	**REG110D0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODT_11_ALON[1:0]	7:6		

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ODT_10_ALON[1:0]	5:4		
	ODT_01_ALON[1:0]	3:2		
	ODT_00_ALON[1:0]	1:0		
05h (110D0Bh)	**REG110D0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_05[6:0]	7:1		
	SEL_WEAK_PH	0		
06h (110D0Ch)	**REG110D0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_06_0[3:0]	7:4		
	LOOPBACK_DIG_EN	3		
	TEST_CLK_EN[2:0]	2:0		
06h (110D0Dh)	**REG110D0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_SEL[3:0]	7:4		
	SYN_DEB_BUS_SEL[1:0]	3:2		
	RESERVED_06_1	1		
	TEST_EN	0		
07h (110D0Eh)	**REG110D0E**	**7:0**	**Default : 0x60**	**Access : R/W**
	DQSM_STA_RST	7		
	DQSM_RST_SEL	6		
	DQSM_SW_RST	5	Reg_r_dqs025x_cnt reset.	
	REF_WPTR_EN	4		
	DQSM_DLY[2:0]	3:1		
	EN_MASK	0		
07h (110D0Fh)	**REG110D0F**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DQSM_STATUS_FALL[3:0]	7:4	Dqs mask falling edge status (STA_TRACK).	
	R_DQS025X_CNT[3:0]	3:0	Dqs05x initial cnt.	
08h (110D10h)	**REG110D10**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_08[7:0]	7:0		
08h (110D11h)	**REG110D11**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_DQSM_STATUS_RISE[3:0]	7:4	Dqs mask rising edge status (STA).	
	RESERVED_08[11:8]	3:0	See description of '110D10h'.	
09h (110D12h)	**REG110D12**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_09_0[3:0]	7:4		
	DQS1_DLY_SEL[1:0]	3:2		

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DQS0_DLY_SEL[1:0]	1:0		
09h (110D13h)	**REG110D13**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_09_1[3:0]	7:4		
	DQS3_DLY_SEL[1:0]	3:2		
	DQS2_DLY_SEL[1:0]	1:0		
0Ah (110D14h)	**REG110D14**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0A[7:0]	7:0		
0Ah (110D15h)	**REG110D15**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0A[15:8]	7:0	See description of '110D14h'.	
0Bh (110D16h)	**REG110D16**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0B[7:0]	7:0	Reserved.	
0Bh (110D17h)	**REG110D17**	**7:0**	**Default : 0x1F**	**Access : R/W**
	GPIOS_LH_SEL	7		
	GPIO_LH_SEL	6		
	-	5	Reserved.	
	GPIO_PAD_MODE[4:0]	4:0		
0Ch (110D18h)	**REG110D18**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0C[5:0]	7:2		
	DDRPLL_STOP_MCLK	1	MCLK2X_SKEW_DQSMASK2 phase select.	
	MIU_STALL_EN	0		
0Ch (110D19h)	**REG110D19**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_SWITCH_CLK_RDY	7	Read only.	
	R_MIU_BUSY	6	Read only : check miu is busy or not (including fifo2).	
	RESERVED_0C[11:6]	5:0	See description of '110D18h'.	
0Dh (110D1Ah)	**REG110D1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0D[0]	7		
	DDRPLL_LF_PDIV[2:0]	6:4		
	AC_RATIO_SEL[1:0]	3:2		
	DDRPLL_LF_EN	1		
	DDRPLL_EN_PDIV4	0		
0Dh (110D1Bh)	**REG110D1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0D[8:1]	7:0	See description of '110D1Ah'.	
0Eh	**REG110D1C**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110D1Ch)	RESERVED_0E[7:0]	7:0	Reserved.	
0Eh (110D1Dh)	**REG110D1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0E[15:8]	7:0	See description of '110D1Ch'.	
0Fh (110D1Eh)	**REG110D1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0F[7:0]	7:0	Reserved.	
0Fh (110D1Fh)	**REG110D1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0F[15:8]	7:0	See description of '110D1Eh'.	
10h (110D20h)	**REG110D20**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	DDRIP[2:0]	6:4	Clock generator loop filter resistor.	
	-	3:1	Reserved.	
	ENFRUNZ	0	Vco free run disable.	
10h (110D21h)	**REG110D21**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DDRPLL_LOCK	7	For internal test only.	
	R_DDRPLL_SSC_OFF	6	For internal test only.	
	R_HIGH_FLAG	5	For internal test only.	
	-	4:0	Reserved.	
11h (110D22h)	**REG110D22**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[7:0]	7:0		
11h (110D23h)	**REG110D23**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[15:8]	7:0	See description of '110D22h'.	
12h (110D24h)	**REG110D24**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[23:16]	7:0	See description of '110D22h'.	
12h (110D25h)	**REG110D25**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[31:24]	7:0	See description of '110D22h'.	
13h (110D26h)	**REG110D26**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[39:32]	7:0	See description of '110D22h'.	
13h (110D27h)	**REG110D27**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_13[7:0]	7:0		
14h (110D28h)	**REG110D28**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSTEP[7:0]	7:0	Clock spread spectrum step.	
14h (110D29h)	**REG110D29**	**7:0**	**Default : 0x80**	**Access : R/W**
	DDR_SSC_EN	7	Clock spread spectrum enable.	

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DDR_SSC_MODE	6	Clock spread spectrum mode.	
	DDFT[1:0]	5:4	Clock generator test mode.	
	-	3:2	Reserved.	
	DDFSTEP[9:8]	1:0	See description of '110D28h'.	
15h (110D2Ah)	**REG110D2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSPAN[7:0]	7:0	Clock spread spectrum period.	
15h (110D2Bh)	**REG110D2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DDFSPAN[13:8]	5:0	See description of '110D2Ah'.	
16h (110D2Ch)	**REG110D2C**	**7:0**	**Default : 0x10**	**Access : RO, R/W**
	R_DUTY_FLAG	7		
	RESERVED_16_6_	6		
	DUTY_DIV[1:0]	5:4		
	DUTY_VT[1:0]	3:2		
	DUTY_EXPECT	1		
	DUTY_ENDUTY	0		
16h (110D2Dh)	**REG110D2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_16[7:0]	7:0		
17h (110D2Eh)	**REG110D2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_17[7:0]	7:0		
17h (110D2Fh)	**REG110D2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_17[15:8]	7:0	See description of '110D2Eh'.	
18h (110D30h)	**REG110D30**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSET[7:0]	7:0	Clock generator frequency set.	
18h (110D31h)	**REG110D31**	**7:0**	**Default : 0x02**	**Access : R/W**
	DDFSET[15:8]	7:0	See description of '110D30h'.	
19h (110D32h)	**REG110D32**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSET[23:16]	7:0	See description of '110D30h'.	
19h (110D33h)	**REG110D33**	**7:0**	**Default : 0xE0**	**Access : R/W**
	DDRPLL_PD	7	Pll power down mode.	
	DDRPLL_PORST	6	Pll power on reset.	
	DDRPLL_RESET	5	Pll reset.	
	-	4:0	Reserved.	

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ah (110D34h)	**REG110D34**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRPLL_INPUT_DIV_SECOND[7:0]	7:0	Set the clock frequency for dram.	
1Ah (110D35h)	**REG110D35**	**7:0**	**Default : 0x80**	**Access : R/W**
	DDRPLL_LOOP_DIV_SECOND[7:0]	7:0	Set the clock frequency for dram.	
1Bh (110D36h)	**REG110D36**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	CLKPH_CKO[3:0]	3:0	MCLK2X_SKEW_MCLK phase select.	
1Bh (110D37h)	**REG110D37**	**7:0**	**Default : 0x40**	**Access : R/W**
	DDRPLL_LOOP_DIV_FIRST[1:0]	7:6	Set the clock frequency for dram.	
	DDRPLL_INPUT_DIV_FIRST[1:0]	5:4	Set the clock frequency for dram.	
	-	3:0	Reserved.	
1Ch (110D38h)	**REG110D38**	**7:0**	**Default : 0x66**	**Access : R/W**
	CLKPH_DQ1[3:0]	7:4	MCLK2X_SKEW_DQ1 phase select.	
	CLKPH_DQ0[3:0]	3:0	MCLK2X_SKEW_DQ0 phase select.	
1Ch (110D39h)	**REG110D39**	**7:0**	**Default : 0x22**	**Access : R/W**
	CLKPH_DQS1[3:0]	7:4	MCLK2X_SKEW_DQS1 phase select.	
	CLKPH_DQS0[3:0]	3:0	MCLK2X_SKEW_DQS0 phase select.	
1Dh (110D3Ah)	**REG110D3A**	**7:0**	**Default : 0x22**	**Access : R/W**
	CLKPH_DQSM0[3:0]	7:4	MCLK2X_SKEW_DQSMASK0 phase select.	
	CLKPH_CMD0[3:0]	3:0	MCLK2X_SKEW_CMD phase select.	
1Dh (110D3Bh)	**REG110D3B**	**7:0**	**Default : 0x22**	**Access : R/W**
	CLKPH_DQSM1[3:0]	7:4	MCLK2X_SKEW_DQSMASK1 phase select.	
	CLKPH_CLK_A[3:0]	3:0	MCLK05X/025X_SKEW phase select.	
1Eh (110D3Ch)	**REG110D3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DQSM1_SKEW[2:0]	6:4		
	-	3	Reserved.	
	DQSM0_SKEW[2:0]	2:0		
1Eh (110D3Dh)	**REG110D3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_1E[15:11]	7:3		
	DQS_SKEW[2:0]	2:0		
1Fh (110D3Eh)	**REG110D3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DQ_SKEW[2:0]	6:4		
	-	3	Reserved.	
	OEN_SKEW[2:0]	2:0		
1Fh (110D3Fh)	**REG110D3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKO_SKEW[2:0]	6:4		
	-	3	Reserved.	
	CMD_SKEW[2:0]	2:0		
24h (110D48h)	**REG110D48**	**7:0**	**Default : 0x66**	**Access : R/W**
	CLKPH_DQ3[3:0]	7:4	MCLK2X_SKEW_DQ3 phase select.	
	CLKPH_DQ2[3:0]	3:0	MCLK2X_SKEW_DQ2 phase select.	
24h (110D49h)	**REG110D49**	**7:0**	**Default : 0x22**	**Access : R/W**
	CLKPH_DQS3[3:0]	7:4	MCLK2X_SKEW_DQS3 phase select.	
	CLKPH_DQS2[3:0]	3:0	MCLK2X_SKEW_DQS2 phase select.	
25h (110D4Ah)	**REG110D4A**	**7:0**	**Default : 0x20**	**Access : R/W**
	CLKPH_DQSM2[3:0]	7:4	MCLK2X_SKEW_DQSMASK2 phase select.	
	CLKPH_CMD1[3:0]	3:0		
25h (110D4Bh)	**REG110D4B**	**7:0**	**Default : 0x20**	**Access : R/W**
	CLKPH_DQSM3[3:0]	7:4	MCLK2X_SKEW_DQSMASK3 phase select.	
	RESERVED_25_1[3:0]	3:0		
26h (110D4Ch)	**REG110D4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DQSM3_SKEW[2:0]	6:4		
	-	3	Reserved.	
	DQSM2_SKEW[2:0]	2:0		
26h (110D4Dh)	**REG110D4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_26[7:0]	7:0		
27h (110D4Eh)	**REG110D4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_27[7:0]	7:0		
27h (110D4Fh)	**REG110D4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_27[15:8]	7:0	See description of '110D4Eh'.	
28h (110D50h)	**REG110D50**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_28[7:0]	7:0		

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (110D51h)	**REG110D51**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_28[15:8]	7:0	See description of '110D50h'.	
29h (110D52h)	**REG110D52**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_29[7:0]	7:0		
29h (110D53h)	**REG110D53**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_29[15:8]	7:0	See description of '110D52h'.	
2Ah (110D54h)	**REG110D54**	**7:0**	**Default : 0x7F**	**Access : R/W**
	RESERVED_2A_1[0]	7		
	ATOP_PD[6:0]	6:0		
2Ah (110D55h)	**REG110D55**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_2A_1[8:1]	7:0	See description of '110D54h'.	
2Dh (110D5Ah)	**REG110D5A**	**7:0**	**Default : 0x11**	**Access : R/W**
	DRVN_DQ_H[3:0]	7:4	DRVN DQ Bit[31:16] for MIU0.	
	DRVN_DQS_H[3:0]	3:0	DRVN DQS Bit[3:2] for MIU0.	
2Dh (110D5Bh)	**REG110D5B**	**7:0**	**Default : 0x11**	**Access : R/W**
	DRVP_DQ_H[3:0]	7:4	DRVP DQ Bit[31:16] for MIU0.	
	DRVP_DQS_H[3:0]	3:0	DRVP DQS Bit[3:2] for MIU0.	
2Eh (110D5Ch)	**REG110D5C**	**7:0**	**Default : 0x11**	**Access : R/W**
	DRVN_DQ[3:0]	7:4	DRVN.	
	DRVN_DQS[3:0]	3:0	DRVN.	
2Eh (110D5Dh)	**REG110D5D**	**7:0**	**Default : 0x11**	**Access : R/W**
	DRVN_CLK[3:0]	7:4	DRVN.	
	DRVN_CMD[3:0]	3:0	DRVN.	
2Fh (110D5Eh)	**REG110D5E**	**7:0**	**Default : 0x11**	**Access : R/W**
	DRVP_DQ[3:0]	7:4	DRVP.	
	DRVP_DQS[3:0]	3:0	DRVP.	
2Fh (110D5Fh)	**REG110D5F**	**7:0**	**Default : 0x11**	**Access : R/W**
	DRVP_CLK[3:0]	7:4	DRVP.	
	DRVP_CMD[3:0]	3:0	DRVP.	
30h (110D60h)	**REG110D60**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SAR_OFF	7	Test CLK enable.	
	AVG_EN	6	Reduce the speed of the dll, it is for ddr2.	

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AVG_MODE[1:0]	5:4	Average mode setting: 0: 4; 1: by8; 2: by16; 3: by32.	
	DLL_CHG_N	3	Sample clock set by SW.	
	DLL_RST	2	DLL Calibration Reset.	
	DLL_PD	1	DLL Calibration HW power down.	
	DLL_CAL_SW	0	DLL Calibration SW mode.	
30h (110D61h)	**REG110D61**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_DLL_REDU_CODE	7	Calibration output.	
	DLL_RD_OUT_SEL[2:0]	6:4	Reg33 read out selection: 0: Reg_r_sar_cnt; 1:reg_r_dll_code; 2: reg_r_avg; 3:reg_r_dll0_code; 4:reg_r_dll1_code.	
	DLL_TEST_CLK_EN	3	Test CLK enable.	
	-	2	Reserved.	
	HW_UPCODE_EN	1	Enable HW auto update DLL code setting in refresh period.	
	DYN_UPCODE_EN	0	Enable update DLL code setting in refresh period.	
31h (110D62h)	**REG110D62**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DLL_PS_CYCLE[7:0]	7:0	Change the pulse time of DLL.	
31h (110D63h)	**REG110D63**	**7:0**	**Default : 0x00**	**Access : R/W**
	DLL_TEST[7:0]	7:0	For dll test.	
32h (110D64h)	**REG110D64**	**7:0**	**Default : 0x00**	**Access : R/W**
	DLL_CODE[7:0]	7:0	Change the delay time of the DLL (0: max delay, 1: Min delay).	
32h (110D65h)	**REG110D65**	**7:0**	**Default : 0xF2**	**Access : R/W**
	DLL_PH[3:0]	7:4	Select the phase of DLL.	
	-	3:2	Reserved.	
	DLL_CODE[9:8]	1:0	See description of '110D64h'.	
33h (110D66h)	**REG110D66**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DLL_RD_OUT[7:0]	7:0	For internal test only.	
33h (110D67h)	**REG110D67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ALWAYS_IN	7	For internal test only.	
	RESERVED_33[4:0]	6:2		
	R_DLL_RD_OUT[9:8]	1:0	See description of '110D66h'.	
34h	**REG110D68**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110D68h)	DLL0_CODE[7:0]	7:0	For dqs0 dll.	
34h (110D69h)	**REG110D69**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	DLL0_CODE[9:8]	1:0	See description of '110D68h'.	
35h (110D6Ah)	**REG110D6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DLL1_CODE[7:0]	7:0	For dqs1 dll.	
35h (110D6Bh)	**REG110D6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DLL1_CODE[9:8]	1:0	See description of '110D6Ah'.	
36h (110D6Ch)	**REG110D6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_36[7:0]	7:0		
36h (110D6Dh)	**REG110D6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_36[15:8]	7:0	See description of '110D6Ch'.	
37h (110D6Eh)	**REG110D6E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DLL1_PH[3:0]	7:4	For 1 dqs delay phase select.	
	DLL0_PH[3:0]	3:0	For 0 dqs delay phase select.	
37h (110D6Fh)	**REG110D6F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DLL3_PH[3:0]	7:4	For 3 dqs delay phase select.	
	DLL2_PH[3:0]	3:0	For 2 dqs delay phase select.	
38h (110D70h)	**REG110D70**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DLL5_PH[3:0]	7:4	For 1 dqs delay phase select.	
	DLL4_PH[3:0]	3:0	For 0 dqs delay phase select.	
38h (110D71h)	**REG110D71**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DLL7_PH[3:0]	7:4	For 3 dqs delay phase select.	
	DLL6_PH[3:0]	3:0	For 2 dqs delay phase select.	
39h (110D72h)	**REG110D72**	**7:0**	**Default : 0x01**	**Access : R/W**
	TRIG_LVL1[3:0]	7:4	Trigger level setting by SW/HW offset.	
	TRIG_LVL0[3:0]	3:0	Trigger level setting by SW/HW offset.	
39h (110D73h)	**REG110D73**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_39[7:0]	7:0		
3Ah (110D74h)	**REG110D74**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3A[7:0]	7:0		
3Ah	**REG110D75**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIU_ATOP Register (Bank = 110D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(110D75h)	RESERVED_3A[15:8]	7:0	See description of '110D74h'.	
3Bh (110D76h)	**REG110D76**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3B[7:0]	7:0		
3Bh (110D77h)	**REG110D77**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3B[15:8]	7:0	See description of '110D76h'.	
3Ch (110D78h)	**REG110D78**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3C[7:0]	7:0		
3Ch (110D79h)	**REG110D79**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3C[15:8]	7:0	See description of '110D78h'.	
3Dh (110D7Ah)	**REG110D7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3D[7:0]	7:0		
3Dh (110D7Bh)	**REG110D7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3D[15:8]	7:0	See description of '110D7Ah'.	
3Eh (110D7Ch)	**REG110D7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDR_TEST[7:0]	7:0		
3Eh (110D7Dh)	**REG110D7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDR_TEST[15:8]	7:0	See description of '110D7Ch'.	
3Fh (110D7Eh)	**REG110D7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDR_TEST_H[7:0]	7:0		
3Fh (110D7Fh)	**REG110D7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDR_TEST_H[15:8]	7:0	See description of '110D7Eh'.	

ADC_DTOP Register (Bank = 1112)

ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (111200h)	**REG111200**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCB_TOGV2	7	1=ADC B channel interleaving every 2 VSYNC.	
	ADCB_TOGH2	6	1=ADC G channel interleaving every 2 VSYNC.	
	ADCG_TOGV2	5	1=ADC R channel interleaving every 2 VSYNC.	
	ADCG_TOGH2	4	1=ADC B channel interleaving every 2 HSYNC.	
	ADCR_TOGV2	3	1=ADC G channel interleaving every 2 HSYNC.	

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ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADCR_TOGH2	2	1=ADC R channel interleaving every 2 HSYNC.	
	RGB_NO_VRAND	1	1=no ADCA interleve V dithering.	
	RGB_NO_RAND	0	1=no ADCA interleve H/V dithering.	
01h (111202h)	**REG111202**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	RGB_INT_V_POLARITY	1	1=ADCA interleave vsync reference pulse polarity high.	
	RGB_INT_H_POLARITY	0	1=ADCA interleave hsync reference pulse polarity high.	
02h (111204h)	**REG111204**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_REF_CYC[7:0]	7:0	ADCA calibration trigger reference pulse cycle number.	
02h (111205h)	**REG111205**	**7:0**	**Default : 0x18**	**Access : R/W, WO**
	-	7:6	Reserved.	
	RGB_SELF_CAL_ALL_GAIN	5	1=ADCA calibration all gain mode enable.	
	RGB_SELF_CAL_MODE[1:0]	4:3	[0]=1: ADCA linear calibration enable. [1]=1: ADCA offset/gain calibration enable.	
	RGB_SELF_CAL_STOP	2	1=ADCA calibration stop in live mode.	
	RGB_SELF_CAL_LIVE	1	1=ADCA calibration live mode enable.	
	RGB_SELF_CAL_START	0	1=ADCA calibration start.	
03h (111206h)	**REG111206**	**7:0**	**Default : 0x10**	**Access : R/W**
	RGB_SELF_CAL_DLY[7:0]	7:0	ADCA claibration delay from reference pulse to linear/offset/gain calibration state.	
03h (111207h)	**REG111207**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_LIVE_WAIT_DLY[7:0]	7:0	ADCA claibration wait delay number of reference pulse before re-starting new calibration in live mode.	
04h (111208h)	**REG111208**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_SELF_CAL_GPUSE_SEL	3	1=ADCA SELF_CAL_G active high during linear calibration & gain calibration; Otherwise, ADCA SELF_CAL_G active high only during linear calibration.	
	RGB_SELF_CAL_BYPASS[2:0]	2:0	[0]=1: bypass ADC R calibration. [1]=1: bypass ADC G calibration. [2]=1: bypass ADC B calibration.	

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ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (11120Ch)	**REG11120C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RGB_LINEAR_CAL_MODE	0	1=ADCA linear calibration long mode.	
06h (11120Dh)	**REG11120D**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RGB_LINEAR_CAL_VREF_SEL[3:0]	7:4	ADCA VCAL setting during linear calibration.	
	RGB_LINEAR_CAL_PGA[3:0]	3:0	ADCA PGA setting during linear calibration.	
07h (11120Eh)	**REG11120E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ADCB_LCAL_EN	2	1=ADC B linear calibration update enable.	
	ADCG_LCAL_EN	1	1=ADC G linear calibration update enable.	
	ADCR_LCAL_EN	0	1=ADC R linear calibration update enable.	
08h (111210h)	**REG111210**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RGB_LINEAR_CAL_DLY[7:0]	7:0	ADCA linear calibration delay samples after reference pulse rising.	
08h (111211h)	**REG111211**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_LINEAR_CAL_DLY[11:8]	3:0	See description of '111210h'.	
09h (111212h)	**REG111212**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RGB_LINEAR_CAL_DUR[7:0]	7:0	ADCA linear calibration duration samples after reference pulse rising.	
12h (111224h)	**REG111224**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ADCB_OCAL_EN	3	1=ADC B offset calibration update enable.	
	ADCG_OCAL_EN	2	1=ADC G offset calibration update enable.	
	ADCR_OCAL_EN	1	1=ADC R offset calibration update enable.	
	RGB_OFFSET_CAL_MODE	0	1=ADCA offset calibration long mode.	
13h (111226h)	**REG111226**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RGB_OFFSET_CAL_DLY[7:0]	7:0	ADCA offset calibration delay samples after reference pulse rising.	
13h (111227h)	**REG111227**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_OFFSET_CAL_DLY[11:8]	3:0	See description of '111226h'.	
14h	**REG111228**	**7:0**	**Default : 0xFF**	**Access : R/W**

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ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111228h)	RGB_OFFSET_CAL_DUR[7:0]	7:0	ADCA offset calibration duration samples after reference pulse rising.	
1Fh (11123Eh)	**REG11123E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RGB_GAIN_CAL_MISMATCH_ONLY	4	1=ADCA gain calibration only calibrate channel0/channel1 mismatch.	
	ADCB_GCAL_EN	3	1=ADC B gain calibration update enable.	
	ADCG_GCAL_EN	2	1=ADC G gain calibration update enable.	
	ADCR_GCAL_EN	1	1=ADC R gain calibration update enable.	
	RGB_GAIN_CAL_MODE	0	1=ADCA gain calibration long mode.	
20h (111240h)	**REG111240**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RGB_GAIN_CAL_DLY[7:0]	7:0	ADCA gain calibration delay samples after reference pulse rising.	
20h (111241h)	**REG111241**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_GAIN_CAL_DLY[11:8]	3:0	See description of '111240h'.	
21h (111242h)	**REG111242**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RGB_GAIN_CAL_DUR[7:0]	7:0	ADCA gain calibration duration samples after reference pulse rising.	
21h (111243h)	**REG111243**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RGB_GAIN_CAL_DUR[15:8]	7:0	See description of '111242h'.	
3Fh (11127Eh)	**REG11127E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_GAIN_CAL_LVREF[3:0]	7:4	ADCA gain calibration low VCAL write value.	
	RGB_GAIN_CAL_HVREF[3:0]	3:0	ADCA gain calibration high VCAL write value.	
3Fh (11127Fh)	**REG11127F**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	RGB_GAIN_CAL_VREF_WP	7	ADCA gain calibration VCAL write enable.	
	-	6:4	Reserved.	
	RGB_GAIN_CAL_VREF_WG[3:0]	3:0	ADCA gain calibration VCAL write related gain setting.	
40h (111280h)	**REG111280**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_GAIN_CAL_TARGET[7:0]	7:0	ADCA gain calibration VCAL_HIGH-VCAL_LOW target digital code write value.	
40h (111281h)	**REG111281**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RGB_GAIN_CAL_TARGET[11:8]	3:0	See description of '111280h'.	

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ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (111282h)	**REG111282**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	RGB_GAIN_CAL_TARGET_WP	7	ADCA gain calibration (VCAL_HIGH-VCAL_LOW) target digital code write enable.	
	-	6:4	Reserved.	
	RGB_GAIN_CAL_TARGET_WG[3:0]	3:0	ADCA gain calibration VCAL_HIGH-VCAL_LOW target digital code write related gain setting.	
51h (1112A2h)	**REG1112A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ADCY_TOGV2	3	1=ADC Y channel interleaving every 2 VSYNC.	
	ADCY_TOGH2	2	1=ADC Y channel interleaving every 2 HSYNC.	
	CYU_NO_VRAND	1	1=no ADCB interleve V dithering.	
	CYU_NO_RAND	0	1=no ADCB interleve H/V dithering.	
52h (1112A4h)	**REG1112A4**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	CYU_INT_V_POLARITY	1	1=ADCB interleave vsync reference pulse polarity high.	
	CYU_INT_H_POLARITY	0	1=ADCB interleave hsync reference pulse polarity high.	
53h (1112A6h)	**REG1112A6**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_SELF_CAL_REF_CYC[7:0]	7:0	ADCB calibration trigger reference pulse cycle number.	
53h (1112A7h)	**REG1112A7**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	-	7:6	Reserved.	
	CYU_SELF_CAL_ALL_GAIN	5	1=ADCB calibration all gain mode enable.	
	CYU_SELF_CAL_MODE[1:0]	4:3	[0]=1: ADCB linear calibration enable. [1]=1: ADCB offset/gain calibration enable.	
	CYU_SELF_CAL_STOP	2	1=ADCB calibration stop in live mode.	
	CYU_SELF_CAL_LIVE	1	1=ADCB calibration live mode enable.	
	CYU_SELF_CAL_START	0	1=ADCB calibration start.	
54h (1112A8h)	**REG1112A8**	**7:0**	**Default : 0x10**	**Access : R/W**
	CYU_SELF_CAL_DLY[7:0]	7:0	ADCB claibration delay from reference pulse to linear/offset/gain calibration state.	
54h	**REG1112A9**	**7:0**	**Default : 0x00**	**Access : R/W**

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ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1112A9h)	CYU_SELF_CAL_LIVE_WAIT_DLY[7:0]	7:0	ADCB claibration wait delay number of reference pulse before re-starting new calibration in live mode.	
55h (1112AAh)	**REG1112AA**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	CYU_SELF_CAL_GPUSE_SEL	0	1=ADCB SELF_CAL_G active high during linear calibration & gain calibration; Otherwise, ADCB SELF_CAL_G active high only during linear calibration.	
57h (1112AEh)	**REG1112AE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CYU_LINEAR_CAL_MODE	0	1=ADCB linear calibration long mode.	
57h (1112AFh)	**REG1112AF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	CYU_LINEAR_CAL_VREF_SEL[3:0]	7:4	ADCB VCAL setting during linear calibration.	
	CYU_LINEAR_CAL_PGA[3:0]	3:0	ADCB PGA setting during linear calibration.	
58h (1112B0h)	**REG1112B0**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:1	Reserved.	
	ADCY_LCAL_EN	0	1=ADC Y linear calibration update enable.	
5Bh (1112B6h)	**REG1112B6**	**7:0**	**Default : 0x1F**	**Access : R/W**
	CYU_LINEAR_CAL_DLY[7:0]	7:0	ADCB linear calibration delay samples after reference pulse rising.	
5Bh (1112B7h)	**REG1112B7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CYU_LINEAR_CAL_DLY[11:8]	3:0	See description of '1112B6h'.	
5Ch (1112B8h)	**REG1112B8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CYU_LINEAR_CAL_DUR[7:0]	7:0	ADCB linear calibration duration samples after reference pulse rising.	
5Dh (1112BAh)	**REG1112BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ADCY_OCAL_EN	1	1=ADC Y offset calibration update enable.	
	CYU_OFFSET_CAL_MODE	0	1=ADCB offset calibration long mode.	
5Eh (1112BCh)	**REG1112BC**	**7:0**	**Default : 0x1F**	**Access : R/W**
	CYU_OFFSET_CAL_DLY[7:0]	7:0	ADCB offset calibration delay samples after reference pulse rising.	
5Eh	**REG1112BD**	**7:0**	**Default : 0x00**	**Access : R/W**

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ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1112BDh)	-	7:4	Reserved.	
	CYU_OFFSET_CAL_DLY[11:8]	3:0	See description of '1112BCh'.	
5Fh (1112BEh)	**REG1112BE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CYU_OFFSET_CAL_DUR[7:0]	7:0	ADCB offset calibration duration samples after reference pulse rising.	
64h (1112C8h)	**REG1112C8**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	CYU_GAIN_CAL_MISMATCH_ONLY	2	1=ADCB gain calibration only calibrate channel0/channel1 mismatch.	
	ADCY_GCAL_EN	1	1=ADC Y gain calibration update enable.	
	CYU_GAIN_CAL_MODE	0	1=ADCB gain calibration long mode.	
65h (1112CAh)	**REG1112CA**	**7:0**	**Default : 0x1F**	**Access : R/W**
	CYU_GAIN_CAL_DLY[7:0]	7:0	ADCB gain calibration delay samples after reference pulse rising.	
65h (1112CBh)	**REG1112CB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CYU_GAIN_CAL_DLY[11:8]	3:0	See description of '1112CAh'.	
66h (1112CCh)	**REG1112CC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CYU_GAIN_CAL_DUR[7:0]	7:0	ADCB gain calibration duration samples after reference pulse rising.	
66h (1112CDh)	**REG1112CD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CYU_GAIN_CAL_DUR[15:8]	7:0	See description of '1112CCh'.	
72h (1112E4h)	**REG1112E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_GAIN_CAL_LVREF[3:0]	7:4	ADCB gain calibration low VCAL write value.	
	CYU_GAIN_CAL_HVREF[3:0]	3:0	ADCB gain calibration high VCAL write value.	
72h (1112E5h)	**REG1112E5**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	CYU_GAIN_CAL_VREF_WP	7	ADCB gain calibration VCAL write enable.	
	-	6:4	Reserved.	
	CYU_GAIN_CAL_VREF_WG[3:0]	3:0	ADCB gain calibration VCAL write related gain setting.	
73h (1112E6h)	**REG1112E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_GAIN_CAL_TARGET[7:0]	7:0	ADCB gain calibration VCAL_HIGH-VCAL_LOW target digital code write value.	
73h (1112E7h)	**REG1112E7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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ADC_DTOP Register (Bank = 1112)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CYU_GAIN_CAL_TARGET[11:8]	3:0	See description of '1112E6h'.	
74h (1112E8h)	**REG1112E8**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	CYU_GAIN_CAL_TARGET_WP	7	ADCB gain calibration (VCAL_HIGH-VCAL_LOW) target digital code write enable.	
	-	6:4	Reserved.	
	CYU_GAIN_CAL_TARGET_WG[3:0]	3:0	ADCB gain calibration VCAL_HIGH-VCAL_LOW target digital code write related gain setting.	
7Bh (1112F6h)	**REG1112F6**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_REF_DLY[7:0]	7:0	The delay samples of ADCA calibration reference pulse after Hsync/Vsync.	
7Bh (1112F7h)	**REG1112F7**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_SELF_CAL_REF_SEL[2:0]	7:5	[2:0]=1xx : ADCA using VSYNC as calibration reference pulse. [2:0]=01x : ADCA using HSYNC as calibration reference pulse. [2:0]=001 : ADCA using HSOUT as calibration reference pulse. [2:0]=000 : ADCA calibration reference always high.	
	RGB_SELF_CAL_REF_EDGE	4	1=ADCA calibration reference using trailing edge of hsync/vsync.	
	RGB_SELF_CAL_REF_DLY[11:8]	3:0	See description of '1112F6h'.	
7Ch (1112F8h)	**REG1112F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_SELF_CAL_REF_DLY[7:0]	7:0	The delay samples of ADCB calibration reference pulse after Hsync/Vsync.	
7Ch (1112F9h)	**REG1112F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	CYU_SELF_CAL_REF_SEL[2:0]	7:5	[2:0]=1xx : ADCB using VSYNC as calibration reference pulse. [2:0]=01x : ADCB using HSYNC as calibration reference pulse. [2:0]=001 : ADCB using HSOUT as calibration reference pulse. [2:0]=000 : ADCB calibration reference always high.	
	CYU_SELF_CAL_REF_EDGE	4	1=ADCB calibration reference using trailing edge of hsync/vsync.	
	CYU_SELF_CAL_REF_DLY[11:8]	3:0	See description of '1112F8h'.	

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FCIE0 Register (Bank = 1113)

FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (111300h)	**REG111300**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (111301h)	**REG111301**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	NC_R2N_ECCCOR_INT	4	Software correct ecc error in RIU2NAND mode interrupt event.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	NC_R2N_RDY_INT	2	RIU2NAND job end interrupt event.	
	NC_JOB_END	1	NAND job end interrupt event.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (111302h)	**REG111302**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (111303h)	**REG111303**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5	Reserved.	
	NC_R2N_ECCCOR_INT_EN	4	Software correct ecc error in RIU2NAND mode interrupt enable.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	NC_R2N_RDY_INT_EN	2	RIU2NAND job end interrupt enable.	
	NC_JOB_ENDEN	1	NAND job end interrupt enable.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h	**REG111304**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111304h)	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (111305h)	**REG111305**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTRL_SEL	6	Select MIU dynamic clock source. 1: Control by SW. 0: Control by HW.	
	MIU_CLK_EN_SW	5	Enable MIU dynamic clock by HW (auto clear). It need to set before reg_mma_enable. 1: Enable. 0: Disable.	
	MIU_CLK_EN_HW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (111306h)	**REG111306**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h	**REG111307**	**7:0**	**Default : 0x00**	**Access : R/W**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111307h)	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '111306h'.	
04h (111308h)	**REG111308**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (111309h)	**REG111309**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '111308h'.	
05h (11130Ah)	**REG11130A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SD_STS_CHG	0	SD/MMC card plug-in or remove status change.	
06h (11130Ch)	**REG11130C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_CARD_DET_SRC	7	SD card-detect pin select. 0: SD_CDZ. 1: SD_DAT3.	
	-	6:1	Reserved.	
	SD_STS_EN	0	SD card status change interrupt enable.	
07h (11130Eh)	**REG11130E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SD_DET_N	0	SD/MMC card detection status.	
07h (11130Fh)	**REG11130F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	NF_RBZ_STS	0	Nand nf_rbz pin status.	
0Ah (111314h)	**REG111314**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	NC_EN	5	NAND controller interface enable.	
	-	4:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh	**REG111316**	**7:0**	**Default : 0x18**	**Access : R/W**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111316h)	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (111317h)	**REG111317**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '111316h'.	
0Ch (111318h)	**REG111318**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (111319h)	**REG111319**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '111318h'.	
0Dh (11131Ah)	**REG11131A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (11131Bh)	**REG11131B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (11131Ch)	**REG11131C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (11131Dh)	**REG11131D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (11131Eh)	**REG11131E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (111320h)	**REG111320**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (111321h)	**REG111321**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	-	2	Reserved.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	-	0	Reserved.	
11h (111322h)	**REG111322**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
12h (111324h)	**REG111324**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (111325h)	**REG111325**	**7:0**	**Default : 0x00**	**Access : RO**
	SD_DAT7	7	SD DATA Line 7.	
	SD_DAT6	6	SD DATA Line 6.	
	SD_DAT5	5	SD DATA Line 5.	
	SD_DAT4	4	SD DATA Line 4.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (111336h)	**REG111336**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (111337h)	**REG111337**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '111336h'.	
1Ch (111338h)	**REG111338**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (111339h)	**REG111339**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '111338h'.	
1Dh (11133Ah)	**REG11133A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (11133Bh)	**REG11133B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '11133Ah'.	
1Fh (11133Eh)	**REG11133E**	**7:0**	**Default : 0x00**	**Access : RO**
	NC_R2N_COUNT_9_0[1:0]	7:6	RIU2NAND word counter[9:0].	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NC_R2N_CS[3:0]	5:2	RIU2NAND state machine.	
	NFC2MI_RW	1	DMA read/write direction. 0: MIU/RIU to NAND. 1: NAND to MIU/RIU.	
	-	0	Reserved.	
1Fh (11133Fh)	**REG11133F**	**7:0**	**Default : 0x00**	**Access : RO**
	NC_R2N_COUNT_9_0[9:2]	7:0	See description of '11133Eh'.	
20h (111340h)	**REG111340**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	R2N_DO_END	6	Assert a pulse to end RIU write to NAND. Set by SW, auto clear by HW.	
	R2N_DO_EN	5	Assert a pulse for RIU write each word to NAND. Set by SW, auto clear by HW.	
	R2N_DO_START	4	Assert a pulse to start RIU write to NAND. Set by SW, auto clear by HW.	
	R2N_DI_END	3	Assert a pulse to end RIU read from NAND. Set by SW, auto clear by HW.	
	R2N_DI_EN	2	Assert a pulse for RIU read each word from NAND. Set by SW, auto clear by HW.	
	R2N_DI_START	1	Assert a pulse to start RIU read from NAND. Set by SW, auto clear by HW.	
	R2N_MODE	0	Enable RIU directly access NAND instead of MIU.	
20h (111341h)	**REG111341**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	NC_R2N_COUNT_11_10[1:0]	7:6	RIU2NAND word counter[11:10].	
	NFIE_DOH4_DLY1	5	Delay type = 0, 1, 2, 3.	
	NFIE_DOH4_DLY0	4	MSB data bus 4 delay cells selection.	
	NFIE_DOL4_DLY1	3	Delay type = 0, 1, 2, 3.	
	NFIE_DOL4_DLY0	2	LSB data bus 4 delay cells selection.	
	NFIE_DO_DLY_EN	1	Enable nfie2pad_do[7:0] delay for SSO issue.	
	-	0	Reserved.	
21h (111342h)	**REG111342**	**7:0**	**Default : 0x00**	**Access : RO**
	NC_R2N_DI_DATA[7:0]	7:0	Data port for RIU read data from NAND.	
21h	**REG111343**	**7:0**	**Default : 0x00**	**Access : RO**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111343h)	NC_R2N_DI_DATA[15:8]	7:0	See description of '111342h'.	
22h (111344h)	**REG111344**	**7:0**	**Default : 0x00**	**Access : R/W**
	R2N_DO_DATA[7:0]	7:0	Data port for RIU write data to NAND.	
22h (111345h)	**REG111345**	**7:0**	**Default : 0x00**	**Access : R/W**
	R2N_DO_DATA[15:8]	7:0	See description of '111344h'.	
23h ~ 24h (111346h ~ 111349h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
25h (11134Ah)	**REG11134A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CIFD_RD_REQ	1	Force read CIF Data FIFO 512 bytes.	
	CIFC_RD_REQ	0	Force read function on CIF Comand FIFO 64 bytes.	
25h (11134Bh)	**REG11134B**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFIE_DOH4_16B_DLY1	7	Delay type = 0, 1, 2, 3.	
	NFIE_DOH4_16B_DLY0	6	MSB data bus 4 delay cells selection.	
	NFIE_DOL4_16B_DLY1	5	Delay type = 0, 1, 2, 3.	
	NFIE_DOL4_16B_DLY0	4	LSB data bus 4 delay cells selection.	
	NFIE_DO_16B_DLY_EN	3	Enable nfie2pad_do[15:8] delay for SSO issue.	
	-	2:0	Reserved.	
2Ch (111359h)	**REG111359**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DS_TESTEN	6	DQS test enable.	
	DQS_MODE[1:0]	5:4	DQS mode sel. (select data latch phase). 00: 2T. 01: 1.5 T. 10: 2.5 T. 11: 1T.	
	DQS_DELAY_SEL[3:0]	3:0	DQS delay cell sel.	
2Dh (11135Ah)	**REG11135A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:0	Reserved.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Dh (11135Bh)	**REG11135B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MIU_WP_LAST2_SEL	6	Miu patch for fcie2mi_last. 0: New patch enable. 1: Original desing (for SD/eMMC).	
	-	5:2	Reserved.	
	NAND_DATA_REORDER[1:0]	1:0	NAND data pin reordering: 2'b00: 15~0; 2'b01: 0~15; 2'b10: 7~0, 8~15; 2'b11: 8~15,0~7;	
2Eh (11135Ch)	**REG11135C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (11135Eh)	**REG11135E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BOOT_SEL_CLR	3	Clear bootsram_access_sel.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh	**REG11135F**	**7:0**	**Default : 0x00**	**Access : R/W**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11135Fh)	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (111360h)	**REG111360**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (111361h)	**REG111361**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 0: Disp_nand_padmux. 1: SD. 2: MS serial mode + SM. 3: MS parallel mode. 4: CF. 5: MMA. 6: DFF. 7: Nand.	
31h (111362h)	**REG111362**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (111363h)	**REG111363**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '111362h'.	
32h (111364h)	**REG111364**	**7:0**	**Default : 0x40**	**Access : R/W**
	TOGGLEN_CNT_RST	7	Toggle count reset.	
	DAT_DIR	6	Data read/write direction.	
	TEST_MODE[1:0]	5:4	Flash macro test mode.	
	DQS_IN_SEL[3:0]	3:0	DQS In delay cell selection.	
32h (111365h)	**REG111365**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h (111366h)	**REG111366**	**7:0**	**Default : 0x01**	**Access : R/W**
	SD_TOGGLE_CNT[7:0]	7:0	Sd data toggle count for flash macro.	
33h (111367h)	**REG111367**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_TOGGLE_CNT[15:8]	7:0	See description of '111366h'.	
34h (111368h)	**REG111368**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (111369h)	**REG111369**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '111368h'.	
35h (11136Ah)	**REG11136A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	POWER_SAVE_INT_FORCE	4	Force Power Save interrupt active, for test.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
36h (11136Ch)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
36h (11136Dh)	**REG11136D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MIU_WP_PATCH	3	Enbale miu wrapper patch.	
	NC_WIDTH_PATCH	2	Enbale nc width patch.	
	MIU_ECC_PATCH_DIS	1	Disable miu ecc correct patch.	
	-	0	Reserved.	
37h (11136Eh)	**REG11136E**	**7:0**	**Default : 0x00**	**Access : R/W**
	NAND_CTL_DELAY_SEL_11_0[7:0]	7:0	Nand control signal delay cell selection. [2:0]: select 8 delay cells on nf_rez. [5:3]: select 8 delay cells on nf_wez. [8:6]: select 8 delay cells on nf_cle. [11:9]: select 8 delay cells on nf_ale.	
37h (11136Fh)	**REG11136F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	NAND_CTL_DELAY_EN	4	Nand control signal delay cell enable.	
	NAND_CTL_DELAY_SEL_11_0[11:8]	3:0	See description of '11136Eh'.	
38h (111370h)	**REG111370**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (111371h)	**REG111371**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '111370h'.	
39h (111372h)	**REG111372**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (111373h)	**REG111373**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '111372h'.	
3Ah (111374h)	**REG111374**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (111375h)	**REG111375**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '111374h'.	
3Bh (111376h)	**REG111376**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (111377h)	**REG111377**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '111376h'.	
3Ch (111378h)	**REG111378**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (111379h)	**REG111379**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '111378h'.	
3Dh (11137Ah)	**REG11137A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (11137Bh)	**REG11137B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '11137Ah'.	
40h	**REG111380**	**7:0**	**Default : 0x04**	**Access : R/W**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111380h)	NC_CHK_RB_STS_DIS	7	While executing wait_rb instruction, state machine checks R/B falling and rising egde status. 0: Enable. 1: Disable.	
	NC_CHK_RB_HIGH	6	While executing wait_rb instruction, state machine checks R/B high by delay 3 cycles instead of checking R/B low first. 0: Disable. 1: Enable.	
	NC_WP_AUTO	5	NAND WPZ controlled by hardware instead of firmware. 0: Software control. 1: Hardware auto mode.	
	NC_WP_EN	4	NAND WPZ controlled by software. 0: WPZ is Low. 1: WPZ is High.	
	NC_CE_AUTO	3	NAND CE controlled by hardware instead of firmware. 0: Software control. 1: Hardware auto mode.	
	NC_CE_EN	2	NAND CE controlled by software. 0: CEZ is Low. 1: CEZ is High.	
	NC_CE_SEL[1:0]	1:0	NAND Flash CE Chip Select 0/1/2/3. 00: Select CEZ. 01: Select CE1Z. 10: Select CE2Z. 11: Select CE3Z.	
40h (111381h)	**REG111381**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_INST_DELAY_NUM1[3:0]	7:4	Cycle count for delay instruction execute.	
	NC_INST_DELAY_NUM[3:0]	3:0	Cycle count for delay instruction execute.	
41h (111382h)	**REG111382**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_RD_HW[1:0]	7:6	Cycle count for RDJ high width.	
	NC_WR_LW[2:0]	5:3	Cycle count for WRJ low width.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NC_WR_HW[2:0]	2:0	Cycle count for WRJ high width. 000: 1 clock cycle. 001: 2 clock cycle. 010: 3 clock cycle. 011: 4 clock cycle. 100: 5 clock cycle. 101: 6 clock cycle. 110: 7 clock cycle. 111: 8 clock cycle.	
41h (111383h)	**REG111383**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_BCH_DEB_SEL	7	Debug mode signals mux out selection. 0: Ecc bch_top group0_dbus. 1: Ecc bch_top group1_dbus.	
	NC_DEB_SEL[2:0]	6:4	Debug mode signals mux out selection. 000: Disable. 001: Dpif_dbus. 010: Bramctrl_dbus. 011: Ecc_dbus. 100: Nfcas_dbus. 101: Instq_dbus.	
	NC_RD_LW[2:0]	3:1	Cycle count for RDJ low width.	
	NC_RD_HW[2]	0	See description of '111382h'.	
42h (111384h)	**REG111384**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	NC_STCHK_ERRH8	1	Status check for High 8 Data Bus. 0: OK. 1: Error.	
	NC_STCHK_ERRL8	0	Status check for Low 8 Data Bus. 0: OK. 1: Error.	
43h	**REG111386**	**7:0**	**Default : 0x00**	**Access : R/W**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111386h)	NC_AUXREG_ADR_WD[7:0]	7:0	Word address. 0x00 ~ 0x07 Command Registers (Hard Wired, Read Only). 0x08 ~ 0x0A Command Registers (R/W). 0x0B ~ 0x16 Address Register Sets (COL2+ROW4) x4. 0x18 Repeat count (10 bits). 0x19 Random data count. (10 bits, read data must be word alignment). ex: (1) read 6 bytes data => 0x44 should be 10h'006. ex: (2) read 7 bytes data => 0x44 should be 10h'008. ex: (3) write 6 bytes data => 0x44 should be 10h'006. ex: (4) write 7 bytes data => 0x44 should be 10h'007. 0x1A Random address offset. (8 bits, CIF_D address). 0x1B Status Check Mask(H8), Expect(L8). 0x1C Wait_Idle_Cnt (8 bits) for Wait_Idle_Inst. 0x20 ~ 0x2F Instruction Queue.	
44h (111388h)	**REG111388**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_AUXREG_DATA[7:0]	7:0	16 bit data port for Auxiliary Registers. 1. 0x44 Write can be consecutive once 0x43 set. 2. 0x44 Read CAN'T be consecutive due to riu_w as clock. Must write 0x43 first then read 0x44.	
44h (111389h)	**REG111389**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_AUXREG_DATA[15:8]	7:0	See description of '111388h'.	
45h (11138Ah)	**REG11138A**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_INST_HB_SEL	7	Instruction Queue Address Higher Bank selection while job start. 0: 00~0F. 1: 10~1F.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NC_NONEFF_NUM[1:0]	6:5	Set the number of none FFh"ECC_DI !=0xFFFF" for skipping ECC check(treated as blank data). 00: Skip ECC when there is 1 "ECC_DI != 0xFFFF". 01: Skip ECC when there is 2 "ECC_DI != 0xFFFF". 10: Skip ECC when there is 3 "ECC_DI != 0xFFFF". 11: Skip ECC when there is 4 "ECC_DI != 0xFFFF".	
	-	4	Reserved.	
	NC_DIR_DOWNSTREAM	3	NAND Flash data transfer direction for data FIFO(MIU). 0: Read from flash. 1: Write to flash.	
	NC_INST_HB_SEL_RPT	2	Instruction Queue Address Higher Bank selection while repeat. 0: 00~0F. 1: 10~1F.	
	NC_CIFC_ACCESS	1	NAND Controller directly access CIF_C. 0: Disable. 1: Enable.	
	NC_JOB_START	0	Start to execute instruction queue from 1st byte and exit until BREAK or error encountered.	
45h (11138Bh)	**REG11138B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CHK_ALLONE	1	Check if all one when page read.	
	CHK_ALLZERO	0	Check if all zero when page read.	
46h (11138Ch)	**REG11138C**	**7:0**	**Default : 0x00**	**Access : RO**
	NF_STCHK_DI_L8[7:0]	7:0	Low 8 Status Read from NAND Flash after issuing Check Status command "70".	
46h (11138Dh)	**REG11138D**	**7:0**	**Default : 0x00**	**Access : RO**
	NF_STCHK_DI_H8[7:0]	7:0	High 8 Status Read from NAND Flash after issuing Check Status command "70".	
47h	**REG11138E**	**7:0**	**Default : 0x00**	**Access : R/W**

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11138Eh)	NC_SER_PART_START_INDEX[0]	7	The sector index which to start this serial partial transaction when NC_SER_PART_MODE = 1. 6'h00: start from 1st sector. 6'h01: start from 2nd sector. 6'h02: start from 3rd sector. 6'h03: start from 4th sector. ..... 6'h3F: start from 63rd sector.	
	NC_SER_PART_CNT[5:0]	6:1	Transfer sector count to hit when NC_SER_PART_MODE = 1. (Note: totoal sector size should be less than page size). 6'h00: 1 sector. 6'h01: 2 sectors. 6'h02: 3 sectors. 6'h03: 4 sectors. ..... 6'h3F: 63 sectors.	
	NC_SER_PART_MODE	0	Serial Partial Mode. If set, in action SER_DATA_IN/SER_DATA_OUT, data transferred are sector size bytes xN.	
47h (11138Fh)	**REG11138F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	NC_SER_PART_START_INDEX[5:1]	4:0	See description of '11138Eh'.	
48h (111390h)	**REG111390**	**7:0**	**Default : 0x00**	**Access : R/W**
	SECTOR_SPARE_SIZE[7:0]	7:0	Spare area size of each sector in NAND FLASH. (must be word alignment, bit[0] should be zero).	
48h (111391h)	**REG111391**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	NC_ONE_COL_ADR	5	Flash Address contains only one column address cycle. 0: 2 column address bytes. 1: 1 column address byte (use MSB of column address register).	
	NC_AUTO_RANDOM_DIS	4	Disable hardware auto support Nand flash random read/write command (Random Data Read 05-E0, Random Data Input 85).	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NC_RANDOM_MODE	3	NAND random IN/OUT access enable. (Data transfer to CIFD or Spare MIU address, depend on reg_spare_dest).	
	NC_SPARE_ECC_BYPASS	2	Not protect ecc for spare data (only BCH used).	
	NC_SPARE_BYPASS	1	If set, dont write sapre area to CIFD (nc_cifc_wen tied to 1).	
	SPARE_DEST	0	NAND spare area data destination/source. 0: Transfer spare data to/from CIFD. 1: Transfer spare data to/from Ping-pong FIFO (MIU).	
49h (111392h)	**REG111392**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_SIZE[7:0]	7:0	Total spare area size of each page in NAND FLASH (must be word alignment, bit[0] should be zero).	
49h (111393h)	**REG111393**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPARE_SIZE[10:8]	2:0	See description of '111392h'.	
4Ah (111394h)	**REG111394**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_RPT_ADR2_SEL[1:0]	7:6	Select NAND Address2 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	
	NC_RPT_ADR1_SEL[2:0]	5:3	Select NAND Address1 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NC_RPT_ADR0_SEL[2:0]	2:0	Select NAND Address0 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	
4Ah (111395h)	**REG111395**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	NC_RPT_ADR3_SEL[2:0]	3:1	Select NAND Address3 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	
	NC_RPT_ADR2_SEL[2]	0	See description of '111394h'.	
4Bh (111396h)	**REG111396**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_EXPECT_DATA0[7:0]	7:0	NAND Signature check: expect data 0.	
4Bh (111397h)	**REG111397**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_EXPECT_DATA1[7:0]	7:0	NAND Signature check: expect data 1.	
4Ch (111398h)	**REG111398**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_COMP_ADDR0[7:0]	7:0	NAND Signature check: compare address 0.	
4Ch (111399h)	**REG111399**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_COMP_ADDR1[7:0]	7:0	NAND Signature check: compare address 1.	
4Dh (11139Ah)	**REG11139A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:5	Reserved.	
	SIGN_MISMATCH1_STS	4	NAND Signature check: Status check for data 1 (0: OK / 1: Mismatch).	
	SIGN_MISMATCH0_STS	3	NAND Signature check: Status check for data 0 (0: OK / 1: Mismatch).	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SIGN_CLR_STS	2	NAND Signature check: clear mismatch status.	
	SIGN_STOP_RUN	1	NAND Signature check: when data mismatch, stop run.	
	SIGN_CHECK_EN	0	NAND Signature check: enable.	
4Eh (11139Ch)	**REG11139C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_MEM_ADDR15_0[7:0]	7:0	NAND spare memory address[15:0] (byte offset).	
4Eh (11139Dh)	**REG11139D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_MEM_ADDR15_0[15:8]	7:0	See description of '11139Ch'.	
4Fh (11139Eh)	**REG11139E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_MEM_ADDR28_16[7:0]	7:0	NAND spare memory address[28:16] (byte offset).	
4Fh (11139Fh)	**REG11139F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPARE_MEM_ADDR28_16[12:8]	4:0	See description of '11139Eh'.	
50h (1113A0h)	**REG1113A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_ECCERR_NSTOP	7	NAND Flash "ECC Uncorrectable Error None Stop" while upstream (NAND -> MIU). 0: Disable. 1: Enable.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NC_ECC_MODE[3:0]	6:3	Select ecc algorithm mode. 4'b0000: 512 bytes, BCH code, 4 bit correct ability. 4'b0001: 512 bytes, BCH code, 8 bit correct ability. 4'b0010: 512 bytes, BCH code, 12 bit correct ability. 4'b0011: 512 bytes, BCH code, 16 bit correct ability. 4'b0100: 512 bytes, BCH code, 20 bit correct ability. 4'b0101: 512 bytes, BCH code, 24 bit correct ability. 4'b0110: 1K bytes, BCH code, 24 bit correct ability. 4'b0111: 1K bytes, BCH code, 32 bit correct ability. 4'b1000: 1K bytes, BCH code, 40 bit correct ability. 4'b1001: 1K bytes, BCH code, 60 bit correct ability. 4'b1010 ~ 4'b1111: reserved.	
	NC_PAGE_MODE[2:0]	2:0	Select nand page size. 3'b000: 512 bytes. 3'b001: 2K bytes. 3'b010: 4K bytes. 3'b011: 8K bytes. 3'b100: 16K bytes. 3'b101: 32K bytes. 3'b110 ~ 3'b111: reserved.	
50h (1113A1h)	**REG1113A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	NC_ECC_BYPASS	2	Bypass ECC (skip ECC check/generate) while data transfer upstream or downstream (redundant area CIF_C being written for upstream but not for downstream). 0: Disable. 1: Enable.	
	NC_ALLONE_ECC_CHECK	1	Enable NAND erase block ecc check.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NC_DYNGATED_EN	0	Dynamic Gated Clock enable. 0: Disable 1: enable.	
51h (1113A2h)	**REG1113A2**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	MAX_ECC_COR_NUM[5:0]	6:1	Maximum number of ECC correctable error bits in a sector during this DMA transaction.	
	ECC_ERROR_FLAG	0	ECC Uncorrectable error happened during this DMA transaction.	
51h (1113A3h)	**REG1113A3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	NC_ECC_SEC_CNT[5:0]	5:0	Current sector count when ECC uncorrectable error (NC_ECC_FLAG = 0x10) happens.	
52h (1113A4h)	**REG1113A4**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_ECC_COR_NUM[7:0]	7:0	Total sector count of which has ECC correctable error happened during this DMA transaction.	
52h (1113A5h)	**REG1113A5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DMA_ECC_COR_NUM[11:8]	3:0	See description of '1113A4h'.	
53h (1113A6h)	**REG1113A6**	**7:0**	**Default : 0x00**	**Access : RO**
	ECC_ERROR_NUM[5:0]	7:2	Number of correctable error.	
	NC_ECC_FLAG[1:0]	1:0	ECC Flag. 2'b00: No error encountered. 2'b01: Correctable error encountered. 2'b10: Uncorrectable error encountered. 2'b11: ECC code error. (RS code only).	
53h (1113A7h)	**REG1113A7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	NC_SEL_ECC_LOC[4:0]	4:0	Select ecc error location.	
54h (1113A8h)	**REG1113A8**	**7:0**	**Default : 0x00**	**Access : RO**
	ECC_ERROR_LOC[7:0]	7:0	ECC Error location.	
54h (1113A9h)	**REG1113A9**	**7:0**	**Default : 0x00**	**Access : RO**
	ECC_ERROR_LOC[15:8]	7:0	See description of '1113A8h'.	
55h (1113AAh)	**REG1113AA**	**7:0**	**Default : 0x05**	**Access : R/W**
	NF_READ_CMD0[7:0]	7:0	Configure command0 for auto random read.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (1113ABh)	**REG1113AB**	**7:0**	**Default : 0xE0**	**Access : R/W**
	NF_READ_CMD1[7:0]	7:0	Configure command1 for auto random read.	
56h (1113ACh)	**REG1113AC**	**7:0**	**Default : 0x85**	**Access : R/W**
	NF_WRITE_CMD[7:0]	7:0	Configure command for auto random write.	
56h (1113ADh)	**REG1113AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	NC_HWCMD_DELAY_NUM[3:0]	3:0	Cycle count for delay auto random command execute.	
57h (1113AEh)	**REG1113AE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RD_STS_CNT[2:0]	6:4	Nand read status phase selection. 0: Normal. 1: Delay 1 T. 2: Delay 2 T. 3~7: reserved.	
	-	3	Reserved.	
	DATA_LATCH_SEL[2:0]	2:0	Nand latch data phase selection. 0: Normal. 1: Delay 0.5 T. 2: Delay 1 T. 3: Delay 1.5 T. 4: Delay 2 T. 5~7: reserved.	
57h (1113AFh)	**REG1113AF**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEC_TURN_CNT[3:0]	7:4	Cycle count for delay sector end.	
	RD_DDR_TIMING[3:0]	3:0	Cycle count for fine tune ddr read path.	
58h (1113B0h)	**REG1113B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	NC_TOGGLE_READ_HOLD	4	Enable toggle nand read hold with CE_ high.	
	NC_PAD_FROM_DDR	3	Nand data input from macro.	
	-	2	Reserved.	
	NC_DDR_TOSH	1	Enable nand toggle mode.	
	NC_DDR_ONFI	0	Enbale nand onif ddr mode.	
58h (1113B1h)	**REG1113B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOGGLE_RDHOLD_CNT[7:0]	7:0	Cycle count for toggle nand read hold.	

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FCIE0 Register (Bank = 1113)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
59h (1113B2h)	**REG1113B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCS_CNT[3:0]	7:4	Cycle count for tCS timing.	
	TRR_CNT[3:0]	3:0	Cycle count for tRR timing.	
59h (1113B3h)	**REG1113B3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRAMBLE_EN	7	Enable randomizer function.	
	SEL_PAGE[6:0]	6:0	Select randomizer seed.	
5Ah (1113B4h)	**REG1113B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TCLHZ_CNT[3:0]	3:0	Cycle count for tCLHZ timing.	
5Ah (1113B5h)	**REG1113B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	TWHR_CNT[7:0]	7:0	Cycle count for tWHR timing.	
5Bh (1113B6h)	**REG1113B6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SER_DATA_IN_BASE_15_0[7:0]	7:0	Serail data input byte count[15:0].	
5Bh (1113B7h)	**REG1113B7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SER_DATA_IN_BASE_15_0[15:8]	7:0	See description of '1113B6h'.	
5Ch (1113B8h)	**REG1113B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SER_DATA_IN_BASE_31_16[7:0]	7:0	Serail data input byte count[31:16].	
5Ch (1113B9h)	**REG1113B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SER_DATA_IN_BASE_31_16[15:8]	7:0	See description of '1113B8h'.	
5Dh (1113BAh)	**REG1113BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	TADL_CNT[7:0]	7:0	Cycle count for tADL timing.	
5Dh (1113BBh)	**REG1113BB**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCWAW_CNT[7:0]	7:0	Cycle count for tCWAW timing.	

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FCIE1 Register (Bank = 1114)

FCIE1 Register (Bank = 1114)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
111480h~1114BFh	**Card CIFC command**	**7:0**	**Default : 0x00**	**Access : R/W**
	Card CIFC command	7:0	Card CIFC command FIFO : 64 bytes	
1114C0h~1114FFh	**Power Save command**	**7:0**	**Default : 0x00**	**Access : R/W**
	Power Save command	7:0	Power Save command FIFO : 128 bytes	

FCIE2 Register (Bank = 1115)

FCIE2 Register (Bank = 1115)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h~7Fh (111500h~1115FFH)	**CIFD_LSB_SRAM**	**7:0**	**Default : 0x00**	**Access : R/W**
	CIFD_LSB_SRAM	7:3	CIFD LSB 512-byte data buffer (0~255)	

FCIE3 Register (Bank = 1116)

FCIE3 Register (Bank = 1116)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h~7Fh (111600h~1116FFH)	**CIFD_MSB_SRAM**	**7:0**	**Default : 0x00**	**Access : R/W**
	CIFD_MSB_SRAM	7:3	CIFD MSB 512-byte data buffer (256~511)	

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MIIC0 Register (Bank = 1118)

MIIC0 Register (Bank = 1118)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (111800h)	**REG111800**	**7:0**	**Default : 0x01**	**Access : R/W**
	MIIC_CFG[7:0]	7:0	Miic configuration register. BIT[7]: reg_error_det_en. 0: Disable. 1: Enable. BIT[6]: reg_oen_push_en. 0: Disable. 1: Enable. BIT[5]: Enable filter. 0: Disable. 1: Enable. BIT[4]: Enable timeout interrupt. 0: Disable. 1: Enable. BIT[3]: Enable clock stretching. 0: Disable. 1: Enable. BIT[2]: Enable DMA. 0: Disable. 1: Enable. BIT[1]: Interrupt enable. 0: Disable. 1: Enable. BIT[0]: Reset. 0: Reset. 1: Not Reset.	
01h (111802h)	**REG111802**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	CMD_START	0	Miic command. [0]: Start.	
01h (111803h)	**REG111803**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	CMD_STOP	0	Miic command. [1]: Stop.	
02h (111804h)	**REG111804**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDATA[7:0]	7:0	I2C write data.	
02h	**REG111805**	**7:0**	**Default : 0x00**	**Access : RO**

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MIIC0 Register (Bank = 1118)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111805h)	-	7:1	Reserved.	
	WRITE_ACK	0	I2C ack for write data from slave iic.	
03h (111806h)	**REG111806**	**7:0**	**Default : 0x00**	**Access : RO**
	RDATA[7:0]	7:0	I2C read data.	
03h (111807h)	**REG111807**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:2	Reserved.	
	RDATA_EN1	1	I2C ack for read data to slave iic.	
	RDATA_EN	0	I2C read data trigger.	
04h (111808h)	**REG111808**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7:1	Reserved.	
	FLAG	0	Miic interrupt FLAG.	
05h (11180Ah)	**-**	**7:0**	**Default : -**	**Access : -**
	_	-	Reserved.	
05h (11180Bh)	**REG11180B**	**7:0**	**Default : 0x00**	**Access : RO**
	_	7	Reserved.	
	MIIC_INT_STATUS[14:8]	6:0	Int_status. [0]ic_start_det_intr, [1]ic_stop_det_intr, [2]ic_rx_done_intr, [3]ic_tx_done_intr, [4]clock_stretching_intr, [5]scl_error_inte, [6]time_out_intr,	
08h (111810h)	**REG111810**	**7:0**	**Default : 0x00**	**Access : R/W**
	STOP_CNT[7:0]	7:0	This register sets the SCL and SDA count for stop.	
08h (111811h)	**REG111811**	**7:0**	**Default : 0x00**	**Access : R/W**
	STOP_CNT[15:8]	7:0	See description of '111810h'.	
09h (111812h)	**REG111812**	**7:0**	**Default : 0x00**	**Access : R/W**
	HCNT[7:0]	7:0	This register sets the SCL clock high-period count.	
09h (111813h)	**REG111813**	**7:0**	**Default : 0x00**	**Access : R/W**
	HCNT[15:8]	7:0	See description of '111812h'.	
0Ah (111814h)	**REG111814**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCNT[7:0]	7:0	This register sets the SCL clock low-period count.	
0Ah	**REG111815**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIIC0 Register (Bank = 1118)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111815h)	LCNT[15:8]	7:0	See description of '111814h'.	
0Bh (111816h)	**REG111816**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDA_CNT[7:0]	7:0	This register sets the closk count between falling edge SCL and SDA.	
0Bh (111817h)	**REG111817**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDA_CNT[15:8]	7:0	See description of '111816h'.	
0Ch (111818h)	**REG111818**	**7:0**	**Default : 0x00**	**Access : R/W**
	START_CNT[7:0]	7:0	This register sets the SCL and SDA count for start.	
0Ch (111819h)	**REG111819**	**7:0**	**Default : 0x00**	**Access : R/W**
	START_CNT[15:8]	7:0	See description of '111818h'.	
0Dh (11181Ah)	**REG11181A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATA_LAT_CNT[7:0]	7:0	This register sets the data latch timing.	
0Dh (11181Bh)	**REG11181B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATA_LAT_CNT[15:8]	7:0	See description of '11181Ah'.	
0Eh (11181Ch)	**REG11181C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMEOUT_CNT[7:0]	7:0	This register sets timing delay of timeout interrupt occur.	
0Eh (11181Dh)	**REG11181D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMEOUT_CNT[15:8]	7:0	See description of '11181Ch'.	
0Fh (11181Eh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

MIIC1 Register (Bank = 1119)

MIIC1 Register (Bank = 1119)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**REG111900**	**7:0**	**Default : 0x01**	**Access : R/W**

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111900h)	MIIC_CFG[7:0]	7:0	Miic configuration register. BIT[7]: reg_error_det_en. 0: Disable. 1: Enable. BIT[6]: reg_oen_push_en. 0: Disable. 1: Enable. BIT[5]: Enable filter. 0: Disable. 1: Enable. BIT[4]: Enable timeout interrupt. 0: Disable. 1: Enable. BIT[3]: Enable clock stretching. 0: Disable. 1: Enable. BIT[2]: Enable DMA. 0: Disable. 1: Enable. BIT[1]: Interrupt enable. 0: Disable. 1: Enable. BIT[0]: Reset. 0: Reset. 1: Not Reset.	
01h (111902h)	**REG111902**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	CMD_START	0	Miic command. [0]: Start.	
01h (111903h)	**REG111903**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	CMD_STOP	0	Miic command. [1]: Stop.	
02h (111904h)	**REG111904**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDATA[7:0]	7:0	I2C write data.	
02h (111905h)	**REG111905**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	WRITE_ACK	0	I2C ack for write data from slave iic.	

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MIIC1 Register (Bank = 1119)

Index (Absolute)	Mnemonic	Bit	Description	
03h (111906h)	**REG111906**	**7:0**	**Default : 0x00**	**Access : RO**
	RDATA[7:0]	7:0	I2C read data.	
03h (111907h)	**REG111907**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RDATA_EN1	1	I2C ack for read data to slave iic.	
	RDATA_EN	0	I2C read data trigger.	
04h (111908h)	**REG111908**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FLAG	0	Miic interrupt FLAG.	
05h (11190Ah)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
05h (11190Bh)	**REG11190B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	MIIC_INT_STATUS[14:8]	6:0	Int_status. [0]ic_start_det_intr, [1]ic_stop_det_intr, [2]ic_rx_done_intr, [3]ic_tx_done_intr, [4]clock_stretching_intr, [5]scl_error_inte, [6]time_out_intr,	
08h (111910h)	**REG111910**	**7:0**	**Default : 0x00**	**Access : R/W**
	STOP_CNT[7:0]	7:0	This register sets the SCL and SDA count for stop.	
08h (111911h)	**REG111911**	**7:0**	**Default : 0x00**	**Access : R/W**
	STOP_CNT[15:8]	7:0	See description of '111910h'.	
09h (111912h)	**REG111912**	**7:0**	**Default : 0x00**	**Access : R/W**
	HCNT[7:0]	7:0	This register sets the SCL clock high-period count.	
09h (111913h)	**REG111913**	**7:0**	**Default : 0x00**	**Access : R/W**
	HCNT[15:8]	7:0	See description of '111912h'.	
0Ah (111914h)	**REG111914**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCNT[7:0]	7:0	This register sets the SCL clock low-period count.	
0Ah (111915h)	**REG111915**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCNT[15:8]	7:0	See description of '111914h'.	
0Bh	**REG111916**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111916h)	SDA_CNT[7:0]	7:0	This register sets the closk count between falling edge SCL and SDA.	
0Bh (111917h)	**REG111917**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDA_CNT[15:8]	7:0	See description of '111916h'.	
0Ch (111918h)	**REG111918**	**7:0**	**Default : 0x00**	**Access : R/W**
	START_CNT[7:0]	7:0	This register sets the SCL and SDA count for start.	
0Ch (111919h)	**REG111919**	**7:0**	**Default : 0x00**	**Access : R/W**
	START_CNT[15:8]	7:0	See description of '111918h'.	
0Dh (11191Ah)	**REG11191A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATA_LAT_CNT[7:0]	7:0	This register sets the data latch timing.	
0Dh (11191Bh)	**REG11191B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATA_LAT_CNT[15:8]	7:0	See description of '11191Ah'.	
0Eh (11191Ch)	**REG11191C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMEOUT_CNT[7:0]	7:0	This register sets timing delay of timeout interrupt occur.	
0Eh (11191Dh)	**REG11191D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMEOUT_CNT[15:8]	7:0	See description of '11191Ch'.	
0Fh (11191Eh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

MIIC2 Register (Bank = 111A)

MIIC2 Register (Bank = 111A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**REG111A00**	**7:0**	**Default : 0x01**	**Access : R/W**

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MIIC2 Register (Bank = 111A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111A00h)	MIIC_CFG[7:0]	7:0	Miic configuration register. BIT[7]: reg_error_det_en. 0: Disable. 1: Enable. BIT[6]: reg_oen_push_en. 0: Disable. 1: Enable. BIT[5]: Enable filter. 0: Disable. 1: Enable. BIT[4]: Enable timeout interrupt. 0: Disable. 1: Enable. BIT[3]: Enable clock stretching. 0: Disable. 1: Enable. BIT[2]: Enable DMA. 0: Disable. 1: Enable. BIT[1]: Interrupt enable. 0: Disable. 1: Enable. BIT[0]: Reset. 0: Reset. 1: Not Reset.	
01h (111A02h)	**REG111A02**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	CMD_START	0	Miic command. [0]: Start.	
01h (111A03h)	**REG111A03**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	CMD_STOP	0	Miic command. [1]: Stop.	
02h (111A04h)	**REG111A04**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDATA[7:0]	7:0	I2C write data.	
02h (111A05h)	**REG111A05**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	WRITE_ACK	0	I2C ack for write data from slave iic.	

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MIIC2 Register (Bank = 111A)

Index (Absolute)	Mnemonic	Bit	Description	
03h (111A06h)	**REG111A06**	**7:0**	**Default : 0x00**	**Access : RO**
	RDATA[7:0]	7:0	I2C read data.	
03h (111A07h)	**REG111A07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RDATA_EN1	1	I2C ack for read data to slave iic.	
	RDATA_EN	0	I2C read data trigger.	
04h (111A08h)	**REG111A08**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FLAG	0	Miic interrupt FLAG.	
05h (111A0Ah)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
05h (111A0Bh)	**REG111A0B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	MIIC_INT_STATUS[14:8]	6:0	Int_status. [0]ic_start_det_intr, [1]ic_stop_det_intr, [2]ic_rx_done_intr, [3]ic_tx_done_intr, [4]clock_stretching_intr, [5]scl_error_inte, [6]time_out_intr,	
08h (111A10h)	**REG111A10**	**7:0**	**Default : 0x00**	**Access : R/W**
	STOP_CNT[7:0]	7:0	This register sets the SCL and SDA count for stop.	
08h (111A11h)	**REG111A11**	**7:0**	**Default : 0x00**	**Access : R/W**
	STOP_CNT[15:8]	7:0	See description of '111A10h'.	
09h (111A12h)	**REG111A12**	**7:0**	**Default : 0x00**	**Access : R/W**
	HCNT[7:0]	7:0	This register sets the SCL clock high-period count.	
09h (111A13h)	**REG111A13**	**7:0**	**Default : 0x00**	**Access : R/W**
	HCNT[15:8]	7:0	See description of '111A12h'.	
0Ah (111A14h)	**REG111A14**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCNT[7:0]	7:0	This register sets the SCL clock low-period count.	
0Ah (111A15h)	**REG111A15**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCNT[15:8]	7:0	See description of '111A14h'.	
0Bh	**REG111A16**	**7:0**	**Default : 0x00**	**Access : R/W**

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MIIC2 Register (Bank = 111A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(111A16h)	SDA_CNT[7:0]	7:0	This register sets the closk count between falling edge SCL and SDA.	
0Bh (111A17h)	**REG111A17**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDA_CNT[15:8]	7:0	See description of '111A16h'.	
0Ch (111A18h)	**REG111A18**	**7:0**	**Default : 0x00**	**Access : R/W**
	START_CNT[7:0]	7:0	This register sets the SCL and SDA count for start.	
0Ch (111A19h)	**REG111A19**	**7:0**	**Default : 0x00**	**Access : R/W**
	START_CNT[15:8]	7:0	See description of '111A18h'.	
0Dh (111A1Ah)	**REG111A1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATA_LAT_CNT[7:0]	7:0	This register sets the data latch timing.	
0Dh (111A1Bh)	**REG111A1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATA_LAT_CNT[15:8]	7:0	See description of '111A1Ah'.	
0Eh (111A1Ch)	**REG111A1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMEOUT_CNT[7:0]	7:0	This register sets timing delay of timeout interrupt occur.	
0Eh (111A1Dh)	**REG111A1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMEOUT_CNT[15:8]	7:0	See description of '111A1Ch'.	
0Fh (111A1Eh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

BACH0 Register (Bank = 112A)

BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
112A00h	**REG112A00**	**15:0**	**Default : 0x0000**	**Access : R/W**
	SYS_RST_CTRL0[15:0]	15:0	0x00. [15] REG_RESET_AU_SYNC 1: RESET 0:Normal. [14] REG_RESET_DPGA_SYNC 1: RESET 0:Normal. [13] REG_RESET_SDM_SYNC 1: RESET 0:Normal.	
112A02h	**REG112A02**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	CKG_CTRL0[15:0]	15:0	0x02. 1: Gate the clock 0: enable the clock. [15] REG_AU_SYS_48M_GATE. [14] REG_AU_SYS_48M_INV_GATE. [13] REG_AU_DAC_GATE. [12] REG_AU_ADC_GATE. [11] REG_AU_SRC1_MAC_48M_GATE. [10] REG_AU_SRC2_MAC_48M_GATE. [9] REG_AU_SYS_216M_GATE. [8] REG_AU_SYS_432M_GATE. [7] REG_AU_CLK_PARSER_GATE. [6] REG_AU_SPDIF_TX_128FS_GATE. [5] REG_AU_SPDIF_RX_128FS_GATE. [1] REG_AU_SRC2_MAC_48M_DYNG_EN. [0] REG_AU_SRC1_MAC_48M_DYNG_EN.	
112A04h	**REG112A04**	**15:0**	**Default : 0x0000**	**Access : R/W**
	CKG_CTRL1[15:0]	15:0	0x04. 1: Invert the clock 0: Not invert the clock. [15] REG_AU_SYS_48M_INVT. [14] REG_AU_SYS_48M_INV_INVT. [13] REG_AU_DAC_INVT. [12] REG_AU_ADC_INVT. [11] REG_AU_SRC1_MAC_48M_INVT. [10] REG_AU_SRC2_MAC_48M_INVT. [9] REG_AU_SYS_216M_INVT. [8] REG_AU_SYS_432M_INVT. [7] REG_AU_CLK_PARSER_INVT. [6] REG_AU_SPDIF_TX_128FS_INVT. [5] REG_AU_SPDIF_RX_128FS_INVT. [0] REG_CKG_AU_SYS_216_SEL. 1: 432MHz 0:216MHz.	
112A06h	**REG112A06**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	TIMING_CTRL0[15:0]	15:0	0x06. [15:14] REG_SYNC_CLK1_SEL. Select the DAC CLOCK phase. [13:12] REG_SYNC_CLK2_SEL. Select the ADC CLOCK phase. . [9:8] REG_DEC_NUM. 0: Decimate ADC data to the sampling rate 8KHz. 1: Decimate ADC data to the sampling rate 16KHz. 2: Decimate ADC data to the sampling rate 32KHz. 3: Select Ch1/2 interpolated data as the input source of the decimation filter. . [7] REG_CH1_INT_128FS_SEL. 0: N.f SYNTH as the clock source. 1: FS SYNTH as the clock source. [6] REG_CH2_INT_128FS_SEL. 0: N.f SYNTH as the clock source. 1: FS SYNTH as the clock source. . [5] REG_EN_ASRC1. 1: Enable the ASRC path. 0: Disable the ASRC path. [4] REG_EN_INT_2. 1: Enable the Ch2 interpolation path. 0: Disable the Ch2 interpolation path. [3] REG_EN_INT_1. 1: Enable the Ch1 interpolation path. 0: Disable the Ch1 interpolation path. [2] REG_EN_DEC_2. 1: Enable the Ch2 CIC filter. 0: Disable the Ch2 CIC filter. [1] REG_EN_DEC_1. 1: Enable the Ch1 CIC filter1. 0: Disable the Ch1 CIC filter. [0] REG_EN_TIME_GEN. 1: Enable the Bach timing generator. 0: Disable the Bach timing generator.	
112A08h	**REG112A08**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	AUDIOBAND_CTRL0[15:0]	15:0	0x08. [15:14] REG_NF_SYNTH_3_RATE_SEL. 0: 125*48KHZ. 1: 125*32KHZ. 2: 125*16KHZ. 3: 125*8 KHZ. . [13] REG_CH1_INT_128FS_NF_SEL. 0: Sel NF_SYNTH_1 as the CH1 INT 128FS NF synthesizer source. 1: Sel NF_SYNTH_2 as the CH1 INT 128FS NF synthesizer source. [12] REG_CH1_INT_128FS_NF_SEL. 0: Sel NF_SYNTH_1 as the CH2 INT 128FS NF synthesizer source. 1: Sel NF_SYNTH_2 as the CH2 INT 128FS NF synthesizer source. . [11] REG_DEC_125FS_NF_SEL. 0: Sel NF_SYNTH_2 as the DEC 125FS NF synthesizer source. 1: Sel NF_SYNTH_3 as the DEC 125FS NF synthesizer source. . [10] REG_DMA1_RD_VALID_SEL. 0: Sel CH1_DAC_FS as DMA1 RD VALID. 1: Sel CH2_DAC_FS as DMA1 RD VALID. . [1] REG_CH12_SYNC_ENABLE. 1: Set 1'b1 as the Ch1 and Ch2 input sources are at the same sampling rate and synchronous. 0: Set 1'b0 as the Ch1 and Ch2 input sources are not at the same sampling rate and asynchronous. [0] REG_INI_SRAM. 1: Initialize the sram in the audioband of the Bach. 0: Normal function.	
112A0Ah	**REG112A0A**	**15:0**	**Default : 0x0000**	**Access : RO**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	AUDIOBAND_STS[15:0]	15:0	0x0A. [15] = REG_IIR_CH3_MACOVER; [14] = REG_IIR_CH2_MACOVER; [13] = REG_IIR_CH1_MACOVER; [12] = REG_IIR_CH4_MACOVER; [11:6] = QUANT_OUT_L[5:0]; [5:0] = QUANT_OUT_R[5:0];	
112A0Ch	**REG112A0C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	SDM_CTRL0[15:0]	15:0	0x0C. [0] REG_EN_SDM. 1: Enable the DAC SDM module. 0: Disable the DAC SDM module. . [1] REG_FS_SYNTH_SEL. . [3:2] REG_DAC_DIN_L_SEL. 0: Mute. 1: Ch1. 2: Ch2. 3: 0.5*(Ch1+Ch2). [5:4] REG_DAC_DIN_R_SEL. 0: Mute. 1: Ch2. 2: Ch1. 3: 0.5*(Ch1+Ch2). . [6] REG_FIX_MSB_EN. [11:7] REG_FIX_MSB_SEL. [12] REG_DITHER_EN. [15:13] REG_DITHER_SEL.	
112A0Eh	**REG112A0E**	**15:0**	**Default : 0x0000**	**Access : R/W**
	SDM_CTRL1[15:0]	15:0	0x0E. REG_SDM_OFFSET.	
112A10h	**REG112A10**	**15:0**	**Default : 0x007D**	**Access : R/W**
	NF_SYNTH_1_NF_H[15:0]	15:0	0x10. [15] REG_NF_SYNTH_1_TRIG. [13:0] REG_NF_SYNTH_1_VALUE[29:16].	
112A12h	**REG112A12**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	NF_SYNTH_1_NF_L[15:0]	15:0	0x12. [15:0] REG_NF_SYNTH_1_VALUE[15:0].	
112A14h	**REG112A14**	**15:0**	**Default : 0x00C0**	**Access : R/W**
	NF_SYNTH_2_NF_H[15:0]	15:0	0x14. [15] REG_NF_SYNTH_2_TRIG. [13:0] REG_NF_SYNTH_2_VALUE[29:16].	
112A16h	**REG112A16**	**15:0**	**Default : 0x0000**	**Access : R/W**
	NF_SYNTH_2_NF_L[15:0]	15:0	0x16. [15:0] REG_NF_SYNTH_2_VALUE[15:0].	
112A18h	**REG112A18**	**15:0**	**Default : 0x0000**	**Access : R/W**
	FS_SYNTH_CTRL0[15:0]	15:0	0x18. [0] REG_FS_SYNTH_EN. 1: Enable the FS synthesizer. 0: Disable the FS synthesizer. [1] REG_FS_SYNTH_SOURCE_SEL. 1: The SPDIF RX/External I2S RX interface's sampling rate is the synthesizer's source. 0: The BT interface's sampling rate is the synthesizer's source. . [6:4] REG_FS_SYNTH_BW. [7] REG_FS_SYNTH_FLOCK. . [8] REG_FS_SYNTH_RATE_SEL. 0: 256fs. 1: 128fs. 2: 64fs.	
112A1Ah	**REG112A1A**	**15:0**	**Default : 0x0000**	**Access : RO**
	FS_SYNTH_STS0[15:0]	15:0	0x1A. [0] REG_FS_SYNTH_NO_SIGNAL.	
112A1Ch	**REG112A1C**	**15:0**	**Default : 0x0000**	**Access : RO**
	FS_SYNTH_NF_H[15:0]	15:0	0x1C. REG_FS_SYNTH_NF[31:16].	
112A1Eh	**REG112A1E**	**15:0**	**Default : 0x0000**	**Access : RO**
	FS_SYNTH_NF_L[15:0]	15:0	0x1E. REG_FS_SYNTH_NF[15: 0].	
112A20h	**REG112A20**	**15:0**	**Default : 0x0000**	**Access : RO**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	FS_SYNTH_FRC[15:0]	15:0	0x20. FS_SYNTH_FRC.	
112A22h	**REG112A22**	**15:0**	**Default : 0x0000**	**Access : R/W**
	IIR_CTRL0[15:0]	15:0	0x22. [0] REG_IIR_CH1_EN. 1: Enable the DEC1 IIR filter. 0: Disable the DEC1 IIR filter. . [1] REG_IIR_CH2_EN. 1: Enable the DEC2 IIR filter. 0: Disable the DEC2 IIR filter. . [2] REG_IIR_CH3_EN. 1: Enable the DEC3 IIR filter. 0: Disable the DEC3 IIR filter. . [3] REG_IIR_CH4_EN. 1: Enable the DEC4 IIR filter. 0: Disable the DEC4 IIR filter. . [4] REG_IIR_BUF_INIT. 1: Intialize the buffer in the IIR module. . [5] REG_IIR_COEFF_WR. Write one filter coefficient to the buffer while the REG_IIR_COEFF_WR changes from low to high. . [15] REG_IIR_CLR_MACOVER. 1: Clear. 0: Normal.	
112A24h	**REG112A24**	**15:0**	**Default : 0x0000**	**Access : R/W**
	IIR_CTRL1[15:0]	15:0	0x24. [5:0]REG_IIR_COEFF_WR_ADDR. The buffer address which is to be written. [15:8] REG_IIR_COEFF_DATA[23:16].	
112A26h	**REG112A26**	**15:0**	**Default : 0x0000**	**Access : R/W**
	IIR_CTRL2[15:0]	15:0	0x26. [15:0] REG_IIR_COEFF_DATA[15:0].	
112A28h	**REG112A28**	**15:0**	**Default : 0x253C**	**Access : R/W**

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BACH0 Register (Bank = 112A)			
Index	**Mnemonic**	**Bit**	**Description**
	MIX_CTRL0[15:0]	15:0	0x28. [15] REG_SEL_DEC1_DOUT. For MUX_DMAWR_L. 0: Sel DEC1_OUT as DEC_L source. 1: Sel DEC2_OUT as DEC_L source. [14] REG_SEL_DEC2_DOUT. For MUX_DMAWR_R. 0: Sel DEC2_OUT as DEC_R source. 1: Sel DEC1_OUT as DEC_R source. . [13:12] REG_ST_MIX. [12] 1: Select DEC1 0:Mute. [13] 1: Select DBB DL 0:Mute. . [11:10] REG_AV_MIX. [10] 1: Select ST_MIX 0: Mute. [11] 1: Select DMA_RD Left channel 0:Mute. . [9 : 8] REG_DBB_UL_MIX. [8] 1: Select DEC1 0:Mute. [9] 1: SelectDMA_RD Right channel 0:Mute. . [7 : 6] REG_AMR_MIX. [6] 1: Select DEC1 0:Mute. [7] 1: Select DBB DL 0:Mute. . [5 : 4] REG_CH1_MUX_SEL. 0: BT DL data. 1: ASRC2. 2: SPDIF RX/External I2S RX Left data. 3: DMA_RD Left data. . [3 : 2] REG_CH2_MUX_SEL. 0: DBB DL data. 1: ASRC2. 2: SPDIF RX/External I2S RX Right data. 3: DMA_RD Right data. . [1 : 0] REG_DMAWR_MUX_SEL. 0: DEC1/DEC2. 1: Parser. 2: AMR_REC. 3: ASRC2.

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
112A30h	**REG112A30**	**15:0**	**Default : 0x0096**	**Access : R/W**

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BACH0 Register (Bank = 112A)			
Index	**Mnemonic**	**Bit**	**Description**
	BT_I2S_CTRL0[15:0]	15:0	0x30. [15] REG_BT_PCM_MODE. 0: I2S interface for the BT TRX. 1: PCM interface for the BT TRX. . [14] REG_BT_PCM_SYNC_SEL. In the PCM interface. 0: The MSB of the serial data is synchronous to the falling edge of the BT_I2S_TRX_WCK signal. 1: The MSB of the serial data is synchronous to the rising edge of the BT_I2S_TRX_WCK signal. . [13] REG_BT_I2S_TRX_BCK_INV. 0: Not invert the BT_I2S_TRX_BCK. 1: Invert the BT_I2S_TRX_BCK. . [12] REG_PAD_I2S_TRX_BCK_INV. 0: Not invert the PAD_I2S_TRX_BCK. 1: Invert the PAD_I2S_TRX_BCK. . [9] REG_BT_I2S_TX_DS2. [8] REG_BT_I2S_TX_DS. . [7] REG_BT_MS_MODE. 0: The BT TRX is in the slave mode. 1: The BT TRX is in the master mode. . [6:5] REG_BT_I2S_WDTH. In the I2S master mode. 0: 16 bit. 1: 24 bit. 2: 32 bit. . [4] REG_BT_I2S_FMT. In the I2S mode. 0: I2S-justified. 1: Left-justified. . [3] REG_BT_I2S_BCK_GEN_DIV2. 1: Force BCK to be divided by 2. 0: Normal function. . [2:1] REG_BT_I2S_BCK_GEN_SEL. In the master mode. 0: WCK is 8KHz.

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
112A32h	**REG112A32**	**15:0**	**Default : 0x2020**	**Access : R/W**
	BT_I2S_CTRL1[15:0]	15:0	0x32. [15] REG_BT_I2S_TRX_WCK_OEN. [14] REG_BT_I2S_TRX_BCK_OEN. [13] REG_BT_I2S_TRX_SDI_OEN. [12] REG_BT_I2S_TRX_SDO_OEN. [6] REG_BT_I2S_LOOPBACK_EN. [5] REG_BT_I2S_SOURCE_SEL. 0: The BT TRX interface is from/to the BT module in the chip. 1: The BT TRX interface is from/to the outside of the chip.	
112A34h	**REG112A34**	**15:0**	**Default : 0x0000**	**Access : RO**
	BT_I2S_STS[15:0]	15:0	0x34. [3:2] REG_BT_I2S_OUT_WDTH[1:0]; [1:0] REG_BT_I2S_IN_WDTH[1:0];	
112A36h	**REG112A36**	**15:0**	**Default : 0x0000**	**Access : R/W**
	RX_FIFO_CTRL0[15:0]	15:0	0x36. [5]REG_BT_RX_FIFO_EXTENSION. [4]REG_BT_RX_FIFO_STATUS_CLR_p.	
112A38h	**REG112A38**	**15:0**	**Default : 0x0000**	**Access : RO**
	RX_FIFO_STS[15:0]	15:0	0x38. [0] REG_BT_RX_FIFO_STATUS.	
112A80h	**REG112A80**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)			
Index	**Mnemonic**	**Bit**	**Description**
	DMA1_CTRL_0[15:0]	15:0	0x80 DMA1_CTRL_0. [15] REG_WR_UNDERRUN_INT_EN. DMA writer underrun threshold interrupt enable. 0 = disable. 1 = enable. [14] REG_WR_OVERRUN_INT_EN. DMA writer overrun threshold interrupt enable. 0 = disable. 1 = enable. [13] REG_RD_UNDERRUN_INT_EN. DMA reader underrun threshold interrupt enable. 0 = disable. 1 = enable. [12] REG_RD_OVERRUN_INT_EN. DMA reader overrun threshold interrupt enable. 0 = disable. 1 = enable. [11] REG_WR_FULL_INT_EN. DMA writer full interrupt enable. 0 = disable. 1 = enable. [10] REG_RD_EMPTY_INT_EN. DMA reader empty interrupt enable. 0 = disable. 1 = enable. [9] REG_WR_FULL_FLAG_CLR / REG_WR_LOCALBUF_FULL_CLR. DMA writer full flag clear / DMA writer local buffer full flag clear. 0 = normal. 1 = clear. [8] REG_RD_EMPTY_FLAG_CLR / REG_RD_LOCALBUF_EMPTY_CLR. DMA reader full flag clear / DMA reader local buffer full flag clear. 0 = normal. 1 = clear. [6] REG_SEL_TES_BUS. DMA test bus selection. 0: Select flag. 1: Select test bus. [5] REG_RD_LR_SWAP_EN. DMA reader left/right channel swap enable. 0 = normal. 1 = swap.

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
112A82h	**REG112A82**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_1[15:0]	15:0	0x82 DMA1_CTRL_1. [15] REG_RD_ENABLE. DMA reader enable. 0 = disable. 1 = enable. [14] REG_RD_INIT. DMA reader initial. 0 = normal. 1 = initial. [13] REG_RD_TRIG. DMA reader trigger. 0 = normal. 1 = trigger. [12] REG_RD_LEVEL_CNT_MASK. DMA reader level counter mask. 0 = normal. 1 = mask. [11:0] REG_RD_BASE_ADDR[11:0]. DMA reader base address [11:0].	
112A84h	**REG112A84**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_2[15:0]	15:0	0x84 DMA1_CTRL_2. [15] Reserved. [14:0] REG_RD_BASE_ADDR[14:0]. DMA reader base address [26:12].	
112A86h	**REG112A86**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_3[15:0]	15:0	0x86 DMA1_CTRL_3. [15:0] REG_RD_BUFF_SIZE. DMA reader buffer size.	
112A88h	**REG112A88**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_4[15:0]	15:0	0x88 DMA1_CTRL_4. [15:0] REG_RD_SIZE. DMA read size.	
112A8Ah	**REG112A8A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_5[15:0]	15:0	0x8A DMA1_CTRL_5. [15:0] REG_RD_OVERRUN_TH. DMA reader overrun threshold.	
112A8Ch	**REG112A8C**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA1_CTRL_6[15:0]	15:0	0x8C DMA1_CTRL_6. [15:0] REG_RD_UNDERRUN_TH. DMA reader underrun threshold.	
112A8Eh	**REG112A8E**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA1_CTRL_7[15:0]	15:0	0x8E DMA1_CTRL_7. [15:0] REG_RD_LEVEL_CNT. DMA reader level counter.	
112A90h	**REG112A90**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA1_CTRL_8[15:0]	15:0	0x90 DMA1_CTRL_8. [7] REG_RD_LOCALBUF_EMPTY. DMA reader local buffer empty flag. [6] REG_WR_LOCALBUF_FULL. DMA writer local buffer full flag. [5] REG_WR_FULL_FLAG. DMA writer full flag. [4] REG_RD_EMPTY_FLAG. DMA reader empty flag. [3] REG_RD_OVERRUN_FLAG. DMA reader overrun falg. [2] REG_RD_UNDERRUN_FLAG. DMA reader underrun flag. [1] REG_WR_OVERRUN_FLAG. DMA writer overrun flag. [0] REG_WR_UNDERRUN_FLAG. DMA writer underrun flag.	
112A92h	**REG112A92**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA1_CTRL_9[15:0]	15:0	0x92 DMA1_CTRL_9. [15] REG_WR_ENABLE. DMA writer enable. 0 = disable. 1 = enable. [14] REG_WR_INIT. DMA writer initial. 0 = normal. 1 = initial. [13] REG_WR_TRIG. DMA writer trigger. 0 = normal. 1 = trigger. [12] REG_WR_LEVEL_CNT_MASK. DMA writer level counter mask. 0 = normal. 1 = mask. [11:0] REG_WR_BASE_ADDR[11:0]. DMA writer base address [11:0].	
112A94h	**REG112A94**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_10[15:0]	15:0	0x94 DMA1_CTRL_10. [15] Reserved. [14:0] REG_WR_BASE_ADDR[14:0]. DMA writer base address [26:12].	
112A96h	**REG112A96**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_11[15:0]	15:0	0x96 DMA1_CTRL_11. [15:0] REG_WR_BUFF_SIZE. DMA writer buffer size.	
112A98h	**REG112A98**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_12[15:0]	15:0	0x98 DMA1_CTRL_12. [15:0] REG_WR_SIZE. DMA write size.	
112A9Ah	**REG112A9A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_13[15:0]	15:0	0x9A DMA1_CTRL_13. [15:0] REG_WR_OVERRUN_TH. DMA writer overrun threshold.	
112A9Ch	**REG112A9C**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA1_CTRL_14[15:0]	15:0	0x9C DMA1_CTRL_14. [15:0] REG_WR_UNDERRUN_TH. DMA writer underrun threshold.	
112A9Eh	**REG112A9E**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA1_CTRL_15[15:0]	15:0	0x9E DMA1_CTRL_15. [15:0] REG_WR_LEVEL_CNT. DMA writer level counter.	
112AA0h	**REG112AA0**	**15:0**	**Default : 0x0000**	**Access : R/W**
	TIMING_CTRL1[15:0]	15:0	0xA0. [15] REG_CH1_INT_CNT_SYNC_SEL. [14] REG_CH2_INT_CNT_SYNC_SEL. [13] REG_ASRC2_CH1_INT_CNT_SYNC_SEL. [12] REG_ASRC2_CH2_INT_CNT_SYNC_SEL. [11] REG_EN_ASRC3_p. [10] REG_EN_ASRC4_p. [9:8] REG_DEC_NUM2. [7] REG_ASRC2_CH1_INT_128FS_SEL. [6] REG_ASRC2_CH2_INT_128FS_SEL. [5] REG_EN_ASRC2_p. [4] REG_EN_ASRC2_INT_1_p. [3] REG_EN_ASRC2_INT_2_p. [2] REG_EN_ASRC2_DEC_1_p. [1] REG_EN_ASRC2_DEC_2_p.	
112AA2h	**REG112AA2**	**15:0**	**Default : 0xEA82**	**Access : R/W**
	AUDIOBAND_CTRL1[15:0]	15:0	0xA2. [15:14]REG_ASRC2_CH_MUX_SEL. [13:12]REG_SDM_DWA_DATAIN_L_SEL. [11:10]REG_SDM_DWA_DATAIN_R_SEL. [9: 8]REG_S2M_ASRC2_CH1_SEL. [7: 6]REG_S2M_ASRC2_CH2_SEL. [5] REG_DMARD_L_DPGA_DIN_SEL. [4] REG_DMARD_R_DPGA_DIN_SEL. [3] Reserved. [2] REG_ASRC2_FS_SYNTH_SEL_p. [1] REG_ASRC2_CH12_SYNC_ENABLE.	
112AA4h	**REG112AA4**	**15:0**	**Default : 0x007D**	**Access : R/W**
	NF_SYNTH_4_NF_H[15:0]	15:0	0xA4. [15] REG_NF_SYNTH_4_TRIG. [13:0] REG_NF_SYNTH_4_VALUE[29:16].	

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
112AA6h	**REG112AA6**	**15:0**	**Default : 0x0000**	**Access : R/W**
	NF_SYNTH_4_NF_L[15:0]	15:0	0xA6. [15:0] REG_NF_SYNTH_4_VALUE[15:0].	
112AA8h	**REG112AA8**	**15:0**	**Default : 0x00C0**	**Access : R/W**
	NF_SYNTH_5_NF_H[15:0]	15:0	0xA8. [15] REG_NF_SYNTH_5_TRIG. [13:0] REG_NF_SYNTH_5_VALUE[29:16].	
112AAAh	**REG112AAA**	**15:0**	**Default : 0x0000**	**Access : R/W**
	NF_SYNTH_5_NF_L[15:0]	15:0	0xAA. [15:0] REG_NF_SYNTH_5_VALUE[15:0].	
112AACh	**REG112AAC**	**15:0**	**Default : 0x0000**	**Access : R/W**
	INT_CTRL[15:0]	15:0	0xAC. [15] Interrupt test Mode. 1: Test mode 0:normal mode. [14] Level interrupt test value. [13] Edge interrupt test value. [4] pasA_mis_shot (edge). [2] AU_PARSER_INT Enable (level). [1] AU_DMA_INT Enable (level). [0] AU_DPGA_INT Enable (level).	
112AB2h	**REG112AB2**	**15:0**	**Default : 0xAA00**	**Access : R/W**
	SINE_GEN_CTRL0[15:0]	15:0	0xB2. [15:14] REG_INT1_MIX_CTRL. [13:12] REG_INT2_MIX_CTRL. [11:10] REG_ASRC2_INT1_MIX_CTRL. [9:8] REG_ASRC2_INT2_MIX_CTRL. [7]REG_PGA1_SWAP. [6]REG_PGA2_SWAP. [5] Reserved. [4]REG_EN_DIT_IIR. [3]REG_EN_DIT_SRC. [2]REG_EN_DIT_SINE. [1] REG_CH2_SIN_GEN_EN. [0] REG_CH1_SIN_GEN_EN.	
112AB4h	**REG112AB4**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	SINE_GEN_CTRL1[15:0]	15:0	0xB4. [15:12] REG_SINE_GEN_CH2_GAIN. Gain = -6db * REG_SINE_GEN_CH2_GAIN. [11: 8] REG_SINE_GEN_CH2_FREQ. Under FS = 48Khz. 4'h0: 250Hz. 4'h1: 500Hz. 4'h2: 1000Hz. 4'h3: 1500Hz. 4'h4: 2000Hz. 4'h5: 3000Hz. 4'h6: 4000Hz. 4'h7: 6000Hz. 4'h8:8000Hz. 4'h9: 12000Hz. otherst: 16000Hz. . [7: 4] REG_SINE_GEN_CH1_GAIN. Gain = -6db * REG_SINE_GEN_CH1_GAIN. [3: 0]REG_SINE_GEN_CH1_FREQ. Under FS = 48Khz. 4'h0: 250Hz. 4'h1: 500Hz. 4'h2: 1000Hz. 4'h3: 1500Hz. 4'h4: 2000Hz. 4'h5: 3000Hz. 4'h6: 4000Hz. 4'h7: 6000Hz. 4'h8:8000Hz. 4'h9: 12000Hz. otherst: 16000Hz.	
112AB6h	**REG112AB6**	**15:0**	**Default : 0x0000**	**Access : R/W**
	TEST_CTRL0[15:0]	15:0	0xB6. [0] REG_DAC_TEST_EN. [1] REG_SDM_TEST_EN. [2] REG_SDM_SFT_DIS. [3] REG_SRAM_CG_EN. [8: 4] REG_TESTCLK_SEL. [15:12] REG_TESTBUS_SEL.	
112AB8h	**REG112AB8**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	RESERVED_0XB8[15:0]	15:0	0xB8. Reserved.	
112ABAh	**REG112ABA**	**15:0**	**Default : 0x0000**	**Access : R/W**
	RESERVED_0XBA[15:0]	15:0	0xBA. Reserved.	
112ABCh	**REG112ABC**	**15:0**	**Default : 0x0000**	**Access : R/W**
	RESERVED_0XBC[15:0]	15:0	0xBC. Reserved.	
112ABEh	**REG112ABE**	**15:0**	**Default : 0x0000**	**Access : R/W**
	RESERVED_0XBE[15:0]	15:0	0xBE.	
112AC0h	**REG112AC0**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)			
Index	**Mnemonic**	**Bit**	**Description**
	DMA2_CTRL_0[15:0]	15:0	0xC0 DMA2_CTRL_0. [15] REG_WR_UNDERRUN_INT_EN. DMA writer underrun threshold interrupt enable. 0 = disable. 1 = enable. [14] REG_WR_OVERRUN_INT_EN. DMA writer overrun threshold interrupt enable. 0 = disable. 1 = enable. [13] REG_RD_UNDERRUN_INT_EN. DMA reader underrun threshold interrupt enable. 0 = disable. 1 = enable. [12] REG_RD_OVERRUN_INT_EN. DMA reader overrun threshold interrupt enable. 0 = disable. 1 = enable. [11] REG_WR_FULL_INT_EN. DMA writer full interrupt enable. 0 = disable. 1 = enable. [10] REG_RD_EMPTY_INT_EN. DMA reader empty interrupt enable. 0 = disable. 1 = enable. [9] REG_WR_FULL_FLAG_CLR / REG_WR_LOCALBUF_FULL_CLR. DMA writer full flag clear / DMA writer local buffer full flag clear. 0 = normal. 1 = clear. [8] REG_RD_EMPTY_FLAG_CLR / REG_RD_LOCALBUF_EMPTY_CLR. DMA reader full flag clear / DMA reader local buffer full flag clear. 0 = normal. 1 = clear. [6] REG_SEL_TES_BUS. DMA test bus selection. 0: Select flag. 1: Select test bus. [5] REG_RD_LR_SWAP_EN. DMA reader left/right channel swap enable. 0 = normal. 1 = swap.

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
112AC2h	**REG112AC2**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_1[15:0]	15:0	0xC2 DMA2_CTRL_1. [15] REG_RD_ENABLE. DMA reader enable. 0 = disable. 1 = enable. [14] REG_RD_INIT. DMA reader initial. 0 = normal. 1 = initial. [13] REG_RD_TRIG. DMA reader trigger. 0 = normal. 1 = trigger. [12] REG_RD_LEVEL_CNT_MASK. DMA reader level counter mask. 0 = normal. 1 = mask. [11:0] REG_RD_BASE_ADDR[11:0]. DMA reader base address [11:0].	
112AC4h	**REG112AC4**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_2[15:0]	15:0	0xC4 DMA2_CTRL_2. [15] reserved. [14:0] REG_RD_BASE_ADDR[14:0]. DMA reader base address [26:12].	
112AC6h	**REG112AC6**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_3[15:0]	15:0	0xC6 DMA2_CTRL_3. [15:0] REG_RD_BUFF_SIZE. DMA reader buffer size.	
112AC8h	**REG112AC8**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_4[15:0]	15:0	0xC8 DMA2_CTRL_4. [15:0] REG_RD_SIZE. DMA read size.	
112ACAh	**REG112ACA**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_5[15:0]	15:0	0xCA DMA2_CTRL_5. [15:0] REG_RD_OVERRUN_TH. DMA reader overrun threshold.	
112ACCh	**REG112ACC**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA2_CTRL_6[15:0]	15:0	0xCC DMA2_CTRL_6. [15:0] REG_RD_UNDERRUN_TH. DMA reader underrun threshold.	
112ACEh	**REG112ACE**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA2_CTRL_7[15:0]	15:0	0xCE DMA2_CTRL_7. [15:0] REG_RD_LEVEL_CNT. DMA reader level counter.	
112AD0h	**REG112AD0**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA2_CTRL_8[15:0]	15:0	0xD0 DMA2_CTRL_8. [7] REG_RD_LOCALBUF_EMPTY. DMA reader local buffer empty flag. [6] REG_WR_LOCALBUF_FULL. DMA writer local buffer full flag. [5] REG_WR_FULL_FLAG. DMA writer full flag. [4] REG_RD_EMPTY_FLAG. DMA reader empty flag. [3] REG_RD_OVERRUN_FLAG. DMA reader overrun falg. [2] REG_RD_UNDERRUN_FLAG. DMA reader underrun flag. [1] REG_WR_OVERRUN_FLAG. DMA writer overrun flag. [0] REG_WR_UNDERRUN_FLAG. DMA writer underrun flag.	
112AD2h	**REG112AD2**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA2_CTRL_9[15:0]	15:0	0xD2 DMA2_CTRL_9. [15] REG_WR_ENABLE. DMA writer enable. 0 = disable. 1 = enable. [14] REG_WR_INIT. DMA writer initial. 0 = normal. 1 = initial. [13] REG_WR_TRIG. DMA writer trigger. 0 = normal. 1 = trigger. [12] REG_WR_LEVEL_CNT_MASK. DMA writer level counter mask. 0 = normal. 1 = mask. [11:0] REG_WR_BASE_ADDR[11:0]. DMA writer base address [11:0].	
112AD4h	**REG112AD4**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_10[15:0]	15:0	0xD4 DMA2_CTRL_10. [15] reserved. [14:0] REG_WR_BASE_ADDR[14:0]. DMA writer base address [24:12].	
112AD6h	**REG112AD6**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_11[15:0]	15:0	0xD6 DMA2_CTRL_11. [15:0] REG_WR_BUFF_SIZE. DMA writer buffer size.	
112AD8h	**REG112AD8**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_12[15:0]	15:0	0xD8 DMA2_CTRL_12. [15:0] REG_WR_SIZE. DMA write size.	
112ADAh	**REG112ADA**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA2_CTRL_13[15:0]	15:0	0xDA DMA2_CTRL_13. [15:0] REG_WR_OVERRUN_TH. DMA writer overrun threshold.	
112ADCh	**REG112ADC**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA2_CTRL_14[15:0]	15:0	0xDC DMA2_CTRL_14. [15:0] REG_WR_UNDERRUN_TH. DMA writer underrun threshold.	
112ADEh	**REG112ADE**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA2_CTRL_15[15:0]	15:0	0xDE DMA2_CTRL_15. [15:0] REG_WR_LEVEL_CNT. DMA writer level counter.	
112AE0h	**REG112AE0**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL0[15:0]	15:0	0xE0 DMA_TEST_CTRL0. [0] DMA_TEST_WR_EN. DMA test wrtier enable. [1] DMA_TEST_WR. DMA test writer. [3:2] DMA_TEST_WR_SEL. DMA test writer selection. [4] DMA_TEST_RD_EN. DMA test reader enable. [5] DMA_TEST_RD. DMA test reader. [7:6] DMA_TEST_RD_SEL. DMA test reader selection.	
112AE2h	**REG112AE2**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL1[15:0]	15:0	0xE2 DMA_TEST_CTRL1. [15:0] DMA_WR_DATA_L_MUX. DMA writer data left echannel value.	
112AE4h	**REG112AE4**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL2[15:0]	15:0	0xE4 DMA_TEST_CTRL2. [15:0] DMA_WR_DATA_R_MUX. DMA writer data right echannel value.	
112AE6h	**REG112AE6**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA_TEST_CTRL3[15:0]	15:0	0xE6 DMA_TEST_CTRL3. [15:0] DMA_RD_DATA_L. DMA read DATA left channel.	
112AE8h	**REG112AE8**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA_TEST_CTRL4[15:0]	15:0	0xE8 DMA_TEST_CTRL4. [15:0] DMA_RD_DATA_R. DMA read DATA right channel.	
112AEAh	**REG112AEA**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA_TEST_CTRL5[15:0]	15:0	0xEA DMA_TEST_CTRL5. DMA1 sine generator setting. [15] REG_SINE_GEN_EN. Sine generator enable. [14] REG_SINE_GEN_L. [13] REG_SINE_GEN_R. Sine generate left/right channel enable. [12] REG_SINE_GEN_RD_WR. Sine generator select reader or writer. 0 = reader. 1 = writer. [11] REG_DMA_TEST_SEL_H. DMA test bus select high word. 0 = low word. 1 = high word. [10:8] REG_DMA_TEST_SEL. DMA test bus selection. [3:0] REG_SINE_GEN_FREQ. Sine generator frequency selection. [7:4] REG_SINE_GEN_GAIN. Sine generator gain selection.	
112AECh	**REG112AEC**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMA_TEST_CTRL6[15:0]	15:0	0xEC DMA_TEST_CTRL6. DMA2 sine generator setting. [15] REG_SINE_GEN_EN. Sine generator enable. [14] REG_SINE_GEN_L. [13] REG_SINE_GEN_R. Sine generate left/right channel enable. [12] REG_SINE_GEN_RD_WR. Sine generator select reader or writer. 0 = reader. 1 = writer. [11] REG_DMA_TEST_SEL_H. DMA test bus select high word. 0 = low word. 1 = high word. [10:8] REG_DMA_TEST_SEL. DMA test bus selection. [3:0] REG_SINE_GEN_FREQ. Sine generator frequency selection. [7:4] REG_SINE_GEN_GAIN. Sine generator gain selection.	
112AEEh	**REG112AEE**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL7[15:0]	15:0	0xEE DMA_TEST_CTRL7. [15] REG_FORCE_MREQ_ON. Force clock miu to be always turned on. [5] DMA2MI_2_SEL. Dma2 miu port selection. [4] DMA2MI_1_SEL. Dma1 miu port selection. [3] REG_DMA2_WR_MODE. Dma2 writer path mode selection (1 for mono & 0 for stereo). [2] REG_DMA1_WR_MODE. Dma1 writer path mode selection (1 for mono & 0 for stereo). [1] REG_DMA2_WR_FIFO_REWRITE_CLR. [0] REG_DMA1_WR_FIFO_REWRITE_CLR.	
112AF0h	**REG112AF0**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TOP_CTRL0[15:0]	15:0	0xF0 DMA_TOP_CTRL0. [5:0] DMA2MI_1_MOBF_IDX.	

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BACH0 Register (Bank = 112A)				
Index	**Mnemonic**	**Bit**	**Description**	
112AF2h	**REG112AF2**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TOP_CTRL1[15:0]	15:0	0xF2 DMA_TOP_CTRL1. [5:0] DMA2MI_2_MOBF_IDX.	
112AF4h	**REG112AF4**	**15:0**	**Default : 0x0000**	**Access : RO**
	RESERVED_0XF4[15:0]	15:0	0xF4.	
112AF6h	**REG112AF6**	**15:0**	**Default : 0x0000**	**Access : RO**
	RESERVED_0XF6[15:0]	15:0	0xF6.	
112AF8h	**REG112AF8**	**15:0**	**Default : 0x0000**	**Access : RO**
	RESERVED_0XF8[15:0]	15:0	0xF8.	
112AFAh	**REG112AFA**	**15:0**	**Default : 0x0000**	**Access : RO**
	RESERVED_0XFA[15:0]	15:0	0xFA.	
112AFCh	**REG112AFC**	**15:0**	**Default : 0x0000**	**Access : RO**
	RESERVED_0XFC[15:0]	15:0	0xFC.	
112AFEh	**REG112AFE**	**15:0**	**Default : 0x0000**	**Access : RO**
	RESERVED_0XFE[15:0]	15:0	0xFE.	

BACH1 Register (Bank = 112B)

BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
112B00h	**REG112B00**	**15:0**	**Default : 0x0000**	**Access : R/W**
	AUDIOBAND_CTRL2[15:0]	15:0	0x00. [15:14] REG_DEC_NUM3. [13:12] REG_DEC_NUM4. [11:10] REG_INT3_MIX_CTRL. [9:8] REG_INT4_MIX_CTRL. [7:6] REG_ASRC2_INT3_MIX_CTRL. [5:4] REG_ASRC2_INT4_MIX_CTRL. [3] REG_EN_DEC_3_p. [2] REG_EN_DEC_4_p. [1] REG_EN_ASRC2_DEC_3_p. [0] REG_EN_ASRC2_DEC_4_p.	
112B02h	**REG112B02**	**15:0**	**Default : 0x05A0**	**Access : R/W**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	AUDIOBAND_CTRL3[15:0]	15:0	0x02. [15] REG_PGA3_SWAP. [14] REG_PGA4_SWAP. [13] REG_SDM_SEL3. [12] REG_SDM_SEL4. [11:10] REG_DAC_DIN_L_SEL2. [9:8] REG_DAC_DIN_R_SEL2. [7:6] REG_SDM_DWA_DATAIN_L_SEL2. [5:4] REG_SDM_DWA_DATAIN_R_SEL2. [3] REG_DEC_125FS_NF_SEL2. [2] REG_ASRC2_DEC_125FS_NF_SEL. [1] REG_ASRC2_DEC_125FS_NF_SEL2.	
112B04h	**REG112B04**	**15:0**	**Default : 0x0080**	**Access : R/W**
	NF_SYNTH_3_NF_H[15:0]	15:0	0x04. [15] REG_NF_SYNTH_3_TRIG. [13:0] REG_NF_SYNTH_3_VALUE[29:16].	
112B06h	**REG112B06**	**15:0**	**Default : 0x0000**	**Access : R/W**
	NF_SYNTH_3_NF_L[15:0]	15:0	0x06. [15:0] REG_NF_SYNTH_3_VALUE[15:0].	
112B08h	**REG112B08**	**15:0**	**Default : 0x0080**	**Access : R/W**
	NF_SYNTH_6_NF_H[15:0]	15:0	0x08. [15] REG_NF_SYNTH_6_TRIG. [13:0] REG_NF_SYNTH_6_VALUE[29:16].	
112B0Ah	**REG112B0A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	NF_SYNTH_6_NF_L[15:0]	15:0	0x0A. [15:0] REG_NF_SYNTH_6_VALUE[15:0].	
112B0Ch	**REG112B0C**	**15:0**	**Default : 0x0465**	**Access : R/W**
	NF_SYNTH_7_NF_H[15:0]	15:0	0x0C. [15] REG_NF_SYNTH_7_TRIG. [13:0] REG_NF_SYNTH_7_VALUE[29:16].	
112B0Eh	**REG112B0E**	**15:0**	**Default : 0x0000**	**Access : R/W**
	NF_SYNTH_7_NF_L[15:0]	15:0	0x0E. [15:0] REG_NF_SYNTH_7_VALUE[15:0].	
112B10h	**REG112B10**	**15:0**	**Default : 0x0000**	**Access : R/W**
	SPDIF_TX_CTRL0[15:0]	15:0	0x10. [15:8] REG_SPDIF_OUT_CS1. [7:0] REG_SPDIF_OUT_CS0.	
112B12h	**REG112B12**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	SPDIF_TX_CTRL1[15:0]	15:0	0x12. [15:8] REG_SPDIF_OUT_CS3. [7:0] REG_SPDIF_OUT_CS2.	
112B14h	**REG112B14**	**15:0**	**Default : 0x0000**	**Access : R/W**
	SPDIF_TX_CTRL2[15:0]	15:0	0x14. [15] REG_TX_FIFO_EX. [14] REG_TX_FIFO_CLR. [13] REG_CNT_RST. [12] REG_SPDIF_FIX. [11] REG_SPDIF_FIX_VAL. [10] REG_SPDIF_CFG. [9] REG_SPDIF_VALIDITY. [8] REG_SPDIF_EN_ABS. [7:0] REG_SPDIF_OUT_CS4.	
112B16h	**REG112B16**	**15:0**	**Default : 0x0000**	**Access : RO**
	SPDIF_TX_STS[15:0]	15:0	0x16. [15:4] SPDIF_DATA_L[23:12]. [3] SPDIF_DATA_V. [2] SPDIN_TX_VALID. [1] SPDIF_OUT. [0] TX_FIFO_STATUS.	
112B18h	**REG112B18**	**15:0**	**Default : 0x3017**	**Access : R/W**
	SPDIF_RX_CTRL0[15:0]	15:0	0x18. [15:12] COARSE_K. [11:8] PHASE_OFFSET. [7:4] FDC_KD_REG. [3:1] PD_RESOLUTION. [0] ENABLE_CDR.	
112B1Ah	**REG112B1A**	**15:0**	**Default : 0x0002**	**Access : R/W**
	SPDIF_RX_CTRL1[15:0]	15:0	0x1A. [3] REG_RX_FIFO_EX. [2] REG_RX_FIFO_CLR. [1] REG_SPDIF_IN_BLOCK_NO_CHECK. [0] PHASE_TRACKER.	
112B1Ch	**REG112B1C**	**15:0**	**Default : 0x0000**	**Access : RO**
	SPDIF_RX_STS0[15:0]	15:0	0x1C. [15] NO_SIGNAL_IN. [14:0] SPDIF_N_F_STATUS.	
112B1Eh	**REG112B1E**	**15:0**	**Default : 0x0000**	**Access : RO**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	SPDIF_RX_STS1[15:0]	15:0	0x1E. [15:0] SPDIN_CS[15:0].	
112B20h	**REG112B20**	**15:0**	**Default : 0x0000**	**Access : RO**
	SPDIF_RX_STS2[15:0]	15:0	0x20. [15:0] SPDIN_CS[31:16].	
112B22h	**REG112B22**	**15:0**	**Default : 0x0000**	**Access : RO**
	SPDIF_RX_STS3[15:0]	15:0	0x22. [15:8] SPDIN_CS[39:32]. [7] SPDIN_LDATA[23]. [6] RX_FIFO_STATUS. [5] SPDIN_WE. [4] COARSE_NORMAL_STATUS. [3] CRT_SPDIF_RX_256FS. [2] CRT_SPDIF_RX_128FS. [1] RECOVERY_DATA. [0] SPDIN_ERROR.	
112B24h	**REG112B24**	**15:0**	**Default : 0x3180**	**Access : R/W**
	DBB_I2S_CTRL[15:0]	15:0	0x24. [15] REG_DBB_PCM_MODE. 1: PCM 0:I2S. [14] REG_DBB_PCM_SYNC_SEL. 1: Data align to rising edge of SYNC pulse 0:falling. [13] REG_DBB_I2S_FMT. 1: Left-justify 0:I2S. [12] REG_DBB_MS_MODE. 1: Master 0:Slave. [11:10] REG_DBB_I2S_WDTH. 0: 16-bit 1:24-bit 2:32-bit. [9] REG_DBB_I2S_BCK_GEN_DIV2. [8:7] REG_DBB_I2S_BCK_GEN_SEL. 0: 8K 1:16K 2:32K 3:48K. [6] REG_DBB_I2S_BCK_GEN_UPDATE. [5] REG_DBB_I2S_TRX_BCK_INV. [4] REG_DBB_RX_FIFO_STATUS_CLR. [3] REG_DBB_RX_FIFO_EXTENSION. [2] REG_DBB_TX_FIFO_STATUS_CLR. [1] REG_DBB_TX_FIFO_EXTENSION. [0] REG_DBB_I2S_LOOPBACK_EN.	
112B26h	**REG112B26**	**15:0**	**Default : 0x3184**	**Access : R/W**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	CODEC_I2S_CTRL[15:0]	15:0	0x26. [15] REG_CODEC_PCM_MODE. 1: PCM 0:I2S. [14] REG_CODEC_PCM_SYNC_SEL. 1: Data align to rising edge of SYNC pulse 0:falling. [13] REG_CODEC_I2S_FMT. 1: Left-justify 0:I2S. [12] REG_CODEC_MS_MODE. 1: Master 0:Slave. [11:10] REG_CODEC_I2S_WDTH. 0: 16-bit 1:24-bit 2:32-bit. [9] REG_CODEC_I2S_BCK_GEN_DIV2. [8:7] REG_CODEC_I2S_BCK_GEN_SEL. 0: 8K 1:16K 2:32K 3:48K. [6] REG_CODEC_I2S_BCK_GEN_UPDATE. [5] REG_CODEC_I2S_TRX_BCK_INV. [4] REG_CODEC_TX_FIFO_STATUS_CLR. [3] REG_CODEC_TX_FIFO_EXTENSION. [2] REG_CODEC_FS_SEL. 1: DEC3 0:ASRC2 DEC3.	
112B28h	**REG112B28**	**15:0**	**Default : 0x2180**	**Access : R/W**
	EXT_I2S_CTRL[15:0]	15:0	0x28. [13] REG_EXT_I2S_FMT. 1: Left-justify 0:I2S. [12] REG_EXT_MS_MODE. 1: Master 0:Slave. [11:10] REG_EXT_I2S_WDTH. 0: 16-bit 1:24-bit 2:32-bit. [9] REG_EXT_I2S_BCK_GEN_DIV2. [8:7] REG_EXT_I2S_BCK_GEN_SEL. 0: 8K 1:16K 2:32K 3:48K. [6] REG_EXT_I2S_BCK_GEN_UPDATE. [5] REG_EXT_I2S_TRX_BCK_INV. [4] REG_EXT_RX_FIFO_STATUS_CLR. [3] REG_EXT_RX_FIFO_EXTENSION. [2] REG_EXT_FS_SEL. [1] REG_EXT_I2S_LOOPBACK_EN.	
112B2Ah	**REG112B2A**	**15:0**	**Default : 0x00C0**	**Access : R/W**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	PAD_CTRL0[15:0]	15:0	0x2A. [15:14] REG_PAD_EXT_I2S_RX_SEL. 0: EXT 1:CODEC 2:BT 3:EXT. [13:12] REG_PAD_CODEC_I2S_TX_S_SEL. 0: CODEC 1:CODEC 2:BT 3:EXT. [11:10] REG_PAD_CODEC_I2S_TX_M_SEL. 0: CODEC 1:CODEC 2:BT 3:DBB. [9:8] REG_PAD_BT_I2S_TRX_S_SEL. 0: BT 1:CODEC 2:BT 3:EXT. [7:6] REG_PAD_BT_I2S_TRX_M_SEL. 0: BT 1:CODEC 2:BT 3:DBB. [5:4] REG_PAD_DBB_I2S_TRX_S_SEL. 0: BT 1:CODEC 2:BT 3:EXT. [3:1] REG_PAD_SPDIF_IN_SEL. 0: PAD_SPDIF_TX_SDI. 1: PAD_EXT_I2S_RX_SDI_S. 2: PAD_BT_I2S_TRX_SDI_S. 3: PAD_BT_I2S_TRX_SDO_S. 4: PAD_CODEC_I2S_TRX_SDI_S. 5: PAD_CODEC_I2S_TRX_SDO_S. 6: PAD_SPDIF_TX_SDO.	
112B2Ch	**REG112B2C**	**15:0**	**Default : 0x0E00**	**Access : R/W**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	PAD_CTRL1[15:0]	15:0	0x2C. [15] REG_CODEC_I2S_TRX_WCK_OEN. [14] REG_CODEC_I2S_TRX_BCK_OEN. [13] REG_CODEC_I2S_TRX_SDI_OEN. [12] REG_CODEC_I2S_TRX_SDO_OEN. [11] REG_EXT_I2S_RX_WCK_OEN. [10] REG_EXT_I2S_RX_BCK_OEN. [9] REG_EXT_I2S_RX_SDI_OEN. [8] REG_DMA2_RD_VALID_SEL. 1: ASRC2_CH1_DAC_FS 0:ASRC2_CH2_DAC_FS. [7] REG_DMA2_WR_VALID_SEL. 1: ASRC2_CH1_DEC_FS 0:CH1_DEC_FS. [6:5] REG_DMA2_WR_MUX_SEL. 0: DEC1/DEC2. 1: Parser. 2: AMR_REC. 3: ASRC2. [4] REG_CH1_MUX_SEL2. 1: SPDIF RX 0:External I2S RX. [3] REG_SPDIF_TX_SOURCE_SEL. 1: DEC3 0:ASRC2 DEC3. [2] REG_SPDIF_TX_SDO_OEN. [1] REG_SPDIF_RX_FS_SEL. 1: ASRC2_CH1_DEC_FS 0:CH1_DEC_FS.	
112B2Eh	**REG112B2E**	**15:0**	**Default : 0x0000**	**Access : RO**
	AUDIOBAND_STS2[15:0]	15:0	0x2E. [15:14] REG_DBB_I2S_IN_WDTH. [13:12] REG_DBB_I2S_OUT_WDTH. [11] REG_DBB_RX_FIFO_STATUS. [10] REG_DBB_TX_FIFO_STATUS. [9:8] REG_CODEC_I2S_IN_WDTH. [7:6] REG_CODEC_I2S_OUT_WDTH. [5] REG_CODEC_TX_FIFO_STATUS. [4] REG_EXT_RX_FIFO_STATUS. [3]REG_PNT_MMC_DEC_ERR. [2]REG_PNT_ASRC2_MMC_DEC_ERR.	
112B30h	**REG112B30**	**15:0**	**Default : 0x0200**	**Access : R/W**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	DIG_MIC_CTRL1[15:0]	15:0	0x30. [15] REG_DIG_MIC_EN. [14] REG_DIG_MIC_BCK_INV. [13] REG_DIG_MIC_BCK_SEL. [12] REG_PAD_CODEC_I2S_TX_SDI_M_SEL. [11] REG_PAD_BT_I2S_TRX_SDI_M_SEL. [10] REG_PAD_DIG_MIC_BCK_OEN. [9:8] REG_PAD_DIG_MIC_SDI_OEN. [5] REG_PNT_MMC_DEC_ERR_CLR. [4] REG_PNT_ASRC2_MMC_DEC_ERR_CLR. [3] REG_PNT_MMC1_DEC_SYNC_ENZ. [2] REG_PNT_MMC3_DEC_SYNC_ENZ. [1] REG_PNT_MMC2_DEC_SYNC_ENZ. [0] REG_PNT_MMC4_DEC_SYNC_ENZ.	
112B32h	**REG112B32**	**15:0**	**Default : 0x0303**	**Access : R/W**
	DIG_MIC_CTRL2[15:0]	15:0	0x32. [15] REG_DIG_MIC_SEL1. [13] REG_DIG_MIC_CH1_SDI_SEL. [12:8] REG_DIG_MIC_CH1_PHASE. [7] REG_DIG_MIC_SEL2. [5] REG_DIG_MIC_CH2_SDI_SEL. [4:0] REG_DIG_MIC_CH2_PHASE.	
112B34h	**REG112B34**	**15:0**	**Default : 0x0303**	**Access : R/W**
	DIG_MIC_CTRL3[15:0]	15:0	0x34. [15] REG_DIG_MIC_SEL3. [13] REG_DIG_MIC_CH3_SDI_SEL. [12:8] REG_DIG_MIC_CH3_PHASE. [7] REG_DIG_MIC_SEL4. [5] REG_DIG_MIC_CH4_SDI_SEL. [4:0] REG_DIG_MIC_CH4_PHASE.	
112B40h	**REG112B40**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA2_WR_DATA_L[15:0]	15:0	0x40.	
112B42h	**REG112B42**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA2_WR_DATA_R[15:0]	15:0	0x42.	
112B44h	**REG112B44**	**15:0**	**Default : 0x0000**	**Access : RO**
	DEC3_DOUT[15:0]	15:0	0x44.	
112B46h	**REG112B46**	**15:0**	**Default : 0x0000**	**Access : RO**
	DEC4_DOUT[15:0]	15:0	0x46.	

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
112B48h	**REG112B48**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_DEC3_OUT[15:0]	15:0	0x48.	
112B4Ah	**REG112B4A**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_DEC4_OUT[15:0]	15:0	0x4A.	
112B4Ch	**REG112B4C**	**15:0**	**Default : 0x0000**	**Access : RO**
	SDM_CH3_IN[15:0]	15:0	0x4C.	
112B4Eh	**REG112B4E**	**15:0**	**Default : 0x0000**	**Access : RO**
	SDM_CH4_IN[15:0]	15:0	0x4E.	
112B60h	**REG112B60**	**15:0**	**Default : 0x0000**	**Access : R/W**
	PARSER_CTRL0[15:0]	15:0	0x60. [0] reg_parser_dis. [1] reg_pkt_len_en. [2] reg_flush. [3] Reserve. [4] reg_parser_rst. [5] reg_clr_pts_int. [6] reg_clr_es_counter. [7] reg_parser_stop. [8] reg_pts_err_rtn. [9] reg_dsp2pas_check_ack. [10] dsp2pas_mpeg1. [11] dsp2pas_chk_id_match_on. [14:12] reserve. [15]ES2 buffer full, then de-ack to parser.	
112B62h	**REG112B62**	**15:0**	**Default : 0x0000**	**Access : R/W**
	PARSER_CTRL1[15:0]	15:0	0x62. [15:8] ID1_MASK:Don't care this bits when match stream id. [7:0] Stream ID1 to filter PES header.	
112B64h	**REG112B64**	**15:0**	**Default : 0x0000**	**Access : R/W**
	PARSER_CTRL2[15:0]	15:0	0x64. [15:8] ID2_MASK:Don't care this bits when match stream id. [7:0] Stream ID2 to filter PES header.	
112B66h	**REG112B66**	**15:0**	**Default : 0x0000**	**Access : R/W**
	PARSER_CTRL3[15:0]	15:0	0x66. [0]Parser filter extra header enable. [6:1]Parser filter extra header byte size. [11:7]To indirect read PD data.	
112B68h	**REG112B68**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	PARSER_CTRL4[15:0]	15:0	0x68. [7:0]Define parser extract header offset.	
112B6Ah	**REG112B6A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	PARSER_CTRL5[15:0]	15:0	0x6A. Reserved.	
112B80h	**REG112B80**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS0[15:0]	15:0	0x80.	
112B82h	**REG112B82**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS1[15:0]	15:0	0x82.	
112B84h	**REG112B84**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS2[15:0]	15:0	0x84.	
112B86h	**REG112B86**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS3[15:0]	15:0	0x86.	
112B88h	**REG112B88**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS4[15:0]	15:0	0x88.	
112B8Ah	**REG112B8A**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS5[15:0]	15:0	0x8A.	
112B8Ch	**REG112B8C**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS6[15:0]	15:0	0x8C.	
112B8Eh	**REG112B8E**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS7[15:0]	15:0	0x8E.	
112B90h	**REG112B90**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS8[15:0]	15:0	0x90.	
112B92h	**REG112B92**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS9[15:0]	15:0	0x92.	
112B94h	**REG112B94**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS10[15:0]	15:0	0x94.	
112B96h	**REG112B96**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS11[15:0]	15:0	0x96.	
112B98h	**REG112B98**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS12[15:0]	15:0	0x98.	
112B9Ah	**REG112B9A**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS13[15:0]	15:0	0x9A.	
112B9Ch	**REG112B9C**	**15:0**	**Default : 0x0000**	**Access : RO**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	PARSER_STATUS14[15:0]	15:0	0x9C.	
112B9Eh	**REG112B9E**	**15:0**	**Default : 0x0000**	**Access : RO**
	PARSER_STATUS15[15:0]	15:0	0x9E.	
112BA0h	**REG112BA0**	**15:0**	**Default : 0x0000**	**Access : RO**
	DEC1_DOUT_AB[15:0]	15:0	0xA0.	
112BA2h	**REG112BA2**	**15:0**	**Default : 0x0000**	**Access : RO**
	DEC1_DOUT_IIR[15:0]	15:0	0xA2.	
112BA4h	**REG112BA4**	**15:0**	**Default : 0x0000**	**Access : RO**
	DEC1_DOUT[15:0]	15:0	0xA4.	
112BA6h	**REG112BA6**	**15:0**	**Default : 0x0000**	**Access : RO**
	DEC2_DOUT[15:0]	15:0	0xA6.	
112BA8h	**REG112BA8**	**15:0**	**Default : 0x0000**	**Access : RO**
	INT1_DOUT[15:0]	15:0	0xA8.	
112BAAh	**REG112BAA**	**15:0**	**Default : 0x0000**	**Access : RO**
	INT2_DOUT[15:0]	15:0	0xAA.	
112BACh	**REG112BAC**	**15:0**	**Default : 0x0000**	**Access : RO**
	IIR1_DOUT[15:0]	15:0	0xAC.	
112BAEh	**REG112BAE**	**15:0**	**Default : 0x0000**	**Access : RO**
	IIR2_DOUT[15:0]	15:0	0xAE.	
112BB0h	**REG112BB0**	**15:0**	**Default : 0x0000**	**Access : RO**
	FM_RX_L_DIN[15:0]	15:0	0xB0.	
112BB2h	**REG112BB2**	**15:0**	**Default : 0x0000**	**Access : RO**
	FM_RX_R_DIN[15:0]	15:0	0xB2.	
112BB4h	**REG112BB4**	**15:0**	**Default : 0x0000**	**Access : RO**
	BT_DL_L_DOUT[15:0]	15:0	0xB4.	
112BB6h	**REG112BB6**	**15:0**	**Default : 0x0000**	**Access : RO**
	BT_DL_R_DOUT[15:0]	15:0	0XB6.	
112BB8h	**REG112BB8**	**15:0**	**Default : 0x0000**	**Access : RO**
	BT_UL_MONO_DOUT[15:0]	15:0	0xB8.	
112BBAh	**REG112BBA**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMARD_L_DOUT[15:0]	15:0	0xBA.	
112BBCh	**REG112BBC**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMARD_R_DOUT[15:0]	15:0	0xBC.	
112BBEh	**REG112BBE**	**15:0**	**Default : 0x0000**	**Access : RO**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	DMAWR_L_DOUT[15:0]	15:0	0xBE.	
112BC0h	**REG112BC0**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMAWR_R_DOUT[15:0]	15:0	0xC0.	
112BC2h	**REG112BC2**	**15:0**	**Default : 0x0000**	**Access : RO**
	DBB_DL_MONO_DIN[15:0]	15:0	0xC2.	
112BC4h	**REG112BC4**	**15:0**	**Default : 0x0000**	**Access : RO**
	TEST_PCM_OUT_CH1[15:0]	15:0	0xC4.	
112BC6h	**REG112BC6**	**15:0**	**Default : 0x0000**	**Access : RO**
	TEST_PCM_OUT_CH2[15:0]	15:0	0xC6.	
112BC8h	**REG112BC8**	**15:0**	**Default : 0x0000**	**Access : RO**
	VALDI_SIGNALS[15:0]	15:0	0xC8.	
112BCAh	**REG112BCA**	**15:0**	**Default : 0x0000**	**Access : RO**
	INT_SIGNALS[15:0]	15:0	0xCA.	
112BCCh	**REG112BCC**	**15:0**	**Default : 0x0000**	**Access : RO**
	CLK_SIGNALS[15:0]	15:0	0xCC.	
112BCEh	**-**	**15:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
112BD0h	**REG112BD0**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_MMP1_IN[15:0]	15:0	0xD0.	
112BD2h	**REG112BD2**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_MMP2_IN[15:0]	15:0	0xD2.	
112BD4h	**REG112BD4**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_INT1_IN[15:0]	15:0	0xD4.	
112BD6h	**REG112BD6**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_INT2_IN[15:0]	15:0	0xD6.	
112BD8h	**REG112BD8**	**15:0**	**Default : 0x0000**	**Access : RO**
	CH3_CIC_ABS_OUT[15:0]	15:0	0xD8.	
112BDAh	**REG112BDA**	**15:0**	**Default : 0x0000**	**Access : RO**
	CH4_CIC_ABS_OUT[15:0]	15:0	0xDA.	
112BDCh	**REG112BDC**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_DEC1_OUT[15:0]	15:0	0xDC.	
112BDEh	**REG112BDE**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_DEC2_OUT[15:0]	15:0	0xDE.	
112BE0h	**REG112BE0**	**15:0**	**Default : 0x0000**	**Access : RO**

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BACH1 Register (Bank = 112B)				
Index	**Mnemonic**	**Bit**	**Description**	
	ASRC2_INT1_OUT[15:0]	15:0	0xE0.	
112BE2h	**REG112BE2**	**15:0**	**Default : 0x0000**	**Access : RO**
	ASRC2_INT2_OUT[15:0]	15:0	0xE2.	
112BE4h	**REG112BE4**	**15:0**	**Default : 0x0000**	**Access : RO**
	SDM_CH1_IN[15:0]	15:0	0xE4.	
112BE6h	**REG112BE6**	**15:0**	**Default : 0x0000**	**Access : RO**
	SDM_CH2_IN[15:0]	15:0	0xE6.	

BACH2 Register (Bank = 112C)

BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
112C00h	**REG112C00**	**15:0**	**Default : 0x0040**	**Access : R/W**
	ANALOG_CTRL00[15:0]	15:0	0x00. [15] REG_MCPLS_EN. [14] INT_AU_DET_TEST_MODE. [13] INT_AU_DET_TEST_VALUE. [12] REG_RSTZ_AU_DET. [6:4] REG_MCPLS_PRD. [3:2] REG_MCPLS_SEL. [1:0] REG_DBNC_TIME.	
112C02h	**REG112C02**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL01[15:0]	15:0	0x02. [15] INT_CLR_HS_GND = RIU_ANALOG_CTRL01. [14] INT_CLR_HS_UNPLUG = RIU_ANALOG_CTRL01. [13] INT_CLR_HS_PLUGIN = RIU_ANALOG_CTRL01. [12] INT_CLR_SPK_UNPLUG = RIU_ANALOG_CTRL01. [11] INT_CLR_SPK_PLUGIN = RIU_ANALOG_CTRL01. [10] INT_CLR_MICLP_UNPLUG = RIU_ANALOG_CTRL01. [9] INT_CLR_MICLP_PLUGIN = RIU_ANALOG_CTRL01. [7] INT_MASK_HS_GND = RIU_ANALOG_CTRL01. [6] INT_MASK_HS_UNPLUG = RIU_ANALOG_CTRL01. [5] INT_MASK_HS_PLUGIN = RIU_ANALOG_CTRL01. [4] INT_MASK_SPK_UNPLUG = RIU_ANALOG_CTRL01. [3] INT_MASK_SPK_PLUGIN = RIU_ANALOG_CTRL01. [2] INT_MASK_MICLP_UNPLUG = RIU_ANALOG_CTRL01. [1] INT_MASK_MICLP_PLUGIN = RIU_ANALOG_CTRL01.	
112C04h	**REG112C04**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL02[15:0]	15:0	0x04. Reserved.	
112C06h	**REG112C06**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL03[15:0]	15:0	0x06. [15] EN_CLK_TST enable clk test block. [14] EN_AUDIO_IBIAS enable auido ibias_atop. [13:12] IBSEL_AUDIO select audio atop bias current, 00:5u,01:2.5u,10:10u,11:7.5u. [11] EN_POLLING_DRV enable charge VREF14_DRV. [10] EN_REF_NO_BG enable audio atop refsys. [9] REG_SEL_CONTROL "select control registor: 0 trim_ok control the ldo input ; 1 reg_control control the ldo.". [8] REG_CONTROL "select ldo input voltage: 0 from VABB divider;1 from micbias". [7] EN_MICDET Enable micphone detection. [6] HST_EN Enable Headset micbias output. [5] RCV_EN Enable handset micbias output. [4:3] MICV_SEL "mic bias level option. 00: 2.1V (default); 01: 2V; 10: 1.9V; 11: 2.3V". [2] EN_MICBIAS Enable micbias. [1:0] SEL_IREFDET reference current option for detect plug-in resistor, 00:10u,01:5u,10:20u,11:15u.	
112C08h	**REG112C08**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL04[15:0]	15:0	0x08. [15:14] SEL_IREFGND reference current option for detect plug-to-gnd resistor, 00:10u,01:5u,10:20u,11:15u. [13] EN_MICTRIM Enable micbias trimming cmparator. [12] EN_MICDET_LP Enable Low power MICDET. [11] PULLUP_HSIP Pull up HSIP to MICDET_IN, 0:Hi-z, 1: pullup. [10] SEL_VCMREF0 "select vcmbuf input volatge for PGA0: 0: From micbias; 1:from VABB divider". [9] EN_VCMBUF0 Enable PGA0 vcmbuf. [8] EN_IBIAS_PGA0 Enable PGA0 Ibias. [7:6] IBIAS_PGA0 Adjust the bias current of PGA0, 00:10u,01:5u,10:20u,11:15u. [5] EN_PGA0_MICA1 Enable PGA0 micamp1. [4] PGA0_MICA1_GAIN PGA0 micamp1 gain, 0:13dB, 1:23dB. [3] EN_PGA0_MICA2 Enable PGA0 micamp2. [2:0] PGA0_MICA2_GAIN "PGA0 micamp2 gain, 0: 000: 0dB 001:3dB 010:6dB 011:9dB. 100: 12dB 101:15dB 110:-3dB 111: -6dB".	
112C0Ah	**REG112C0A**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL05[15:0]	15:0	0x0A. [15] PGA0_MICA2_SEL "PGA0 micamp2 input select: 0: From micphone; 1: from Line-in". [14] PGA0_MUTE_L Mute PGA0 L-channel. [13] EN_PGA0_MICA3 Enable PGA0 micamp3. [12] PGA0_MICA3_GAIN PGA0 micamp3 gain, 0:13dB, 1:23dB. [11] EN_PGA0_MICA4 Enable PGA0 micamp4. [10:8] PGA0_MICA4_GAIN "PGA0 micamp4 gain, 0: 000: 0dB 001:3dB 010:6dB 011:9dB. 100: 12dB 101:15dB 110:-3dB 111: -6dB". [7] PGA0_MICA4_SEL "PGA0 micamp4 input select: 0: From micphone; 1: from Line-in". [6] PGA0_MUTE_R Mute PGA0 R-channel. [5] PGA0_LINE_SEL "PGA0 LINE-IN select: 0: From Line0_L &&Line0_R; 1: From Line1_L&&Line1_R;". [4] SEL_VCMREF1 "select vcmbuf input volatge for PGA1: 0: From micbias; 1:from VABB divider". [3] EN_VCMBUF1 Enable PGA1 vcmbuf. [2] EN_IBIAS_PGA1 Enable PGA1 Ibias. [1:0] IBIAS_PGA1 Adjust the bias current of PGA1, 00:10u,01:5u,10:20u,11:15u.	
112C0Ch	**REG112C0C**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL06[15:0]	15:0	0x0C. [15] EN_PGA1_MICA2 Enable PGA1 micamp2. [14:12] PGA1_MICA2_GAIN "PGA1 micamp2 gain, 0: 000: 0dB 001:3dB 010:6dB 011:9dB. 100: 12dB 101:15dB 110:-3dB 111: -6dB". [11] PGA1_MUTE_L Mute PGA1 L-channel. [10] EN_PGA1_MICA4 Enable PGA1 micamp4. [9:7] PGA1_MICA4_GAIN "PGA1 micamp4 gain, 0: 000: 0dB 001:3dB 010:6dB 011:9dB. 100: 12dB 101:15dB 110:-3dB 111: -6dB". [6] PGA1_MUTE_R Mute PGA1 R-channel. [5] PGA1_LINE_SEL "PGA1 LINE-IN select: 0: From Line1_L &&Line1_R; 1: From Line0_L&&Line0_R;". [4] POS_RL0 "Audio DAC0 data latching mode select. 0: Negtive edge select. 1: Positive edge select". [3] LDO11_VC0 1.1V LDO (in DAC0)voltage select 0:1.2V, 1:1.3V. [2] EN_DAC0_LDO11 enable 1.1V LDO(in DAC0). [1] EN_DAC0_L enable L-channel DAC0. [0] EN_DAC0_R enable R-channel DAC0.	
112C0Eh	**REG112C0E**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL07[15:0]	15:0	0x0E. [15] POS_RL1 "Audio DAC1 data latching mode select. 0: Negtive edge select. 1: Positive edge select". [14] LDO11_VC1 1.1V LDO (in DAC1)voltage select 0:1.2V, 1:1.3V. [13] EN_DAC1_LDO11 enable 1.1V LDO(in DAC1). [12] EN_DAC1_L enable L-channel DAC1. [11] EN_DAC1_R enable R-channel DAC1. [10] EN_ADC0_DIT enable ADC0 dither. [9:8] SEL_DIT_LVL_ADC0 "selecte ADC0 dither level: 00=1/3Vref, 01=1/6Vref. 10=1/2Vref, 11=2/3Vref". [7:6] SEL_IBIAS_ADC0 "select ADC0 bias current: 00: 5uA, 01:7.5uA, 10:10uA, 11:2.5uA". [5] RESET_ADC0_R (Rchannel) Reset ADC0 input, 0:normal, 1:short input. [4] RESET_ADC0_L (Lchannel) Reset ADC0 input, 0:normal, 1:short input. [3] SHRT_ADC0_R (Rchannel) Short ADC0 input, 0:normal, 1:short input. [2] SHRT_ADC0_L (Lchannel) Short ADC0 input, 0:normal, 1:short input. [1] EN_ADC0 enable ADC0. [0] EN_ADC1_DIT enable ADC1 dither.	
112C10h	**REG112C10**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL08[15:0]	15:0	0x10. [15:14] SEL_DIT_LVL_ADC1 "selecte ADC1 dither level: 00=1/3Vref, 01=1/6Vref. 10=1/2Vref, 11=2/3Vref". [13:12] SEL_IBIAS_ADC1 "select ADC1 bias current: 00: 5uA, 01:7.5uA, 10:10uA, 11:2.5uA". [11] RESET_ADC1_R (Rchannel) Reset ADC1 input, 0:normal, 1:short input. [10] RESET_ADC1_L (Lchannel) Reset ADC1 input, 0:normal, 1:short input. [9] SHRT_ADC1_R (Rchannel) Short ADC1 input, 0:normal, 1:short input. [8] SHRT_ADC1_L (Lchannel) Short ADC1 input, 0:normal, 1:short input. [7] EN_ADC1 enable ADC1. [6] EN_EARR Enable R channel earphone. [5] EN_EARL Enable L channel earphone. [4] EN_OPLP Enable OPLP amp. [3] EN_STG2AB Earphone driver class AB drive stage stage. [2:1] GAIN_EAR "Earphone gain control: 00: Gain=0.6; 01: Gain=0.4; 10: Gain=1; 11: Gain=1.2; ".	
112C12h	**REG112C12**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL09[15:0]	15:0	0x12. [15:14] TCSEL Control the oplp output current to control the Vcm set up time when audio power on. [13:12] EAR_POPRES "Earphone depop res control: X0: AC mode(r=500); X1: DC mode.". [11] EAR_MUTE Mute earphone driver. [10:7] TST_DRV Select test current. [6:5] ISEL_DRV Change driver bias current. [4:3] ISEL_OCP Select OCP current. [2:0] MX_EAR "Earphone MUX control: 000: DAC0 output; 001: DAC0 output(inv channel); 010: DAC1 output; 011: DAC1 output(inv channel); 100: PGA0 output; 101: VCM14;".	

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
112C14h	**REG112C14**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL10[15:0]	15:0	0x14. [15] EN_LINE0_L Enable L-channel LINE-out PGA0. [14] EN_LINE0_R Enable R-channel LINE-out PGA0. [13:11] GAIN_LINE0 "LINE-out PGA0 gain control: 000: 0dB; 001:3dB;010:6dB;011:9dB;100:12dB". [10:9] MX_LINE0 "LINE-out PGA0 input select: 00: From DAC0; 01: From DAC0(inv channel); 10: From PGA0; 11: From VMID". [8] MUTE_LINE0 Mute LINE-out PGA0. [7] EN_LINE1_L Enable L-channel LINE-out PGA1. [6] EN_LINE1_R Enable R-channel LINE-out PGA1. [5:3] GAIN_LINE1 "LINE-out PGA1 gain control: 000: 0dB; 001:3dB;010:6dB;011:9dB;100:12dB". [2:1] MX_LINE1 "LINE-out PGA1 input select: 00: From DAC0; 01: From DAC0(inv channel); 10: From PGA0; 11: From VMID". [0] MUTE_LINE1 Mute LINE-out PGA1.	
112C16h	**REG112C16**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
	ANALOG_CTRL11[15:0]	15:0	0x16. [15] EN_LDO25 Enable 2.5V LDO. [14:13] V_SET_LDO25 "Select LDO output voltage: 00: 2.5V 01:2.35V 10:2.65V 11:2.8V". [12] EN_CLK Enable 48MHz CLK input. [11] DAC_CLK_FREQ select DAC frequency. 0: 24MHz(defualt), 1:12MHz. [10] ADC_CLK_FREQ select ADC frequency. 0: 48MHz(defualt), 1:24MHz. [9] SEL_PHS_ADCCLK select ADC clk phase, 0: inv clk 1:not inv. [8:7] SEL_CK_AUDIO "select audio clk sourece: 00: 48M form MPLL; 01: 48M from USB; 10: 368M from AUPLL; 11: From digital clk". [6:3] TST_AUDIO "select test current/voltage output. 0000: Hi-Z, 0001: currentgen cur, 0010: micamp cur, 0011:PGA0 cur, 0100: PGA1 cur, 0101: ADC0 cur, 0110: ADC1 cur, 0111: LDO25 vol, 1000:DAC0 cur, 1001:DAC1 cur, 1010:DRV cur, 1011:nothing, 1100: VREF11_LDO11, 1101:LDO11, 1110-1111:nothing".	
112C18h	**REG112C18**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL12[15:0]	15:0	0x18. [7:0] AUDIO_REG reseved register.	
112C1Ah	**REG112C1A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL13[15:0]	15:0	0x1A.	
112C1Ch	**REG112C1C**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL14[15:0]	15:0	0x1C.	
112C1Eh	**REG112C1E**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL15[15:0]	15:0	0x1E.	
112C20h	**REG112C20**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL16[15:0]	15:0	0x20.	
112C22h	**REG112C22**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL17[15:0]	15:0	0x22.	

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BACH2 Register (Bank = 112C)				
Index	**Mnemonic**	**Bit**	**Description**	
112C24h	**REG112C24**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL18[15:0]	15:0	0x24.	
112C26h	**REG112C26**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL19[15:0]	15:0	0x26.	

BACH3 Register (Bank = 112D)

BACH3 Register (Bank = 112D)				
Index	**Mnemonic**	**Bit**	**Description**	
112D40h	**REG112D40**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	MMP1_DPGA_CFG1[10:0]	10:0	0x40 MMP1_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D42h	**REG112D42**	**15:0**	**Default : 0x007F**	**Access : R/W**

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BACH3 Register (Bank = 112D)				
Index	**Mnemonic**	**Bit**	**Description**	
	-	15:9	Reserved.	
	MMP1_DPGA_CFG2[8:0]	8:0	0x42 MMP1_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D44h	**REG112D44**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	MMP2_DPGA_CFG1[10:0]	10:0	0x44 MMP2_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D46h	**REG112D46**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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BACH3 Register (Bank = 112D)				
Index	**Mnemonic**	**Bit**	**Description**	
	MMP2_DPGA_CFG2[8:0]	8:0	0x46 MMP2_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D48h	**REG112D48**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DEC1_1_DPGA_CFG1[10:0]	10:0	0x48 DEC1_1_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D4Ah	**REG112D4A**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DEC1_1_DPGA_CFG2[8:0]	8:0	0x4A DEC1_1_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D4Ch	**REG112D4C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DEC1_2_DPGA_CFG1[10:0]	10:0	0x4C DEC1_2_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D4Eh	**REG112D4E**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DEC1_2_DPGA_CFG2[8:0]	8:0	0x4E DEC1_2_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D50h	**REG112D50**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DEC1_3_DPGA_CFG1[10:0]	10:0	0x50 DEC1_3_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D52h	**REG112D52**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DEC1_3_DPGA_CFG2[8:0]	8:0	0x52 DEC1_3_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D54h	**REG112D54**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DBB_1_DPGA_CFG1[10:0]	10:0	0x54 DBB_1_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D56h	**REG112D56**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DBB_1_DPGA_CFG2[8:0]	8:0	0x56 DBB_1_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D58h	**REG112D58**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DBB_2_DPGA_CFG1[10:0]	10:0	0x58 DBB_2_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D5Ah	**REG112D5A**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DBB_2_DPGA_CFG2[8:0]	8:0	0x5A DBB_2_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D5Ch	**REG112D5C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DMARD_L_DPGA_CFG1[10:0]	10:0	0x5C DMARD_L_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D5Eh	**REG112D5E**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DMARD_L_DPGA_CFG2[8:0]	8:0	0x5E DMARD_L_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D60h	**REG112D60**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DMARD_R_DPGA_CFG1[10:0]	10:0	0x60 DMARD_R_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D62h	**REG112D62**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DMARD_R_DPGA_CFG2[8:0]	8:0	0x62 DMARD_R_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D64h	**REG112D64**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	ASRC2_MMP1_DPGA_CFG1[10:0]	10:0	0x64 ASRC2_MMP1_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D66h	**REG112D66**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	ASRC2_MMP1_DPGA_CFG2[8:0]	8:0	0x66 ASRC2_MMP1_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D68h	**REG112D68**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	ASRC2_MMP2_DPGA_CFG1[10:0]	10:0	0x68 ASRC2_MMP2_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D6Ah	**REG112D6A**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	ASRC2_MMP2_DPGA_CFG2[8:0]	8:0	0x6A ASRC2_MMP2_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D6Ch	**REG112D6C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	CODEC1_DPGA_CFG1[10:0]	10:0	0x6C CODEC1_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D6Eh	**REG112D6E**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	CODEC1_DPGA_CFG2[8:0]	8:0	0x6E CODEC1_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D70h	**REG112D70**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	CODEC2_DPGA_CFG1[10:0]	10:0	0x70 CODEC2_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D72h	**REG112D72**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	CODEC2_DPGA_CFG2[8:0]	8:0	0x72 CODEC2_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D74h	**REG112D74**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	SPDIF1_DPGA_CFG1[10:0]	10:0	0x74 SPDIF1_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D76h	**REG112D76**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	SPDIF1_DPGA_CFG2[8:0]	8:0	0x76 SPDIF1_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D78h	**REG112D78**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	SPDIF2_DPGA_CFG1[10:0]	10:0	0x78 SPDIF2_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D7Ah	**REG112D7A**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	SPDIF2_DPGA_CFG2[8:0]	8:0	0x7A SPDIF2_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D7Ch	**REG112D7C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DMAWR1_DPGA_CFG1[10:0]	10:0	0x7C DMAWR1_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D7Eh	**REG112D7E**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DMAWR1_DPGA_CFG2[8:0]	8:0	0x7E DMAWR1_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D80h	**REG112D80**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DMAWR2_DPGA_CFG1[10:0]	10:0	0x80 DMAWR2_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D82h	**REG112D82**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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	DMAWR2_DPGA_CFG2[8:0]	8:0	0x82 DMAWR2_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D84h	**REG112D84**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DMAWR3_DPGA_CFG1[10:0]	10:0	0x84 DMAWR3_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D86h	**REG112D86**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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	DMAWR3_DPGA_CFG2[8:0]	8:0	0x86 DMAWR3_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D88h	**REG112D88**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	DMAWR4_DPGA_CFG1[10:0]	10:0	0x88 DMAWR4_DPGA_CFG1. [15:11] Reserved. [10:6] REG_OFFSET. Gain Offset for the DPGA. Gain Offset = (signed)DPGA_GAIN_OFFSET * (-0.5dB). [5:3] STEP. Step Size for the fading function in the right channel. 000 = 1 samples. 001 = 2 samples. 010 = 4 samples. 011 = 8 samples. 100 = 16 samples. 101 = 32 samples. 110 = 64 samples. 111 = reserved. [2] MUTE_2_ZERO. DPGA mute to zero. 0 = disable. 1 = enable. [1] FADING_EN. Fading enable. 0 = disable. 1 = enable. [0] DPGA_EN. DPGA Enable. 0 = disable. 1 = enable.	
112D8Ah	**REG112D8A**	**15:0**	**Default : 0x007F**	**Access : R/W**
	-	15:9	Reserved.	

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Index	**Mnemonic**	**Bit**	**Description**	
	DMAWR4_DPGA_CFG2[8:0]	8:0	0x8A DMAWR4_DPGA_CFG2. [15:9] Reserved. [8] REG_GAIN_TRIG. Gain trigger. [7:0] REG_GAIN. Gain for the DPGA. Gain = (signed) DPGA_GAIN * (-0.5dB).	
112D8Ch	**REG112D8C**	**15:0**	**Default : 0x0F0F**	**Access : R/W**

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BACH3 Register (Bank = 112D)			
Index	**Mnemonic**	**Bit**	**Description**
	PGA1_DPGA_CFG1[15:0]	15:0	0x8C PGA1_DPGA_CFG1. Pga1_dpga_cfg. [15]REG_EN. DPGA Enable. 0 = disable. 1 = enable. [14]REG_MUTE. DPGA mute. 0 = disable. 1 = enable. [13]REG_GAIN_TRIG. DPGA gain trigger. 0 = hold. 1 = trigger. [12:8]REG_GAIN. Gain = (signed)DPGA_GAIN * (-3dB). Pga2_dpga_cfg. [7]REG_EN. DPGA Enable. 0 = disable. 1 = enable. [6]REG_MUTE. DPGA mute. 0 = disable. 1 = enable. [5]REG_GAIN_TRIG. DPGA gain trigger. 0 = hold. 1 = trigger. [4:0]REG_GAIN. Gain = (signed)DPGA_GAIN * (-3dB). [7]REG_EN. DPGA Enable. 0 = disable. 1 = enable. [6]REG_MUTE. DPGA mute. 0 = disable. 1 = enable. [5]REG_GAIN_TRIG. DPGA gain trigger. 0 = hold. 1 = trigger. [4:0]REG_GAIN. Gain = (signed)DPGA_GAIN * (-3dB).

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BACH3 Register (Bank = 112D)				
Index	**Mnemonic**	**Bit**	**Description**	
112D8Eh	**REG112D8E**	**15:0**	**Default : 0x0F0F**	**Access : R/W**
	PGA2_DPGA_CFG1[15:0]	15:0	0x8E PGA2_DPGA_CFG1. Pga3_dpga_cfg. [15]REG_EN. DPGA Enable. 0 = disable. 1 = enable. [14]REG_MUTE. DPGA mute. 0 = disable. 1 = enable. [13]REG_GAIN_TRIG. DPGA gain trigger. 0 = hold. 1 = trigger. [12:8]REG_GAIN. Gain = (signed)DPGA_GAIN * (-3dB). Pga4_dpga_cfg. [7]REG_EN. DPGA Enable. 0 = disable. 1 = enable. [6]REG_MUTE. DPGA mute. 0 = disable. 1 = enable. [5]REG_GAIN_TRIG. DPGA gain trigger. 0 = hold. 1 = trigger. [4:0]REG_GAIN.	
112D90h	**REG112D90**	**15:0**	**Default : 0x0000**	**Access : R/W**

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BACH3 Register (Bank = 112D)				
Index	**Mnemonic**	**Bit**	**Description**	
	DPGA_MUTE_CFG[15:0]	15:0	0x90 DPGA_MUTE_CFG. [15]DPGA mute done interrupt mask. 0 = mask. 1 = normal. [14]DPGA status clear. 0 = normal. 1 = clear. [13]PGA status clear. 0 = normal. 1 = clear. [12:10]Reserved. [9:0] DPGA mute done bypass. 0 = normal. 1 = bypass. [9]MMP1_MUTE_DONE. [8]MMP2_MUTE_DONE. [7]DEC1_1_MUTE_DONE. [6]DEC1_2_MUTE_DONE. [5]DEC1_3_MUTE_DONE. [4]DBB_1_MUTE_DONE. [3]DBB_2_MUTE_DONE. [2]DMARD_L_MUTE_DONE. [1]DMARD_R_MUTE_DONE. [0]SPARE_MUTE_DONE.	
112D92h	**REG112D92**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DPGA_MUTE_CFG2[15:0]	15:0	0x92 DPGA_MUTE_CFG2.	
112D94h	**REG112D94**	**15:0**	**Default : 0x0000**	**Access : RO**
	DPGA_MUTE_STS[15:0]	15:0	0x94 DPGA_MUTE_STS. [15:11]Reserved. [10]ASRC2_MMP1_MUTE_DONE. [9]ASRC2_MMP2_MUTE_DONE. [8]DMARD_R_MUTE_DONE. [7]DMARD_L_MUTE_DONE. [6]DBB_2_MUTE_DONE. [5]DBB_1_MUTE_DONE. [4]DEC1_3_MUTE_DONE. [3]DEC1_2_MUTE_DONE. [2]DEC1_1_MUTE_DONE. [1]MMP2_MUTE_DONE. [0]MMP1_MUTE_DONE.	

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BACH3 Register (Bank = 112D)				
Index	**Mnemonic**	**Bit**	**Description**	
112D96h	**REG112D96**	**15:0**	**Default : 0x0000**	**Access : RO**
	DPGA_MUTE_STS2[15:0]	15:0	0x96 DPGA_MUTE_STS2.	
112D98h	**REG112D98**	**15:0**	**Default : 0x0000**	**Access : RO**
	DPGA_MUTE_STS3[15:0]	15:0	0x98 DPGA_MUTE_STS3. [15:14]PGA_STATUS. [13:0]DPGA_STATUS.	

USBC (Single Port) Register (Bank = 1138)

USBC Register (Bank = 1138)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (113800h)	**RST_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved	
	OTG_XIU_ENABLE	6	The OTG XIU read and write operation are invalid if the bit is set to 1'b0.	
	UHC_XIU_ENABLE	5	The UHC XIU read and write operation are invalid if the bit is set to 1'b0.	
	-	4	Reserved for port1 in dual port design.	
	REG_SUSPEND_	3	Initial suspend control	
	OTG_RST	2	Write 1 to reset OTG controller.	
	UHC_RST	1	Write 1 to reset UHC controller.	
	USB_RST	0	Write 1 to reset USB controller.	
00h (113801h)	**-**	**7:0**	**Default : 0x02**	**Access : R/W**
		7:4	Reserved	
		3:2	Reserved for port1 in dual port design.	
	REG_VBUSVALID	1	Override vbusvalid value for port 0.	
	VBUS_SEL	0	The select option for vbusvalid in port 0. Default value is select to register value.	
01h (113802h)	**PORT_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:6	Reserved.	
	HSIC_EN	5	UTMI select 0: Normal UTMI 1: HSIC UTMI (UIC)	
	IDPULLUP_CTRL	4	OTG idpullup control.	
	PME_POL	3	Power management event polarity select	

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USBC Register (Bank = 1138)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INT_POL	2	Interrupt polarity select	
	PORT_CTRL	1:0	2'b00: UHC and OTG are both disable 2'b01: UHC enable 2'b10: OTG enable 2'b11: the setting is prohibited	
01h (113803h)	**-**	**7:0**	**Default : -**	**Access : -**
		7:0	Reserved	
02h (113804h)	**INTERRUPT_ENABLE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	ID_CHG_INTEN	3	The interrupt enable of status: ID state changed.	
	BVAL_CHG_INTEN	2	The interrupt enable of status: BVALID state changed.	
	AVAL_CHG_INTEN	1	The interrupt enable of status: AVALID state changed.	
	VBUS_CHG_INTEN	0	The interrupt enable of status: VBUSVALID state changed.	
02h (113805h)	**-**	**7:0**	**Default : -**	**Access : -**
	_	7:0	Reserved.	
03h (113806h)	**INTERRUPT_STATUS1**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	_	7:4	Reserved.	
	ID_CHG_STS	3	The interrupt status: ID state changed.	
	BVAL_CHG_STS	2	The interrupt status: BVALID state changed.	
	AVAL_CHG_STS	1	The interrupt status: AVALID state changed.	
	VBUS_CHG_STS	0	The interrupt status: VBUSVALID state changed.	
04h (113808h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	LINESTATE[1:0]	7:6	DM and DP single status.	
	SESSEND	5	UTMI status.	
	HOSTDISCON	4	Device disconnect in high speed mode.	
	IDDIG	3	PAD CID status.	
	BVALID	2	The status of Power detector.	
	AVALID	1	The status of Power detector.	
	VBUSVALID	0	The status of Power detector.	
04h (113809h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	ID_DEB_CNT[2:0]	7:5	PAD CID debouncing counter	
	RXACTIVE	4	UTMI data interface.	
	RXVALID	3	UTMI data interface.	

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USBC Register (Bank = 1138)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RXVALIDH	2	UTMI data interface.	
	RXERROR	1	UTMI data interface.	
	TXREADY	0	UTMI data interface.	
05h (11380Ah)	**Power Management Event Enable**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	11	Reserved	
	NEW_PV2MI_RD_SEL	10	Read burst size of new pv2mi bridge 2'b00=8 2'b01=16 2'b10=32 2'b11=64	
	NEW_PV2MI_WRT_SEL	9	Write burst size of new pv2mi bridge 2'b00=4 2'b01=8 2'b10=16 2'b11=32	
	UHC_DBUS_MASK	7	To mask uhc debug bus.	
	CONN_BVAL_INTEN	6	The interrupt and PME enable CONN_BVAL_STS.	
	CONN_AVAL_INTEN	5	The interrupt and PME enable CONN_AVAL_STS.	
	CONN_VBUS_INTEN	4	The interrupt and PME enable CONN_VBUS_STS.	
	RESET_INTEN	3	The interrupt and PME enable RESET_STS.	
	RESUME_INTEN	2	The interrupt and PME enable RESUME_STS.	
	DEV_DET_INTEN	1	The interrupt and PME enable DEV_DET_STS.	
	WAKEUP_INTEN	0	The interrupt and PME enable WAKEUP_STS.	
06h (11380Ch)	**Power Management Event Status**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	-	7	Reserved.	
	CONN_BVAL_STS	6	OTG detect bvalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_AVAL_STS	5	OTG detect avalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_VBUS_STS	4	OTG detect PAD_VBUS rising in the suspend mode. The status will both result interrupt and PME.	
	RESET_STS	3	OTG detect host send USB bus reset in suspend mode. The status will both result interrupt and PME.	

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USBC Register (Bank = 1138)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RESUME_STS	2	OTG detect host send USB bus resume signaling in suspend mode. The status will both result interrupt and PME.	
	DEV_DET_STS	1	UHC detect device plug-in in suspend mode. The status will both result interrupt and PME.	
	WAKEUP_STS	0	UHC detect device remote wakeup in suspend mode. The status will both result interrupt and PME.	
07h (11380Eh)	**uh2mi_adr_mask**	**7:0**	**Default : 0x00**	**Access : R/W**
	uh2mi_adr_mask	7:0	8 bit miu address mask for uh2mi_addr[29:22]	
07h (11380Fh)	**uh2mi_adr_ctrl**	**7:0**	**Default : 0x00**	**Access : R/W**
	Override mode value	2	Uh2mi_miu1_sel value when override mode is enabled	
	Override mode enable	1	uh2mi_miu1_sel override mode enable	
	Bit-wised mode enable	0	Bit-wised mode enable for uh2mi_adr[29:22]	

UHC2 Register (Bank = 1139)

UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (113900h)	**HCCAP**	**7:0**	**Default : 0x10**	**Access : RO**
	CAPLENGTH	7:0	Capability Register Length. This register is used as an offset to be added to register base to determine the beginning of the Operational Register Space.	
01h (113902h)	**HCCAP**	**7:0**	**Default : 0x00**	**Access : RO**
	HCIVERSION[7:0]	7:0	Host Controller Interface Version Number. This register is a two-byte register containing a BCD encoding of the EHCI revision number supported by the Host Controller.	
01h (113903h)	**HCCAP**	**7:0**	**Default : 0x01**	**Access : RO**
	HCIVERSION[15:8]	7:0	See description of '2402h'.	
02h (113904h)	**HCSPARAMS**	**7:0**	**Default : 0x01**	**Access : RO**
	-	7:4	Reserved.	
	N_PORTS	3:0	Number of Ports. This field specifies the number of physical	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			downstream ports implemented on the Host Controller.	
04h (113908h)	**HCCPARAMS**	**7:0**	**Default : 0x06**	**Access : RO**
	-	7:3	Reserved.	
	ASYN_SCH_PARK_CAP	2	Asynchronous Schedule Park Capability. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via the Frame List Size field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	PROG_FR_LIST_FLAG	1	Programmable Frame List Flag. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via Frame List Size Field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	-	0	Reserved.	
08h (113910h)	**USBCMD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INT_OAAD	6	Interrupt on Asynchronous Advance Doorbell. This bit is used as a doorbell by software to ring the Host Controller to issue an interrupt at the next advance of Asynchronous Schedule.	
	ASCH_EN	5	Asynchronous Schedule Enable. This bit controls whether the Host Controller skips the processing of Asynchronous Schedule. 0: Do not process Asynchronous Schedule. 1: Use the ASYNCLISTADDR register to access the Asynchronous Schedule.	
	PSCH_EN	4	Periodic Schedule Enable. This bit controls whether the Host Controller skips the processing of Periodic Schedule. 0: Do not process Periodic Schedule. 1: Use the PERIODICKISTBASE register to access the Periodic Schedule.	
	FRL_SIZE	3:2	Frame List Size. This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value).	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			01: 512 elements (2048 bytes). 10: 256 elements (1024 bytes). 11: Reserved.	
	HC_RESET	1	Host Controller Reset. This control bit is used by software to reset the Host Controller.	
	RS	0	Run/Stop. When this bit is set to '1', the Host Controller proceeds with the execution of schedule. 0: Stop. 1: Run.	
08h (113911h)	**USBCMD**	**7:0**	**Default : 0x0b**	**Access : R/W**
	-	7:4	Reserved.	
	ASYN_PK_EN	3	Asynchronous Schedule Park Mode Enable. Software uses this register to enable or disable the Park mode. When this register is set to 1, the Park mode is enabled.	
	-	2	Reserved.	
	ASYN_PK_CNT	1:0	Asynchronous Schedule Park Mode Count. This field contains a count for the number of successive transactions that the Host Controller is allowed to execute from a high-speed queue head on Asynchronous Schedule.	
09h (113912h)	**USBCMD**	**7:0**	**Default : 0x08**	**Access : R/W**
	INT_THRC	7:0	Interrupt Threshold Control. This field is used by system software to select the maximum rate at which the Host Controller will issue interrupts. The only valid values are described below: Value Maximum Interrupt Interval for High Speed 00h Reserved. 01h 1 micro-frame. 02h 2 micro-frames. 04h 4 micro-frames. 08h 8 micro-frames (default, equals to 1ms). 10h 16 micro-frames (2 ms). 20h 32 micro-frames (4 ms). 40h 64 micro-frames (8 ms). Note: For Full Speed, these registers are reserved.	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ah (113914h)	**USBSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:6	Reserved.	
	INT_OAA	5	Interrupt on Async Advance. This status bit indicates the assertion of interrupt on Async Advance Doorbell.	
	H_SYSERR	4	Host System Error. The Host Controller sets this bit to 1 when a serious error occurred during a host system access involving the Host Controller module.	
	FRL_ROL	3	Frame List Rollover. The Host Controller sets this bit to 1 when the Frame List Index rolls over from its maximum value to zero.	
	PO_CHG_DET	2	Port Change Detect. The Host Controller sets this bit to '1' when any port has a change bit transition from '0' to '1'. In addition, this bit is loaded with the OR of all of the PORTSC change bits.	
	USBERR_INT	1	USB Error Interrupt. The Host Controller sets this bit to '1' when the completion of a USB transaction results in an error condition.	
	USB_INT	0	USB Interrupt. The Host Controller sets this bit to '1' upon the completion of a USB transaction.	
0Ah (113915h)	**USBSTS**	**7:0**	**Default : 0x10**	**Access : RO**
	ASCH_STS	7	Asynchronous Schedule Status. This bit reports the actual status of Asynchronous Schedule.	
	PSCH_STS	6	Periodic Schedule Status. This bit reports the actual status of Periodic Schedule.	
	RECLAMATION	5	Reclamation. This is a read-only status bit, and is used to detect an empty of Asynchronous Schedule.	
	HCHALTED	4	Host Controller Halted. This bit is a zero whenever the Run/Stop bit is set to '1'. The Host Controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to '0'.	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:0	Reserved.	
0Ch (113918h)	**USBINTR**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_OAA_EN	5	Interrupt on Async Advance Enable. When this bit is set to '1', and the Interrupt on Async Advance bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	H_SYSERR_EN	4	Host System Error Enable. When this bit is set to '1', and the Host System Error Status bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	FRL_ROL_EN	3	Frame List Rollover Enable. When this bit is set to '1', and the Frame List Rollover bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	PO_CHG_INT_EN	2	Port Change Interrupt Enable. When this bit is set to '1', and the Port Change Detect bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	USBERR_INT_EN	1	USB Error Interrupt Enable. When this bit is set to '1', and the USBERRINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	USB_INT_EN	0	USB Interrupt Enable. When this bit is set to '1', and the USBINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
0Eh (11391Ch)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRINDEX[7:0]	7:0	Frame Index. This register is used by the Host Controller to index the frame into the Periodic Frame List. It updates every 125 microseconds. This register cannot be written unless the Host Controller is in the Halted state.	
0Eh (11391Dh)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FRINDEX[13:8]	5:0	See description of '1Ch'.	
12h (113925h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[15:12]	7:4	Periodic Frame List Base Address. This register contains the beginning address of the Periodic Frame List in the system memory. These bits correspond to memory address signals [31:12].	
	-	3:0	Reserved.	
13h (113926h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[23:16]	7:0	See description of '25h'.	
13h (113927h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[31:24]	7:0	See description of '25h'.	
14h (113928h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[7:5]	7:5	Current Asynchronous List Address. This register contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5].	
	-	4:0	Reserved.	
14h (113929h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[15:8]	7:0	Please see description of '28h'.	
15h (11392Ah)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[23:16]	7:0	Please see description of '28h'.	
15h (11392Bh)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[31:24]	7:0	Please see description of '28h'.	
18h (113930h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, R/WC, RO**
	PO_SUSP	7	Port Suspend (R/W). 1: Port is in suspend state. 0: Port is not in suspend state. The Port Enable bit and Suspend bit of this register define the port state as follows: Bits [Port Enable, Suspend] — Port State 0X — Disable 14 — Enable 15 — Suspend During the suspend state, downstream propagation of data is blocked on this port, except for port reset. While in the suspend state, the port is sensitive to	

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UHC2 Register (Bank = 1139)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			resume detection. Writing a zero to this bit is ignored by the Host Controller. The Host Controller will unconditionally set this bit to a zero when: Ÿ The software sets Force Port Resume bit to a zero (from a one) Ÿ The software sets Port Reset bit to a one (from a zero) Note: Before setting this bit, RUN/STOP bit should be set to 0.
	F_PO_RESM	6	Force Port Resume (R/W). 1: Resume detected/driven on port. 0: No resume detected/driven on port. Software sets this bit to a one to resume signaling. The Host Controller sets this bit to a one if a J-to-K transition is detected while the port is in the suspend state. When this bit transits to a one for the detection of a J-to-K transition, the Port Change Detect bit in USBSTS register is also set to a one.
	POR_RESET_STS	5	USB port reset status. The bit is a read only status.
		4	Reserved.
	PO_EN_CHG	3	Port Enable/Disable Change (R/WC). 1: Port enable/disable status has changed. 0: No change.
	PO_EN	2	Port Enable/Disable (R/W). 1: Enable. 0: Disable. Ports can only be enabled by the Host Controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field.
	CONN_CHG	1	Connect Status Change (R/WC). 1: Change current connect status. 0: No change. This bit indicates a change has occurred in the port's current connect status.
	CONN_STS	0	Current Connect Status (RO). 1: Device is present on the port. 0: No device is present. This value reflects the current state of the port, and may not correspond directly to cause the Connect

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Status Change bit to be set. When TST_FORCEEN is set to '1', this signal is the output of U_HDISCON.	
18h (113931h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	-	7:4	Reserved.	
	LINE_STS	3:2	Line Status (RO). These bits reflect the current logical levels of the D+ and D- signal lines.	
	-	1	Reserved.	
	PO_RESET	0	Port Reset. 1: Port is in reset. 0: Port is not in reset. When the software writes a one to this bit, the bus reset sequence as defined in the USB spec. is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence. Note: Before setting this bit, RUN/STOP bit should be set to 0.	
1Ah (113934h)	**HCMISC**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	U_SUSP_N	6	Transceiver Suspend Mode. Active LOW places the transceiver in suspend mode that draws minimal power from power supplies. This is part of the power management.	
	EOF2_TIME	5:4	EOF 2 Timing Points, controlling EOF 2 timing point before next SOF. High-Speed EOF2 Time: 00: 2 clocks (30 MHz) = 66ns. 01: 4 clocks (30 MHz) = 133ns. 10: 8 clocks (30 MHz) = 266ns. 11: 16 clocks (30 MHz) = 533ns. Full-Speed EOF2 Time: 00: 20 clocks (30 MHz) = 666ns. 01: 40 clocks (30 MHz) = 1.333us. 10: 80 clocks (30 MHz) = 2.66us. 11: 160 clocks (30 MHz) = 5.3us. Low-Speed EOF2 Time: 00: 40 clocks (30 MHz) = 1.33us.	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			01: 80 clocks (30 MHz) = 2.66us. 10: 160 clocks (30 MHz) = 5.33us. 11: 320 clocks (30 MHz) = 10.66us.	
	EOF1_TIME	3:2	EOF 1 Timing Points, controlling EOF 1 timing point before next SOF. This value should be adjusted according to the maximum packet size. High-Speed EOF1 Time: 00: 6us. 01: 12us. 10: 24us. 11: 36us. Full-Speed EOF1 Time: 00: 53.3us. 01: 70.0us. 10: 86.0us. 11: 700us. Low-Speed EOF1 Time: 00: 3750 clocks (30 MHz) = 125us. 01: 3500 clocks (30 MHz) = 116us. 10: 3250 clocks (30 MHz) = 108us. 11: 4000 clocks (30 MHz) = 133us.	
	ASYN_SCH_SLPT	1:0	Asynchronous Schedule Sleep Timer, controlling the Asynchronous Schedule sleep timer. 00: 5us. 01: 10us. 10: 15us. 11: 20us.	
20h (113940h)	**BMCS**	**7:0**	**Default : 0x10**	**Access : R/W**
	FORCE_NO_CHIRP	7	Force Full/Low speed mode	
	-	6:5	Reserved (must be set to '0' at all times).	
	VBUS_OFF	4	VBUS Off. This bit controls the voltage on VBUS ON/OFF (Default is OFF) or in other words, the signal U_DRVBUS. 0: VBUS On. 1: VBUS Off.	
	INT_POLARITY	3	Control the polarity of system interrupt signal SYS_INT_N. 0: Active LOW (default). 1: Active HIGH.	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HALF_SPEED	2	Half Speed Enable. 1: FIFO controller asserts ACK to DMA once every two clock cycles. 0: FIFO controller asserts ACK to DMA continuously. This bit is set to '1' while implementing FPGA.	
	HDISCON_FLT_SEL	1	Select a timer to filter out noise of HDISCON from UTMI+. 0: Approximated to 135 us. 1: Approximated to 270 us.	
	VBUS_FLT_SEL	0	Select a timer to filter out noise of VBUS_VLD from UTMI+. This signal is valid when signal U_VBUSVLD is connected. 0: Approximated to 135 us. 1: Approximated to 472 us.	
20h (113941h)	**BMCS**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	HOST_SPD_TYP	2:1	Host Speed Type, indicating speed type of the attached device. 10: HS. 00: FS. 01: LS. 11: Reserved.	
	VBUS_VLD	0	VBUS Valid. When the voltage on VBUS is above the valid VBUS threshold, this signal is valid when U_VBUSVLD is connected.	
22h (113944h)	**BUSMONINTSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:5	Reserved.	
	DMA_ERROR	4	DMA Error Interrupt. DMA operation cannot be finished normally, and an error signal is received. When CPU initiates DMA to fill up or read out device's FIFO, and DMA controller gets error response from system bus, this bit will be set. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DMA_CMPLT	3	DMA Completion Interrupt. DMA operation is finished normally. When CPU initiates DMA to fill up or read out device's FIFO, this	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			bit will be set after mission completion. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DPLGRMV	2	Device Plug Remove. This register is set to '1' once the device plug is removed. Writing '1' clears this register and writing '0' takes no effect.	
	OVC	1	Over Current Detection. This register is set to '1' when the VBUS does not reach VBUS_VLD within the expected time. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
	VBUS_ERR	0	VBUS Error. This register is set to '1' when the Bus Monitor state machine moves to "VBUS_ERROR" state. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
24h (113948h)	**BUSMONINTEN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMA_ERROR_EN	4	DMA_ERROR interrupt enable.	
	DMA_CMPLT_EN	3	DMA_CMPLT interrupt enable.	
	BPLGRMV_EN	2	BPLGRMV interrupt enable.	
	OVC_EN	1	OVC interrupt enable.	
	A_VBUS_ERR_EN	0	A_VBUS_ERR interrupt enable.	
28h (113950h)	**TST**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_LOOPBK	4	FIFO Loop Back Mode. A '1' turns on the loop-back mode. When this bit is set to '1', the Host Controller will enter the loop-back mode. During the loop-back mode, the Host Controller will use manual setting of DMA control to trigger DMA master.	
	TST_MOD	3	Test Mode. A '1' turns on the test mode. When this bit is set to '1', the Host Controller will enter the test mode. This test mode can save simulation time. In normal mode, the Host Controller uses a counter	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			for 10 ms detection of USB reset. The count is a large number. In test mode, the Host Controller will use a smaller number counter for USB reset detection to save the test cycle on test machine.	
	TST_PKT	2	Test Mode for Packet. Upon writing a '1' to this bit, the Host Controller repetitively sends the packet defined in UTMI spec. to transceiver. Run/Stop bit should also be enabled to enable the function.	
	TST_KSTA	1	Upon writing a '1', the D+/D- is set to the high-speed K state.	
	TST_JSTA	0	Upon writing a '1', the D+/D- is set to the high-speed J state.	
38h (113970h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DMA_IO	3	DMA IO to IO. Force DMA Controller not to toggle address. This bit is set when the DMA target is not a system memory but an IO device. If this register is set to '1', the 'DMA_LEN' must be an integer multiple of DWORD (4 byes), and the 'DMA_MADDR' must align to the boundary of DWORD (4 bytes).	
	-	2	Reserved.	
	DMA_TYPE	1	DMA Type, the transfer type of data moving. 0: FIFO to Memory. 1: Memory to FIFO.	
	DMA_START	0	DMA Start, informing DMA Controller to initiate DMA transfer. This bit is set to start the transfer and cleared when the DMA operation is completed. Note that this bit cannot be cleared by software; it can only be cleared by hardware in the case of either DMA completion or DMA error. Note that if DMA_LEN and DMA_START are set at the same time, the DMA_LEN will take effect immediately.	
38h (113971h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[7:0]	7:0	DMA Length.	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			The total bytes the DMA Controller will move. The unit is byte. The maximum length could be 1024B-1.	
39h (113972h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[15:8]	7:0	See description of '71h'.	
39h (113973h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DMA_LEN[16]	0	See description of '71h'.	
3Ah (113974h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[7:0]	7:0	DMA Memory Address. The starting address of memory to request DMA transfer.	
3Ah (113975h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[15:8]	7:0	See description of '74h'.	
3Bh (113976h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[23:16]	7:0	See description of '74h'.	
3Bh (113977h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[31:24]	7:0	See description of '74h'.	
40h (113980h)	**PROJ_SPEC_REG0**	7:0	**Default: 0x00**	**Access: R/W, WO**
	DBUS_SELECT	7:5	Selects debug bus banks.	
	SFT_CLK_RECOV	4	Clock recovery controlled by software. The register is R/W and the MIU clock will be always active if the bit is kept as 1.	
	OLD_XI2PV	3	Enables old version XIU access.	
	CLK_STOP	2	Triggers the clock stop mechanism. Set 1 to stop the all clock in UHC. The bit also represents the clock status of UHC. Reading the bit if it is 1, it represents the clock is stopped.	
	EN_RD_RD_SCRAMBLE	1	Enables memory inverted read.	
	EN_RD_WR_SCRAMBLE	0	Enables memory inverted write.	
40h (113981h)	**PROJ_SPEC_REG1**	**7:0**	**Default: 0x00**	**Access: R/W**
	SPLIT_SHORT_PKT_CLR_ACT	7	If the transfer is a periodic split transaction, the active status will be cleared when a short packet is received.	
	NON_ALIGN_EN	6	Enables MIU address non-alignment mode. It also means enabling new PV2MI bridge.	
	INVALID_MIU_ACS_INTEN	5	Enables interrupt when MIU invalid write occurs.	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MIU_WR_PROTECT_EN	4	Enables MIU write protect.	
	DAT_RD_PRI_EN	3	The enable option (MIU priority access) of the "data read".	
	DAT_WR_PRI_EN	2	The enable option (MIU priority access) of the "data write".	
	QT_RD_PRI_EN	1	The enable option (MIU priority access) of the "q-table read".	
	QT_WR_PRI_EN	0	The enable option (MIU priority access) of the "q-table write".	
41h (113982h)	**PROJ_SPEC_REG2**	**7:0**	**Default: 0x00**	**Access: R/W**
	QT_RD_PRI_SEL	7:6	The select (delay time of MIU priority assert) of the "q-table read". 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	QT_WR_PRI_SEL	5:4	The select (delay time of MIU priority assert) of the "q-table write". 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	DAT_RD_PRI_SEL	3:2	The select (delay time of MIU priority assert) of the "data read". 2'b00: 21.3us 2'b01: 16.0us 2'b10: 10.7us 2'b11: 5.3us	
	DAT_RD_PRI_SEL	1:0	The select (delay time of MIU priority assert) of the "data write". 2'b00: 21.3us 2'b01: 16.0us 2'b10: 10.7us 2'b11: 5.3us	
41h (113983h)	**PROJ_SPEC_REG3**	**7:0**	**Default: -**	**Access: R/W**
	Miu1_sel	7:6	2'b00: uh2mi_miu1_sel = uh2mi_adr[25] 2'b01: uh2mi_miu1_sel = uh2mi_adr[24] 2'b10: uh2mi_miu1_sel = uh2mi_adr[23]	

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2'b11: uh2mi_miu1_sel = uh2mi_adr[22]	
	Reserved	5	Reserved	
	En_last_done	4	Enable the mechanism that UHC state machine will wait until the last write data is done (mi2uh_last_done_z) when in write memory cycle.	
	Periodic_pri_sel	3:2	The select (delay time of MIU priority assert) of the periodic (Isochronous an Interrupt) transfer. 2'b00: 5.3us 2'b01: 4.0us 2'b10: 2.6us 2'b11: 1.3us	
	periodic_high_pri_en	1	Enable option for MIU high priority when proceeding periodic (Isochronous and Interrupt) transfer.	
	eof1_high_pri_en	0	Enable MIU high priority mechanism when in EOF1 window.	
42h (113984h)	fusbh200_dbus[7:0]	7:0	Internal bus for debugging.	
	FDBUS_REG1	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[15:8]	7:0	Internal bus for debugging.	
43h (113986h)	**FDBUS_REG2**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[23:16]	7:0	Internal bus for debugging.	
43h (113987h)	**FDBUS_REG3**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[31:24]	7:0	Internal bus for debugging.	
44h (113988h)	**FDBUS_REG4**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[39:32]	7:0	Internal bus for debugging.	
44h (113989h)	**FDBUS_REG5**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[47:40]	7:0	Internal bus for debugging.	
45h (11398Ah)	**STATUS_REG**	**7:0**	**Default: 0x00**	**Access: R/W1C**
	-	7:1	Reserved.	
	INVALID_MIU_ACS	0	Interrupt status of invalid MIU write.	
46h (11398Ch)	**MIU_WRITE_RANGE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[7:0]	7:0	MIU write protect lower boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
46h	**MIU_WRITE_RANGE1**	**7:0**	**Default: 0x00**	**Access: R/W**

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UHC2 Register (Bank = 1139)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(11398Dh)	LOWER_BOUND[15:8]	7:0	MIU write protect lower boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
47h (11398Eh)	**MIU_WRITE_RANGE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[23:16]	7:0	MIU write protect lower boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
47h (11398Fh)	**MIU_WRITE_RANGE3**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[7:0]	7:0	MIU write protect upper boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (113990h)	**MIU_WRITE_RANGE4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[15:8]	7:0	MIU write protect upper boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (113991h)	**MIU_WRITE_RANGE5**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[23:16]	7:0	MIU write protect upper boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	

GOPG0_0 Register (Bank = 1202)

GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**REG120200**	**7:0**	**Default : 0x09**	**Access : R/W**

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120200h)	5541_EN	7	RGB5541 alpha mask mode enable, only for RGB1555 Data type.	
	-	6	Reserved.	
	YUV_TRS_EN	5	YUV Transparent color enable.	
	GWIN_FLD_INV	4	Input Field inverse.	
	GWIN_PROG_MD	3	GWINs display mode. 0: Interlace. 1: Progress.	
	GWIN_HS_INV	2	Input Hsync inverse.	
	GWIN_VS_INV	1	Input Vsync inverse.	
	GWIN_RST	0	GOP soft reset.	
00h (120201h)	**REG120201**	**7:0**	**Default : 0x40**	**Access : R/W**
	ALPHA_INV	7	Alpha out inverse.	
	HS_MASK	6	1: Mask Hsync when VFDE is low. 0: No mask.	
	DISP_VBACK	5	V line read out direction. 0: Down. 1: Up.	
	DISP_HBACK	4	H pixel read out direction. 0: Forward. 1: Back.	
	RGB_TRS_EN	3	RGB Transparent color enable.	
	GWIN_YUVOUT	2	GOP out format. 0: RGB. 1: VYU.	
	-	1	Reserved.	
	OUT_RDY	0	Output ready.	
01h (120202h)	**REG120202**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_PINPON_DWIN	7	GWIN0 PINPON mode (with DWIN).	
	-	6:3	Reserved.	

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GWIN_DEST[2:0]	2:0	GOP destination. 0: SC0_IP_MAIN. 1: SC0_IP_SUB. 2: SC0_OP. 3: MVOP. 4: SC1_IP_MAIN. 5: SC1_OP. 6: SC2_OP. 7: DIP.	
01h (120203h)	**REG120203**	**7:0**	**Default : 0x42**	**Access : R/W**
	RI_END[3:0]	7:4	REGDMA interval end.	
	RI_STR[3:0]	3:0	REGDMA interval start.	
02h (120204h)	**REG120204**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ROLL_RATE[5:0]	5:0	Scroll Rate.	
02h (120205h)	**REG120205**	**7:0**	**Default : 0x15**	**Access : R/W**
	BLINK_EN	7	Blink enable.	
	BLINK_RATE[6:0]	6:0	Blink toggle duration.	
03h (120206h)	**REG120206**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[7:0]	7:0	Palette Table.	
03h (120207h)	**REG120207**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[15:8]	7:0	See description of '120206h'.	
04h (120208h)	**REG120208**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[23:16]	7:0	See description of '120206h'.	
04h (120209h)	**REG120209**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[31:24]	7:0	See description of '120206h'.	
05h (12020Ah)	**REG12020A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_ADR[7:0]	7:0	Palette Table address.	
05h (12020Bh)	**REG12020B**	**7:0**	**Default : 0x80**	**Access : R/W**
	PSRAM_BLKPRD[1:0]	7:6	Data Stable for 4N cycle before and after switching psram clk.	

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PSRAM_CTL[1:0]	5:4	Palette SRAM control. 0: RIU mode. 1: REGDMA mode. --- for external GOP engine---. 2: RIU mode. 3: REGDMA mode.	
	-	3	Reserved.	
	PSRAM_APART	2	Palette Table map apart for different GWIN.	
	PSRAM_RE	1	Palette Table read.	
	PSRAM_WE	0	Palette Table write.	
06h (12020Ch)	**REG12020C**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGDMA_END[7:0]	7:0	END address for REGDMA mode.	
06h (12020Dh)	**REG12020D**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGDMA_STR[6:0]	7:1	Start Base address for REGDMA mode. Start address = REGDMA_STR<<9;	
	REGDMA_END[8]	0	See description of '12020Ch'.	
07h (12020Eh)	**REG12020E**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGDMA_STR[14:7]	7:0	See description of '12020Dh'.	
07h (12020Fh)	**REG12020F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	REGDMA_STR[18:15]	3:0	See description of '12020Dh'.	
08h (120210h)	**REG120210**	**7:0**	**Default : 0xBF**	**Access : R/W**
	-	7:5	Reserved.	
	DUMMY0_INT_MASK	4	Dummy0 interrupt mask.	
	FLD_INT_MASK	3	Fld interrupt mask.	
	REGDMA_ERR_INT_MASK	2	REGDMA error interrupt mask.	
	VS1_INT_MASK	1	VS1 interrupt mask.	
	VS0_INT_MASK	0	VS0 interrupt mask.	
08h (120211h)	**REG120211**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	FLD	6	Field info.	
	-	5:4	Reserved.	
	FLD_ERR_INT	3	Field interrupt.	
	-	2	Reserved.	

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VS1_INT	1	VS1 interrupt flag.	
	VS0_INT	0	VS0 interrupt flag.	
09h (120212h)	**REG120212**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	RDMA_STATE[2:0]	2:0	RDMA state. 0: REGDMA_STR. 1: REGDMA_SEND0. 2: REGDMA_SEND1. 4: WAIT_RDMA_GO. 6: WAIT_MIU_ACK. 7: DMA_IDLE.	
09h (120213h)	**REG120213**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	LB0_BIST_FAIL	6	LB0 BIST.	
	PSRAM_BIST_FAIL	5	PSRAM BIST.	
	GW_FF_BIST_FAIL	4	Buffer BIST.	
	LB_UF	3	Line buffer underflow.	
	LB_OF	2	Line buffer overflow.	
	GW_UF	1	Buffer underflow.	
	GW_OF	0	Buffer overflow.	
0Ah (120214h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Bh (120216h)	**REG120216**	**7:0**	**Default : 0x00**	**Access : R/W**
	THREE_D_MIDDLE_OFFSET_Q[7:0]	7:0	Garbage line num in top bottom mode. (offset shoud be set to 0 on ip).	
0Bh (120217h)	**REG120217**	**7:0**	**Default : 0x00**	**Access : R/W**
	RDMA_FF_CMPRS_EN_Q[1:0]	7:6	Enable rdma ff compress. 00: Compress mode off. 01: Transparent mode. 10: Uni color mode. 11: Both transparent/ uni color mode.	
	HANDSHAKE_MODE_Q	5	Enable hand-shaking valid bit =1.	
	THREE_D_PIX_INI_Q[4:0]	4:0	Set initial start pix in side by side mode.	
0Ch (120218h)	**REG120218**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_PIX_NUM_Q[7:0]	7:0	Set output valid bit num in one line.	

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (120219h)	**REG120219**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_PIX_NUM_Q[11:8]	3:0	See description of '120218h'.	
0Dh (12021Ah)	**REG12021A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_LINE_NUM_Q[7:0]	7:0	Set output valid line num in one frame.	
0Dh (12021Bh)	**REG12021B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_LINE_NUM_Q[11:8]	3:0	See description of '12021Ah'.	
0Eh (12021Ch)	**REG12021C**	**7:0**	**Default : 0x69**	**Access : R/W**
	RDMA_HT[7:0]	7:0	RDMA H total (unit: 2 pixels) > reg_strch_size.	
0Eh (12021Dh)	**REG12021D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	RDMA_HT[10:8]	2:0	See description of '12021Ch'.	
0Fh (12021Eh)	**REG12021E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PIPE_Q[7:0]	7:0	Hsync input pipe delay.	
0Fh (12021Fh)	**REG12021F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HS_PIPE_Q[9:8]	1:0	See description of '12021Eh'.	
10h (120220h)	**REG120220**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SLOW_RATIO[5:0]	5:0	FIFO read out slow ratio.	
10h (120221h)	**REG120221**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SLOW_THD[6:0]	6:0	FIFO out speed slow down when data counts <= SLOW_THD.	
11h (120222h)	**REG120222**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_Q[7:0]	7:0	Brightness value: -256~255. Use 2's complement.	
11h (120223h)	**REG120223**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	CON_YG_Q[5:0]	6:1	Y Contrast gain. Gain = REG_CON / 16.	
	BRI_Q[8]	0	See description of '120222h'.	

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (120224h)	**REG120224**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_UB_Q[5:0]	5:0	U Contrast gain. Gain = REG_CON / 16.	
12h (120225h)	**REG120225**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_VR_Q[5:0]	5:0	V Contrast gain. Gain = REG_CON / 16.	
13h ~ 18h (120226h ~ 120231h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
19h (120232h)	**REG120232**	**7:0**	**Default : 0xF0**	**Access : R/W**
	DMA_THD[7:0]	7:0	DMA FIFO threshold.	
19h (120233h)	**REG120233**	**7:0**	**Default : 0x42**	**Access : R/W**
	GW_HI_TSH[1:0]	7:6	DMA access high priority.	
	-	5	Reserved.	
	DMA_EXT[4:0]	4:0	DMA Burst length new mode: DMA_EXT [4:0]. 0: FF depth - current level. (equal the "burst all" in old mode). 31: 255. else: 8*DMA_EXT.	
1Ch (120238h)	**REG120238**	**7:0**	**Default : 0x7D**	**Access : R/W**
	-	7	Reserved.	
	DMA_BURST_LEVEL[6:0]	6:0	Target level of rdma ff each time into burst state, valid level : h0~h7d(0~125).	
1Ch (120239h)	**REG120239**	**7:0**	**Default : 0x00**	**Access : R/W**
	LB_COUPLE_EN	7	Couple RDMA ff with strch ff when strch_V off.	
	-	6:0	Reserved.	
1Dh (12023Ah)	**REG12023A**	**7:0**	**Default : 0x20**	**Access : R/W**
	ACCURATE_HI_TSH_EN	7	DMA access high priority : accurate mode enable.	
	ACCURATE_GW_HI_TSH[6:0]	6:0	DMA access high priority level (unit : 1/128 FF depth).	
1Eh (12023Ch)	**REG12023C**	**7:0**	**Default : 0x20**	**Access : R/W**
	THREE_D_MIDDLE_Q[7:0]	7:0	Set three d middle.	
1Eh	**REG12023D**	**7:0**	**Default : 0x01**	**Access : R/W**

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(12023Dh)	-	7:4	Reserved.	
	THREE_D_MIDDLE_Q[11:8]	3:0	See description of '12023Ch'.	
20h (120240h)	**REG120240**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	PRI1_Q[1:0]	5:4	2nd priority GWIN number.	
	-	3:2	Reserved.	
	PRI0_Q[1:0]	1:0	1st priority GWIN number.	
22h ~ 23h (120244h ~ 120247h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
24h (120248h)	**REG120248**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[7:0]	7:0	Transparent color key {R[7:0], G[7:0], B[7:0]}: for RGB source.	
24h (120249h)	**REG120249**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[15:8]	7:0	See description of '120248h'.	
25h (12024Ah)	**REG12024A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[23:16]	7:0	See description of '120248h'.	
26h (12024Ch)	**REG12024C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[7:0]	7:0	Transparent color key {V[7:0], Y[7:0], U[7:0]}: for YUV source.	
26h (12024Dh)	**REG12024D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[15:8]	7:0	See description of '12024Ch'.	
27h (12024Eh)	**REG12024E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[23:16]	7:0	See description of '12024Ch'.	
28h (120250h)	**REG120250**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	THREE_D_MODE_Q[2:0]	3:1	3D OSD mode: 0: Off. 1: L/R swith by frame. 2: L/R side by side. 3: L/R top - bottom. 4: L/R line alternative.	
	3D_FLAG_INV_Q	0	Input 3D flag L/R inverse.	
28h	**REG120251**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120251h)	YC_SWAP_Q	7	Switch Y/C when dtype is UV8Y8.	
	UV_SWAP_Q	6	Switch U/V (R/B).	
	-	5:0	Reserved.	
2Eh ~ 2Fh (12025Ch ~ 12025Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (120260h)	**REG120260**	**7:0**	**Default : 0x68**	**Access : R/W**
	STRCH_HSIZE_Q[7:0]	7:0	Stretch Window H size (unit: 2 pixel). When V stretch ratio=1, hsize has no size limit. When V stretch ratio !=1, the max hsize is limited by line buffer size.	
30h (120261h)	**REG120261**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	STRCH_HSIZE_Q[10:8]	2:0	See description of '120260h'.	
31h (120262h)	**REG120262**	**7:0**	**Default : 0x40**	**Access : R/W**
	STRCH_VSIZE_Q[7:0]	7:0	Stretch Window V size.	
31h (120263h)	**REG120263**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VSIZE_Q[11:8]	3:0	See description of '120262h'.	
32h (120264h)	**REG120264**	**7:0**	**Default : 0x64**	**Access : R/W**
	STRCH_HST_Q[7:0]	7:0	Stretch Window H coordinate.	
32h (120265h)	**REG120265**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	STRCH_HST_Q[12:8]	4:0	See description of '120264h'.	
34h (120268h)	**REG120268**	**7:0**	**Default : 0x00**	**Access : R/W**
	STRCH_VST_Q[7:0]	7:0	Stretch Window V coordinate.	
34h (120269h)	**REG120269**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VST_Q[11:8]	3:0	See description of '120268h'.	
35h (12026Ah)	**REG12026A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSTRCH_Q[7:0]	7:0	Stretch H ratio. = In/Out* 2^12.	
35h	**REG12026B**	**7:0**	**Default : 0x10**	**Access : R/W**

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(12026Bh)	-	7:5	Reserved.	
	HSTRCH_Q[12:8]	4:0	See description of '12026Ah'.	
36h (12026Ch)	**REG12026C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTRCH_Q[7:0]	7:0	Stretch V ratio.	
36h (12026Dh)	**REG12026D**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	VSTRCH_Q[12:8]	4:0	See description of '12026Ch'.	
38h (120270h)	**REG120270**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSTRCH_INI_Q[7:0]	7:0	Stretch H start value.	
38h (120271h)	**REG120271**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HSTRCH_INI_Q[12:8]	4:0	See description of '120270h'.	
39h (120272h)	**REG120272**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTRCH_INI_Q[7:0]	7:0	Stretch V start value.	
39h (120273h)	**REG120273**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VSTRCH_INI_Q[12:8]	4:0	See description of '120272h'.	
3Ah (120274h)	**REG120274**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TRS_STRCH	4	0: Transparent color only duplicate if stretch. 1: Stretch transparent color like normal color.	
	VSTRCH_MD[1:0]	3:2	V-stretch mode. 0: Linear. 1: Duplicate. 2: Nearest.	
	HSTRCH_MD[1:0]	1:0	H-stretch mode. 0: 6-tap (including nearest). 1: Duplicate.	
3Bh (120276h)	**REG120276**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	DYNAMIC_GATING_EN_Q	5	Enable dynamic gating.	
	-	4	Reserved.	
	OLD_ADDR	3	0: GOP DMA use new address. 1: GOP DMA use old address.	

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GOPG0_0 Register (Bank = 1202)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MIU_REQ_DISABLE	2	0: Normal gop to miu access. 1: Disable gop to miu access.	
	-	1:0	Reserved.	
3Bh (120277h)	**REG120277**	**7:0**	**Default : 0x80**	**Access : R/W**
	MIUREQ_HOLD_CYCLE_Q[3:0]	7:4	Compress mode turn on, set miu req hold time. base: 4. - >holdtime = miureq_hold_cycle x 4 x (cmpress rate).	
	-	3:0	Reserved.	
3Ch (120278h)	**REG120278**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CMQ_VS0_INT_MASK	5	CMQ VS0 interrupt mask.	
	-	4	Reserved.	
	MASK_1ST_HS_EVEN_Q	3	Mask 1st hsync in even field for GOP_VE.	
	MASK_1ST_HS_ODD_Q	2	Mask 1st hsync in odd field for GOP_VE.	
	-	1:0	Reserved.	
60h ~ 63h (1202C0h ~ 1202C7h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
70h ~ 71h (1202E0h ~ 1202E3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
74h (1202E8h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
75h ~ 75h (1202EAh ~ 1202EBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
78h (1202F0h)	**REG1202F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	REGDMA_ONESHOT	1	REGDMA write only in one frame start.	
	REGDMA_EN	0	REGDMA write mode enable.	
78h (1202F1h)	**REG1202F1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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GOPG0_0 Register (Bank = 1202)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	REGDMA_ACK	0	REGDMA DONE ACK. sequence: 1: {REGDMA_oneshot, REG_REGDMA_EN}=2'b11. 2: Wait REGDMA_ACK. 3: Clear REG_REGDMA_EN.

GOPG0_1 Register (Bank = 1203)

GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (120300h)	**REG120300**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_DTYPE_Q[3:0]	7:4	GWIN0 Source Data Type. 0: RGB1555/Blink. 1: RGB565. 2: ARGB4444. 3: 2266. 4. 8bit palette. 5: ARGB8888. 6: ARGB1555. 7.ABGR8888. 8: RGB1555/UV7Y8. 9: UV8Y8. 10.RGBA5551. 11.RGBA4444.	
	GWIN0_HROLL_Q	3	GWIN0 Horizontal scroll enable (H/V scroll cannot be enabled at the same time).	
	GWIN0_VROLL_Q	2	GWIN0 Vertical scroll enable (H/V scroll cannot be enabled at the same time).	
	DRAM_GWIN0_RSTOP_Q	1	GWIN0 H/V scroll auto-stop enable.	
	GWIN0_EN	0	Graphic window 0 Enable.	
00h (120301h)	**REG120301**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_TILE_16BPP_Q	7	16bpp Tile mode format. 0: Linear. 1: Tile mode.	

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GWIN0_ALPHA_EN_Q	6	GWIN0 alpha_enable. 1: Pixel alpha. 0: Constant alpha.	
	-	5:0	Reserved.	
01h (120302h)	**REG120302**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, unit 1 word.	
01h (120303h)	**REG120303**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[15:8]	7:0	See description of '120302h'.	
02h (120304h)	**REG120304**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[23:16]	7:0	See description of '120302h'.	
02h (120305h)	**REG120305**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_Q[27:24]	3:0	See description of '120302h'.	
03h (120306h)	**REG120306**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HSTR_PIX0_Q[4:0]	4:0	Delete pixel number at hstart for pixel alignment unit:1 pixel.	
03h (120307h)	**REG120307**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HEND_PIX0_Q[4:0]	4:0	Delete pixel number at hend for pixel alignment unit:1 pixel.	
04h (120308h)	**REG120308**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_HSTR_Q[7:0]	7:0	The horizontal start pixel of Display Image for GWIN0. Unit: 1 word pixels.	
04h (120309h)	**REG120309**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HSTR_Q[10:8]	2:0	See description of '120308h'.	
05h (12030Ah)	**REG12030A**	**7:0**	**Default : 0x01**	**Access : R/W**
	GWIN0_HEND_Q[7:0]	7:0	The horizontal end pixel of Display Image for GWIN0. Unit: 1 word pixels.	
05h (12030Bh)	**REG12030B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HEND_Q[10:8]	2:0	See description of '12030Ah'.	

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (12030Ch)	**REG12030C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VSTR_Q[7:0]	7:0	The vertical start line of Display Image for GWIN0. Unit: 1 line.	
06h (12030Dh)	**REG12030D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VSTR_Q[11:8]	3:0	See description of '12030Ch'.	
07h ~ 07h (12030Eh ~ 12030Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
08h (120310h)	**REG120310**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VEND_Q[7:0]	7:0	The vertical end line of Display Image for GWIN0. Unit: 1 line.	
08h (120311h)	**REG120311**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VEND_Q[11:8]	3:0	See description of '120310h'.	
09h (120312h)	**REG120312**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK0_HSIZE_Q[7:0]	7:0	Ring Block0 line size.	
09h (120313h)	**REG120313**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RBLK0_HSIZE_Q[10:8]	2:0	See description of '120312h'.	
0Ah (120314h)	**REG120314**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_ALPHA_Q[7:0]	7:0	GWIN0 constant alpha.	
0Bh ~ 0Bh (120316h ~ 120317h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ch (120318h)	**REG120318**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[7:0]	7:0	GWIN0 1st data offset address after REG_DRAM_RBLK0_STR, unit: 1 word.	
0Ch (120319h)	**REG120319**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[15:8]	7:0	See description of '120318h'.	
0Dh (12031Ah)	**REG12031A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[23:16]	7:0	See description of '120318h'.	

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Dh (12031Bh)	**REG12031B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN0_VSTR_Q[27:24]	3:0	See description of '120318h'.	
0Eh (12031Ch)	**REG12031C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_HSTR_Q[7:0]	7:0	GWIN0 1st word offset of each line, unit 1 word.	
0Eh (12031Dh)	**REG12031D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DRAM_GWIN0_HSTR_Q[10:8]	2:0	See description of '12031Ch'.	
10h (120320h)	**REG120320**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_SIZE_Q[7:0]	7:0	Ring Block 0 size, unit: 1 word.	
10h (120321h)	**REG120321**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_SIZE_Q[15:8]	7:0	See description of '120320h'.	
11h (120322h)	**REG120322**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_SIZE_Q[23:16]	7:0	See description of '120320h'.	
11h (120323h)	**REG120323**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_SIZE_Q[27:24]	3:0	See description of '120320h'.	
12h (120324h)	**REG120324**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_RLENGTH_Q[7:0]	7:0	GWIN0 Scroll length. Vertical use [15:0], Horizontal use [7:0], [7] is sign bit, use 2's complement. unit: 1 word pixels.	
12h (120325h)	**REG120325**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_RLENGTH_Q[15:8]	7:0	See description of '120324h'.	
14h (120328h)	**REG120328**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_HVSTOP_Q[7:0]	7:0	Scroll auto-stop offset. Vertical use [21:0], Horizontal use [9:0], unit 1 word.	
14h (120329h)	**REG120329**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_HVSTOP_Q[15:8]	7:0	See description of '120328h'.	
15h (12032Ah)	**REG12032A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_HVSTOP_Q[23:16]	7:0	See description of '120328h'.	
15h (12032Bh)	**REG12032B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN0_HVSTOP_Q[27:24]	3:0	See description of '120328h'.	

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (12032Ch)	**REG12032C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GWIN0_FADE_INC_Q	6	FADE IN/OUT. 1: Stronger. 0: Weaker.	
	GWIN0_FADE_INI_Q	5	FADE Initial.	
	GWIN0_FADE_EN_Q	4	FADE enable.	
	GWIN0_FADE_RATE_Q[3:0]	3:0	FADE frame Rate for GWIN0.	
16h (12032Dh)	**REG12032D**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:6	Reserved.	
	BG0_EN_Q	5	Graphic Background Window Enable.	
	BG0_ALPHA_EN_Q	4	BG WIN0 alpha enable.	
	BG0_ALPHA_Q[3:0]	3:0	BG WIN0 alpha.	
18h (120330h)	**REG120330**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG0_CLR_Q[7:0]	7:0	BGWIN0 color.	
18h (120331h)	**REG120331**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG0_CLR_Q[15:8]	7:0	See description of '120330h'.	
19h (120332h)	**REG120332**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG0_HSTR_Q[7:0]	7:0	BGWIN0 H start pixel.	
19h (120333h)	**REG120333**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG0_HSTR_Q[11:8]	3:0	See description of '120332h'.	
1Ah (120334h)	**REG120334**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG0_HEND_Q[7:0]	7:0	BGWIN0 H end pixel.	
1Ah (120335h)	**REG120335**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG0_HEND_Q[11:8]	3:0	See description of '120334h'.	
1Ch (120338h)	**REG120338**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG0_VSTR_Q[7:0]	7:0	BGWIN0 V start line.	
1Ch (120339h)	**REG120339**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG0_VSTR_Q[11:8]	3:0	See description of '120338h'.	
1Dh	**REG12033A**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(12033Ah)	BG0_VEND_Q[7:0]	7:0	BGWIN0 V end line.	
1Dh (12033Bh)	**REG12033B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG0_VEND_Q[11:8]	3:0	See description of '12033Ah'.	
1Eh (12033Ch)	**REG12033C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, 3D L/R mode unit 1 word.	
1Eh (12033Dh)	**REG12033D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[15:8]	7:0	See description of '12033Ch'.	
1Fh (12033Eh)	**REG12033E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[23:16]	7:0	See description of '12033Ch'.	
1Fh (12033Fh)	**REG12033F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_LR_Q[27:24]	3:0	See description of '12033Ch'.	
20h (120340h)	**REG120340**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_DTYPE_Q[3:0]	7:4	GWIN1 Source Data Type.	
	GWIN1_HROLL_Q	3	GWIN1 Horizontal scroll enable (H/V scroll cannot be enabled at the same time).	
	GWIN1_VROLL_Q	2	GWIN1 Vertical scroll enable (H/V scroll cannot be enabled at the same time).	
	DRAM_GWIN1_RSTOP_Q	1	GWIN1 H/V scroll auto-stop enable.	
	GWIN1_EN	0	Graphic window 1 Enable.	
20h (120341h)	**REG120341**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_TILE_16BPP_Q	7	16bpp Tile mode format.	
	GWIN1_ALPHA_EN_Q	6	GWIN1 alpha_enable. 1: Pixel alpha. 0: Constant alpha.	
	-	5:0	Reserved.	
21h (120342h)	**REG120342**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_Q[7:0]	7:0	Ring Block start address in dram for GWIN1 read out, unit 1 word.	
21h (120343h)	**REG120343**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_Q[15:8]	7:0	See description of '120342h'.	
22h	**REG120344**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120344h)	DRAM_RBLK1_STR_Q[23:16]	7:0	See description of '120342h'.	
22h (120345h)	**REG120345**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK1_STR_Q[27:24]	3:0	See description of '120342h'.	
23h (120346h)	**REG120346**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HSTR_PIX1_Q[4:0]	4:0	Delete pixel number at hstart for pixel alignment unit:1 pixel.	
23h (120347h)	**REG120347**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HEND_PIX1_Q[4:0]	4:0	Delete pixel number at hend for pixel alignment unit:1 pixel.	
24h (120348h)	**REG120348**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_HSTR_Q[7:0]	7:0	The horizontal start pixel of Display Image for GWIN1. Unit: 1 word pixels.	
24h (120349h)	**REG120349**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN1_HSTR_Q[10:8]	2:0	See description of '120348h'.	
25h (12034Ah)	**REG12034A**	**7:0**	**Default : 0x01**	**Access : R/W**
	GWIN1_HEND_Q[7:0]	7:0	The horizontal end pixel of Display Image for GWIN1. Unit: 1 word pixels.	
25h (12034Bh)	**REG12034B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN1_HEND_Q[10:8]	2:0	See description of '12034Ah'.	
26h (12034Ch)	**REG12034C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_VSTR_Q[7:0]	7:0	The vertical start line of Display Image for GWIN1 unit: 1 line.	
26h (12034Dh)	**REG12034D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN1_VSTR_Q[11:8]	3:0	See description of '12034Ch'.	
27h ~ 27h (12034Eh ~ 12034Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (120350h)	**REG120350**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_VEND_Q[7:0]	7:0	The vertical end line of Display Image for GWIN1 Unit: 1 line.	
28h (120351h)	**REG120351**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN1_VEND_Q[11:8]	3:0	See description of '120350h'.	
29h (120352h)	**REG120352**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK1_HSIZE_Q[7:0]	7:0	Ring Block1 line size.	
29h (120353h)	**REG120353**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RBLK1_HSIZE_Q[10:8]	2:0	See description of '120352h'.	
2Ah (120354h)	**REG120354**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_ALPHA_Q[7:0]	7:0	GWIN1 constant alpha.	
2Ch (120358h)	**REG120358**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_VSTR_Q[7:0]	7:0	GWIN1 1st data offset address after. REG_DRAM_RBLK1_STR, unit: 1 word.	
2Ch (120359h)	**REG120359**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_VSTR_Q[15:8]	7:0	See description of '120358h'.	
2Dh (12035Ah)	**REG12035A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_VSTR_Q[23:16]	7:0	See description of '120358h'.	
2Dh (12035Bh)	**REG12035B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN1_VSTR_Q[27:24]	3:0	See description of '120358h'.	
2Eh (12035Ch)	**REG12035C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_HSTR_Q[7:0]	7:0	GWIN1 1st word offset of each line, unit 1 word.	
2Eh (12035Dh)	**REG12035D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DRAM_GWIN1_HSTR_Q[10:8]	2:0	See description of '12035Ch'.	
30h (120360h)	**REG120360**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_SIZE_Q[7:0]	7:0	Ring Block 1 size, unit 1 word.	
30h (120361h)	**REG120361**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_SIZE_Q[15:8]	7:0	See description of '120360h'.	
31h	**REG120362**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120362h)	DRAM_RBLK1_SIZE_Q[23:16]	7:0	See description of '120360h'.	
31h (120363h)	**REG120363**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK1_SIZE_Q[27:24]	3:0	See description of '120360h'.	
32h (120364h)	**REG120364**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_RLENGTH_Q[7:0]	7:0	GWIN1 Scroll length. Vertical use [15:0], Horizontal use [7:0], [7] is sign bit, use 2's complement. unit: 1 word pixels.	
32h (120365h)	**REG120365**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_RLENGTH_Q[15:8]	7:0	See description of '120364h'.	
34h (120368h)	**REG120368**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_HVSTOP_Q[7:0]	7:0	Scroll auto-stop offset. Vertical use [21:0], Horizontal use [9:0], unit 1 word.	
34h (120369h)	**REG120369**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_HVSTOP_Q[15:8]	7:0	See description of '120368h'.	
35h (12036Ah)	**REG12036A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_HVSTOP_Q[23:16]	7:0	See description of '120368h'.	
35h (12036Bh)	**REG12036B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN1_HVSTOP_Q[27:24]	3:0	See description of '120368h'.	
36h (12036Ch)	**REG12036C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GWIN1_FADE_INC_Q	6	FADE IN/OUT. 1: Stronger. 0: Weaker.	
	GWIN1_FADE_INI_Q	5	FADE Initial.	
	GWIN1_FADE_EN_Q	4	FADE enable.	
	GWIN1_FADE_RATE_Q[3:0]	3:0	FADE frame Rate for GWIN1.	
36h (12036Dh)	**REG12036D**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:6	Reserved.	
	BG1_EN_Q	5	Graphic Background Window Enable.	
	BG1_ALPHA_EN_Q	4	BG WIN1 alpha enable.	
	BG1_ALPHA_Q[3:0]	3:0	BG WIN1 alpha.	

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GOPG0_1 Register (Bank = 1203)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (120370h)	**REG120370**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG1_CLR_Q[7:0]	7:0	BGWIN1 color.	
38h (120371h)	**REG120371**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG1_CLR_Q[15:8]	7:0	See description of '120370h'.	
39h (120372h)	**REG120372**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG1_HSTR_Q[7:0]	7:0	BGWIN1 H start pixel.	
39h (120373h)	**REG120373**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG1_HSTR_Q[11:8]	3:0	See description of '120372h'.	
3Ah (120374h)	**REG120374**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG1_HEND_Q[7:0]	7:0	BGWIN1 H end pixel.	
3Ah (120375h)	**REG120375**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG1_HEND_Q[11:8]	3:0	See description of '120374h'.	
3Ch (120378h)	**REG120378**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG1_VSTR_Q[7:0]	7:0	BGWIN1 V start line.	
3Ch (120379h)	**REG120379**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG1_VSTR_Q[11:8]	3:0	See description of '120378h'.	
3Dh (12037Ah)	**REG12037A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BG1_VEND_Q[7:0]	7:0	BGWIN1 V end line.	
3Dh (12037Bh)	**REG12037B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BG1_VEND_Q[11:8]	3:0	See description of '12037Ah'.	
3Eh (12037Ch)	**REG12037C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_LR_Q[7:0]	7:0	Ring Block start address in dram for GWIN1 read out, 3D L/R mode unit 1 word.	
3Eh (12037Dh)	**REG12037D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_LR_Q[15:8]	7:0	See description of '12037Ch'.	
3Fh (12037Eh)	**REG12037E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_LR_Q[23:16]	7:0	See description of '12037Ch'.	
3Fh (12037Fh)	**REG12037F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

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GOPG0_1 Register (Bank = 1203)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	DRAM_RBLK1_STR_LR_Q[27:24]	3:0	See description of '12037Ch'.

GOPG1_0 Register (Bank = 1205)

GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (120500h)	**REG120500**	**7:0**	**Default : 0x09**	**Access : R/W**
	5541_EN	7	RGB5541 alpha mask mode enable, only for RGB1555 Data type.	
	-	6	Reserved.	
	YUV_TRS_EN	5	YUV Transparent color enable.	
	GWIN_FLD_INV	4	Input Field inverse.	
	GWIN_PROG_MD	3	GWINs display mode. 0: Interlace. 1: Progress.	
	GWIN_HS_INV	2	Input Hsync inverse.	
	GWIN_VS_INV	1	Input Vsync inverse.	
	GWIN_RST	0	GOP soft reset.	
00h (120501h)	**REG120501**	**7:0**	**Default : 0x40**	**Access : R/W**
	ALPHA_INV	7	Alpha out inverse.	
	HS_MASK	6	1: Mask Hsync when VFDE is low. 0: No mask.	
	DISP_VBACK	5	V line read out direction. 0: Down. 1: Up.	
	DISP_HBACK	4	H pixel read out direction. 0: Forward. 1: Back.	
	RGB_TRS_EN	3	RGB Transparent color enable.	
	GWIN_YUVOUT	2	GOP out format. 0: RGB. 1: VYU.	
	-	1	Reserved.	

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OUT_RDY	0	Output ready.	
01h (120502h)	**REG120502**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_PINPON_DWIN	7	GWIN0 PINPON mode (with DWIN).	
	-	6:3	Reserved.	
	GWIN_DEST[2:0]	2:0	GOP destination. 0: SC0_IP_MAIN. 1: SC0_IP_SUB. 2: SC0_OP. 3: MVOP. 4: SC1_IP_MAIN. 5: SC1_OP. 6: SC2_OP. 7: DIP.	
01h (120503h)	**REG120503**	**7:0**	**Default : 0x42**	**Access : R/W**
	RI_END[3:0]	7:4	REGDMA interval end.	
	RI_STR[3:0]	3:0	REGDMA interval start.	
02h (120505h)	**REG120505**	**7:0**	**Default : 0x15**	**Access : R/W**
	BLINK_EN	7	Blink enable.	
	BLINK_RATE[6:0]	6:0	Blink toggle duration.	
03h (120506h)	**REG120506**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[7:0]	7:0	Palette Table.	
03h (120507h)	**REG120507**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[15:8]	7:0	See description of '120506h'.	
04h (120508h)	**REG120508**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[23:16]	7:0	See description of '120506h'.	
04h (120509h)	**REG120509**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_WD[31:24]	7:0	See description of '120506h'.	
05h (12050Ah)	**REG12050A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRAM_ADR[7:0]	7:0	Palette Table address.	
05h (12050Bh)	**REG12050B**	**7:0**	**Default : 0x80**	**Access : R/W**
	PSRAM_BLKPRD[1:0]	7:6	Data Stable for 4N cycle before and after switching psram clk.	

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PSRAM_CTL[1:0]	5:4	Palette SRAM control. 0: RIU mode. 1: REGDMA mode. --- for external GOP engine---. 2: RIU mode. 3: REGDMA mode.	
	-	3	Reserved.	
	PSRAM_APART	2	Palette Table map apart for different GWIN.	
	PSRAM_RE	1	Palette Table read.	
	PSRAM_WE	0	Palette Table write.	
06h (12050Ch)	**REG12050C**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGDMA_END[7:0]	7:0	END address for REGDMA mode.	
06h (12050Dh)	**REG12050D**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGDMA_STR[6:0]	7:1	Start Base address for REGDMA mode. Start address = REGDMA_STR<<9;	
	REGDMA_END[8]	0	See description of '12050Ch'.	
07h (12050Eh)	**REG12050E**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGDMA_STR[14:7]	7:0	See description of '12050Dh'.	
07h (12050Fh)	**REG12050F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	REGDMA_STR[18:15]	3:0	See description of '12050Dh'.	
08h (120510h)	**REG120510**	**7:0**	**Default : 0xBF**	**Access : R/W**
	-	7:5	Reserved.	
	DUMMY0_INT_MASK	4	Dummy0 interrupt mask.	
	FLD_INT_MASK	3	Fld interrupt mask.	
	REGDMA_ERR_INT_MASK	2	REGDMA error interrupt mask.	
	VS1_INT_MASK	1	VS1 interrupt mask.	
	VS0_INT_MASK	0	VS0 interrupt mask.	
08h (120511h)	**REG120511**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	FLD	6	Field info.	
	-	5:4	Reserved.	
	FLD_ERR_INT	3	Field interrupt.	
	-	2	Reserved.	

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VS1_INT	1	VS1 interrupt flag.	
	VS0_INT	0	VS0 interrupt flag.	
09h (120512h)	**REG120512**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	RDMA_STATE[2:0]	2:0	RDMA state. 0: REGDMA_STR. 1: REGDMA_SEND0. 2: REGDMA_SEND1. 4: WAIT_RDMA_GO. 6: WAIT_MIU_ACK. 7: DMA_IDLE.	
09h (120513h)	**REG120513**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	LB0_BIST_FAIL	6	LB0 BIST.	
	PSRAM_BIST_FAIL	5	PSRAM BIST.	
	GW_FF_BIST_FAIL	4	Buffer BIST.	
	LB_UF	3	Line buffer underflow.	
	LB_OF	2	Line buffer overflow.	
	GW_UF	1	Buffer underflow.	
	GW_OF	0	Buffer overflow.	
0Ah (120514h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Bh (120516h)	**REG120516**	**7:0**	**Default : 0x00**	**Access : R/W**
	THREE_D_MIDDLE_OFFSET_Q[7:0]	7:0	Garbage line num in top bottom mode. (offset shoud be set to 0 on ip).	
0Bh (120517h)	**REG120517**	**7:0**	**Default : 0x00**	**Access : R/W**
	RDMA_FF_CMPRS_EN_Q[1:0]	7:6	Enable rdma ff compress. 00: Compress mode off. 01: Transparent mode. 10: Uni color mode. 11: Both transparent/ uni color mode.	
	HANDSHAKE_MODE_Q	5	Enable hand-shaking valid bit =1.	
	THREE_D_PIX_INI_Q[4:0]	4:0	Set initial start pix in side by side mode.	
0Ch (120518h)	**REG120518**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_PIX_NUM_Q[7:0]	7:0	Set output valid bit num in one line.	

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (120519h)	**REG120519**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_PIX_NUM_Q[11:8]	3:0	See description of '120518h'.	
0Dh (12051Ah)	**REG12051A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_LINE_NUM_Q[7:0]	7:0	Set output valid line num in one frame.	
0Dh (12051Bh)	**REG12051B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_LINE_NUM_Q[11:8]	3:0	See description of '12051Ah'.	
0Eh (12051Ch)	**REG12051C**	**7:0**	**Default : 0x69**	**Access : R/W**
	RDMA_HT[7:0]	7:0	RDMA H total (unit: 2 pixels) > reg_strch_size.	
0Eh (12051Dh)	**REG12051D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	RDMA_HT[10:8]	2:0	See description of '12051Ch'.	
0Fh (12051Eh)	**REG12051E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PIPE_Q[7:0]	7:0	Hsync input pipe delay.	
0Fh (12051Fh)	**REG12051F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HS_PIPE_Q[9:8]	1:0	See description of '12051Eh'.	
10h (120520h)	**REG120520**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SLOW_RATIO[5:0]	5:0	FIFO read out slow ratio.	
10h (120521h)	**REG120521**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SLOW_THD[6:0]	6:0	FIFO out speed slow down when data counts <= SLOW_THD.	
11h (120522h)	**REG120522**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_Q[7:0]	7:0	Brightness value: -256~255. Use 2's complement.	
11h (120523h)	**REG120523**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	CON_YG_Q[5:0]	6:1	Y Contrast gain. Gain = REG_CON / 16.	
	BRI_Q[8]	0	See description of '120522h'.	

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (120524h)	**REG120524**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_UB_Q[5:0]	5:0	U Contrast gain. Gain = REG_CON / 16.	
12h (120525h)	**REG120525**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_VR_Q[5:0]	5:0	V Contrast gain. Gain = REG_CON / 16.	
19h (120532h)	**REG120532**	**7:0**	**Default : 0xF0**	**Access : R/W**
	DMA_THD[7:0]	7:0	DMA FIFO threshold.	
19h (120533h)	**REG120533**	**7:0**	**Default : 0x42**	**Access : R/W**
	GW_HI_TSH[1:0]	7:6	DMA access high priority.	
	-	5	Reserved.	
	DMA_EXT[4:0]	4:0	DMA Burst length new mode: DMA_EXT [4:0]. 0: FF depth - current level. (equal the "burst all" in old mode). 31: 255. else: 8*DMA_EXT.	
1Ch (120538h)	**REG120538**	**7:0**	**Default : 0x7D**	**Access : R/W**
	-	7	Reserved.	
	DMA_BURST_LEVEL[6:0]	6:0	Target level of rdma ff each time into burst state, valid level : h0~h7d(0~125).	
1Ch (120539h)	**REG120539**	**7:0**	**Default : 0x00**	**Access : R/W**
	LB_COUPLE_EN	7	Couple RDMA ff with strch ff when strch_V off.	
	-	6:0	Reserved.	
1Dh (12053Ah)	**REG12053A**	**7:0**	**Default : 0x20**	**Access : R/W**
	ACCURATE_HI_TSH_EN	7	DMA access high priority : accurate mode enable.	
	ACCURATE_GW_HI_TSH[6:0]	6:0	DMA access high priority level (unit : 1/128 FF depth).	
1Eh (12053Ch)	**REG12053C**	**7:0**	**Default : 0x20**	**Access : R/W**
	THREE_D_MIDDLE_Q[7:0]	7:0	Set three d middle.	
1Eh (12053Dh)	**REG12053D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	THREE_D_MIDDLE_Q[11:8]	3:0	See description of '12053Ch'.	
20h	**REG120540**	**7:0**	**Default : 0x10**	**Access : R/W**

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120540h)	-	7:6	Reserved.	
	PRI1_Q[1:0]	5:4	2nd priority GWIN number.	
	-	3:2	Reserved.	
	PRI0_Q[1:0]	1:0	1st priority GWIN number.	
22h ~ 23h (120544h ~ 120547h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
24h (120548h)	**REG120548**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[7:0]	7:0	Transparent color key {R[7:0], G[7:0], B[7:0]}: for RGB source.	
24h (120549h)	**REG120549**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[15:8]	7:0	See description of '120548h'.	
25h (12054Ah)	**REG12054A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[23:16]	7:0	See description of '120548h'.	
26h (12054Ch)	**REG12054C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[7:0]	7:0	Transparent color key {V[7:0], Y[7:0], U[7:0]}: for YUV source.	
26h (12054Dh)	**REG12054D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[15:8]	7:0	See description of '12054Ch'.	
27h (12054Eh)	**REG12054E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[23:16]	7:0	See description of '12054Ch'.	
28h (120550h)	**REG120550**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	THREE_D_MODE_Q[2:0]	3:1	3D OSD mode: 0: Off. 1: L/R swith by frame. 2: L/R side by side. 3: L/R top - bottom. 4: L/R line alternative.	
	3D_FLAG_INV_Q	0	Input 3D flag L/R inverse.	
28h (120551h)	**REG120551**	**7:0**	**Default : 0x00**	**Access : R/W**
	YC_SWAP_Q	7	Switch Y/C when dtype is UV8Y8.	
	UV_SWAP_Q	6	Switch U/V (R/B).	
	-	5:0	Reserved.	

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Eh ~ 2Fh (12055Ch ~ 12055Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (120560h)	**REG120560**	**7:0**	**Default : 0x68**	**Access : R/W**
	STRCH_HSIZE_Q[7:0]	7:0	Stretch Window H size (unit: 2 pixel). When V stretch ratio=1, hsize has no size limit. When V stretch ratio !=1, the max hsize is limited by line buffer size.	
30h (120561h)	**REG120561**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	STRCH_HSIZE_Q[10:8]	2:0	See description of '120560h'.	
31h (120562h)	**REG120562**	**7:0**	**Default : 0x40**	**Access : R/W**
	STRCH_VSIZE_Q[7:0]	7:0	Stretch Window V size.	
31h (120563h)	**REG120563**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VSIZE_Q[11:8]	3:0	See description of '120562h'.	
32h (120564h)	**REG120564**	**7:0**	**Default : 0x64**	**Access : R/W**
	STRCH_HST_Q[7:0]	7:0	Stretch Window H coordinate.	
32h (120565h)	**REG120565**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	STRCH_HST_Q[12:8]	4:0	See description of '120564h'.	
34h (120568h)	**REG120568**	**7:0**	**Default : 0x00**	**Access : R/W**
	STRCH_VST_Q[7:0]	7:0	Stretch Window V coordinate.	
34h (120569h)	**REG120569**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VST_Q[11:8]	3:0	See description of '120568h'.	
35h (12056Ah)	**REG12056A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSTRCH_Q[7:0]	7:0	Stretch H ratio. = In/Out* 2^12.	
35h (12056Bh)	**REG12056B**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	HSTRCH_Q[12:8]	4:0	See description of '12056Ah'.	
36h	**REG12056C**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(12056Ch)	VSTRCH_Q[7:0]	7:0	Stretch V ratio.	
36h (12056Dh)	**REG12056D**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	VSTRCH_Q[12:8]	4:0	See description of '12056Ch'.	
38h (120570h)	**REG120570**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSTRCH_INI_Q[7:0]	7:0	Stretch H start value.	
38h (120571h)	**REG120571**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HSTRCH_INI_Q[12:8]	4:0	See description of '120570h'.	
39h (120572h)	**REG120572**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTRCH_INI_Q[7:0]	7:0	Stretch V start value.	
39h (120573h)	**REG120573**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VSTRCH_INI_Q[12:8]	4:0	See description of '120572h'.	
3Ah (120574h)	**REG120574**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TRS_STRCH	4	0: Transparent color only duplicate if stretch. 1: Stretch transparent color like normal color.	
	VSTRCH_MD[1:0]	3:2	V-stretch mode. 0: Linear. 1: Duplicate. 2: Nearest.	
	HSTRCH_MD[1:0]	1:0	H-stretch mode. 0: 6-tap (including nearest). 1: Duplicate.	
3Bh (120576h)	**REG120576**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	DYNAMIC_GATING_EN_Q	5	Enable dynamic gating.	
	-	4	Reserved.	
	OLD_ADDR	3	0: GOP DMA use new address. 1: GOP DMA use old address.	
	MIU_REQ_DISABLE	2	0: Normal gop to miu access. 1: Disable gop to miu access.	
	-	1:0	Reserved.	

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GOPG1_0 Register (Bank = 1205)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Bh (120577h)	**REG120577**	**7:0**	**Default : 0x80**	**Access : R/W**
	MIUREQ_HOLD_CYCLE_Q[3:0]	7:4	Compress mode turn on, set miu req hold time. base: 4. - >holdtime = miureq_hold_cycle x 4 x (cmpress rate).	
	-	3:0	Reserved.	
3Ch (120578h)	**REG120578**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CMQ_VS0_INT_MASK	5	CMQ VS0 interrupt mask.	
	-	4	Reserved.	
	MASK_1ST_HS_EVEN_Q	3	Mask 1st hsync in even field for GOP_VE.	
	MASK_1ST_HS_ODD_Q	2	Mask 1st hsync in odd field for GOP_VE.	
	-	1:0	Reserved.	
78h (1205F0h)	**REG1205F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	REGDMA_ONESHOT	1	REGDMA write only in one frame start.	
	REGDMA_EN	0	REGDMA write mode enable.	
78h (1205F1h)	**REG1205F1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	REGDMA_ACK	0	REGDMA DONE ACK. sequence: 1: {REGDMA_oneshot, REG_REGDMA_EN}=2'b11. 2: Wait REGDMA_ACK. 3: Clear REG_REGDMA_EN.	

GOPG1_1 Register (Bank = 1206)

GOPG1_1 Register (Bank = 1206)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**REG120600**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG1_1 Register (Bank = 1206)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120600h)	GWIN0_DTYPE_Q[3:0]	7:4	GWIN0 Source Data Type. 0: RGB1555/Blink. 1: RGB565. 2: ARGB4444. 3: 2266. 4. 8bit palette. 5: ARGB8888. 6: ARGB1555. 7.ABGR8888. 8: RGB1555/UV7Y8. 9: UV8Y8. 10.RGBA5551. 11.RGBA4444.	
	-	3:1	Reserved.	
	GWIN0_EN	0	Graphic window 0 Enable.	
00h (120601h)	**REG120601**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_TILE_16BPP_Q	7	16bpp Tile mode format. 0: Linear. 1: Tile mode.	
	GWIN0_ALPHA_EN_Q	6	GWIN0 alpha_enable. 1: Pixel alpha. 0: Constant alpha.	
	-	5:0	Reserved.	
01h (120602h)	**REG120602**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, unit 1 word.	
01h (120603h)	**REG120603**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[15:8]	7:0	See description of '120602h'.	
02h (120604h)	**REG120604**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[23:16]	7:0	See description of '120602h'.	
02h (120605h)	**REG120605**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_Q[27:24]	3:0	See description of '120602h'.	
03h (120606h)	**REG120606**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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GOPG1_1 Register (Bank = 1206)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DEL_HSTR_PIX0_Q[4:0]	4:0	Delete pixel number at hstart for pixel alignment unit:1 pixel.	
03h (120607h)	**REG120607**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HEND_PIX0_Q[4:0]	4:0	Delete pixel number at hend for pixel alignment unit:1 pixel.	
04h (120608h)	**REG120608**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_HSTR_Q[7:0]	7:0	The horizontal start pixel of Display Image for GWIN0. Unit: 1 word pixels.	
04h (120609h)	**REG120609**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HSTR_Q[10:8]	2:0	See description of '120608h'.	
05h (12060Ah)	**REG12060A**	**7:0**	**Default : 0x01**	**Access : R/W**
	GWIN0_HEND_Q[7:0]	7:0	The horizontal end pixel of Display Image for GWIN0. Unit: 1 word pixels.	
05h (12060Bh)	**REG12060B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HEND_Q[10:8]	2:0	See description of '12060Ah'.	
06h (12060Ch)	**REG12060C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VSTR_Q[7:0]	7:0	The vertical start line of Display Image for GWIN0. Unit: 1 line.	
06h (12060Dh)	**REG12060D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VSTR_Q[11:8]	3:0	See description of '12060Ch'.	
08h (120610h)	**REG120610**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VEND_Q[7:0]	7:0	The vertical end line of Display Image for GWIN0. Unit: 1 line.	
08h (120611h)	**REG120611**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VEND_Q[11:8]	3:0	See description of '120610h'.	
09h (120612h)	**REG120612**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK0_HSIZE_Q[7:0]	7:0	Ring Block0 line size.	
09h (120613h)	**REG120613**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

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GOPG1_1 Register (Bank = 1206)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RBLK0_HSIZE_Q[10:8]	2:0	See description of '120612h'.	
0Ah (120614h)	**REG120614**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_ALPHA_Q[7:0]	7:0	GWIN0 constant alpha.	
0Ch (120618h)	**REG120618**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[7:0]	7:0	GWIN0 1st data offset address after REG_DRAM_RBLK0_STR, unit: 1 word.	
0Ch (120619h)	**REG120619**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[15:8]	7:0	See description of '120618h'.	
0Dh (12061Ah)	**REG12061A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[23:16]	7:0	See description of '120618h'.	
0Dh (12061Bh)	**REG12061B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN0_VSTR_Q[27:24]	3:0	See description of '120618h'.	
16h (12062Ch)	**REG12062C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GWIN0_FADE_INC_Q	6	FADE IN/OUT. 1: Stronger. 0: Weaker.	
	GWIN0_FADE_INI_Q	5	FADE Initial.	
	GWIN0_FADE_EN_Q	4	FADE enable.	
	GWIN0_FADE_RATE_Q[3:0]	3:0	FADE frame Rate for GWIN0.	
16h (12062Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Eh (12063Ch)	**REG12063C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, 3D L/R mode unit 1 word.	
1Eh (12063Dh)	**REG12063D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[15:8]	7:0	See description of '12063Ch'.	
1Fh (12063Eh)	**REG12063E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[23:16]	7:0	See description of '12063Ch'.	
1Fh (12063Fh)	**REG12063F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_LR_Q[27:24]	3:0	See description of '12063Ch'.	
20h	**REG120640**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG1_1 Register (Bank = 1206)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120640h)	GWIN1_DTYPE_Q[3:0]	7:4	GWIN1 Source Data Type.	
	-	3:1	Reserved.	
	GWIN1_EN	0	Graphic window 1 Enable.	
20h (120641h)	**REG120641**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_TILE_16BPP_Q	7	16bpp Tile mode format.	
	GWIN1_ALPHA_EN_Q	6	GWIN1 alpha_enable. 1: Pixel alpha. 0: Constant alpha.	
	-	5:0	Reserved.	
21h (120642h)	**REG120642**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_Q[7:0]	7:0	Ring Block start address in dram for GWIN1 read out, unit 1 word.	
21h (120643h)	**REG120643**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_Q[15:8]	7:0	See description of '120642h'.	
22h (120644h)	**REG120644**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_Q[23:16]	7:0	See description of '120642h'.	
22h (120645h)	**REG120645**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK1_STR_Q[27:24]	3:0	See description of '120642h'.	
23h (120646h)	**REG120646**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HSTR_PIX1_Q[4:0]	4:0	Delete pixel number at hstart for pixel alignment unit:1 pixel.	
23h (120647h)	**REG120647**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HEND_PIX1_Q[4:0]	4:0	Delete pixel number at hend for pixel alignment unit:1 pixel.	
24h (120648h)	**REG120648**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_HSTR_Q[7:0]	7:0	The horizontal start pixel of Display Image for GWIN1. Unit: 1 word pixels.	
24h (120649h)	**REG120649**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN1_HSTR_Q[10:8]	2:0	See description of '120648h'.	
25h	**REG12064A**	**7:0**	**Default : 0x01**	**Access : R/W**

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GOPG1_1 Register (Bank = 1206)

Index (Absolute)	Mnemonic	Bit	Description	
(12064Ah)	GWIN1_HEND_Q[7:0]	7:0	The horizontal end pixel of Display Image for GWIN1. Unit: 1 word pixels.	
25h (12064Bh)	**REG12064B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN1_HEND_Q[10:8]	2:0	See description of '12064Ah'.	
26h (12064Ch)	**REG12064C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_VSTR_Q[7:0]	7:0	The vertical start line of Display Image for GWIN1 unit: 1 line.	
26h (12064Dh)	**REG12064D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN1_VSTR_Q[11:8]	3:0	See description of '12064Ch'.	
28h (120650h)	**REG120650**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_VEND_Q[7:0]	7:0	The vertical end line of Display Image for GWIN1 Unit: 1 line.	
28h (120651h)	**REG120651**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN1_VEND_Q[11:8]	3:0	See description of '120650h'.	
29h (120652h)	**REG120652**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK1_HSIZE_Q[7:0]	7:0	Ring Block1 line size.	
29h (120653h)	**REG120653**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RBLK1_HSIZE_Q[10:8]	2:0	See description of '120652h'.	
2Ah (120654h)	**REG120654**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_ALPHA_Q[7:0]	7:0	GWIN1 constant alpha.	
2Ch (120658h)	**REG120658**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_VSTR_Q[7:0]	7:0	GWIN1 1st data offset address after. REG_DRAM_RBLK1_STR, unit: 1 word.	
2Ch (120659h)	**REG120659**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_VSTR_Q[15:8]	7:0	See description of '120658h'.	
2Dh (12065Ah)	**REG12065A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN1_VSTR_Q[23:16]	7:0	See description of '120658h'.	
2Dh (12065Bh)	**REG12065B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN1_VSTR_Q[27:24]	3:0	See description of '120658h'.	

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GOPG1_1 Register (Bank = 1206)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (12066Ch)	**REG12066C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GWIN1_FADE_INC_Q	6	FADE IN/OUT. 1: Stronger. 0: Weaker.	
	GWIN1_FADE_INI_Q	5	FADE Initial.	
	GWIN1_FADE_EN_Q	4	FADE enable.	
	GWIN1_FADE_RATE_Q[3:0]	3:0	FADE frame Rate for GWIN1.	
3Eh (12067Ch)	**REG12067C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_LR_Q[7:0]	7:0	Ring Block start address in dram for GWIN1 read out, 3D L/R mode unit 1 word.	
3Eh (12067Dh)	**REG12067D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_LR_Q[15:8]	7:0	See description of '12067Ch'.	
3Fh (12067Eh)	**REG12067E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR_LR_Q[23:16]	7:0	See description of '12067Ch'.	
3Fh (12067Fh)	**REG12067F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK1_STR_LR_Q[27:24]	3:0	See description of '12067Ch'.	

GOPG2_0 Register (Bank = 1208)

GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (120800h)	**REG120800**	**7:0**	**Default : 0x09**	**Access : R/W**
	5541_EN	7	RGB5541 alpha mask mode enable, only for RGB1555 Data type.	
	-	6	Reserved.	
	YUV_TRS_EN	5	YUV Transparent color enable.	
	GWIN_FLD_INV	4	Input Field inverse.	
	GWIN_PROG_MD	3	GWINs display mode. 0: Interlace. 1: Progress.	
	GWIN_HS_INV	2	Input Hsync inverse.	

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GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GWIN_VS_INV	1	Input Vsync inverse.	
	GWIN_RST	0	GOP soft reset.	
00h (120801h)	**REG120801**	**7:0**	**Default : 0x40**	**Access : R/W**
	ALPHA_INV	7	Alpha out inverse.	
	HS_MASK	6	1: Mask Hsync when VFDE is low. 0: No mask.	
	DISP_VBACK	5	V line read out direction. 0: Down. 1: Up.	
	DISP_HBACK	4	H pixel read out direction. 0: Forward. 1: Back.	
	RGB_TRS_EN	3	RGB Transparent color enable.	
	GWIN_YUVOUT	2	GOP out format. 0: RGB. 1: VYU.	
	-	1	Reserved.	
	OUT_RDY	0	Output ready.	
01h (120802h)	**REG120802**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_PINPON_DWIN	7	GWIN1 PINPON mode (with DWIN).	
	-	6:3	Reserved.	
	GWIN_DEST[2:0]	2:0	GOP destination. 0: SC0_IP_MAIN. 1: SC0_IP_SUB. 2: SC0_OP. 3: MVOP. 4: SC1_IP_MAIN. 5: SC1_OP. 6: SC2_OP. 7: DIP.	
08h (120810h)	**REG120810**	**7:0**	**Default : 0xBB**	**Access : R/W**
	-	7:5	Reserved.	
	DUMMY0_INT_MASK	4	Dummy0 interrupt mask.	
	FLD_INT_MASK	3	Fld interrupt mask.	
	-	2	Reserved.	
	VS1_INT_MASK	1	VS1 interrupt mask.	

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GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VS0_INT_MASK	0	VS0 interrupt mask.	
08h (120811h)	**REG120811**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	FLD	6	Field info.	
	-	5:4	Reserved.	
	FLD_ERR_INT	3	Field interrupt.	
	-	2	Reserved.	
	VS1_INT	1	VS1 interrupt flag.	
	VS0_INT	0	VS0 interrupt flag.	
09h (120812h)	**REG120812**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	RDMA_STATE[2:0]	2:0	RDMA state. 0: REGDMA_STR. 1: REGDMA_SEND0. 2: REGDMA_SEND1. 4: WAIT_RDMA_GO. 6: WAIT_MIU_ACK. 7: DMA_IDLE.	
09h (120813h)	**REG120813**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	LB0_BIST_FAIL	6	LB0 BIST.	
	PSRAM_BIST_FAIL	5	PSRAM BIST.	
	GW_FF_BIST_FAIL	4	Buffer BIST.	
	LB_UF	3	Line buffer underflow.	
	LB_OF	2	Line buffer overflow.	
	GW_UF	1	Buffer underflow.	
	GW_OF	0	Buffer overflow.	
0Bh (120816h)	**REG120816**	**7:0**	**Default : 0x00**	**Access : R/W**
	THREE_D_MIDDLE_OFFSET_Q[7:0]	7:0	Garbage line num in top bottom mode. (offset shoud be set to 0 on ip).	
0Bh	**REG120817**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG2_0 Register (Bank = 1208)

Index (Absolute)	Mnemonic	Bit	Description	
(120817h)	RDMA_FF_CMPRS_EN_Q[1:0]	7:6	Enable rdma ff compress. 00: Compress mode off. 01: Transparent mode. 10: Uni color mode. 11: Both transparent/ uni color mode.	
	HANDSHAKE_MODE_Q	5	Enable hand-shaking valid bit =1.	
	THREE_D_PIX_INI_Q[4:0]	4:0	Set initial start pix in side by side mode.	
0Ch (120818h)	**REG120818**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_PIX_NUM_Q[7:0]	7:0	Set output valid bit num in one line.	
0Ch (120819h)	**REG120819**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_PIX_NUM_Q[11:8]	3:0	See description of '120818h'.	
0Dh (12081Ah)	**REG12081A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_LINE_NUM_Q[7:0]	7:0	Set output valid line num in one frame.	
0Dh (12081Bh)	**REG12081B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_LINE_NUM_Q[11:8]	3:0	See description of '12081Ah'.	
0Eh (12081Ch)	**REG12081C**	**7:0**	**Default : 0x69**	**Access : R/W**
	RDMA_HT[7:0]	7:0	RDMA H total (unit: 2 pixels) > reg_strch_size.	
0Eh (12081Dh)	**REG12081D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	RDMA_HT[10:8]	2:0	See description of '12081Ch'.	
0Fh (12081Eh)	**REG12081E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PIPE_Q[7:0]	7:0	Hsync input pipe delay.	
0Fh (12081Fh)	**REG12081F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HS_PIPE_Q[9:8]	1:0	See description of '12081Eh'.	
10h (120820h)	**REG120820**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SLOW_RATIO[5:0]	5:0	FIFO read out slow ratio.	
10h (120821h)	**REG120821**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SLOW_THD[6:0]	6:0	FIFO out speed slow down when data counts <= SLOW_THD.	

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GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (120822h)	**REG120822**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_Q[7:0]	7:0	Brightness value: -256~255. Use 2's complement.	
11h (120823h)	**REG120823**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	CON_YG_Q[5:0]	6:1	Y Contrast gain. Gain = REG_CON / 16.	
	BRI_Q[8]	0	See description of '120822h'.	
12h (120824h)	**REG120824**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_UB_Q[5:0]	5:0	U Contrast gain. Gain = REG_CON / 16.	
12h (120825h)	**REG120825**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_VR_Q[5:0]	5:0	V Contrast gain. Gain = REG_CON / 16.	
19h (120832h)	**REG120832**	**7:0**	**Default : 0xF0**	**Access : R/W**
	DMA_THD[7:0]	7:0	DMA FIFO threshold.	
19h (120833h)	**REG120833**	**7:0**	**Default : 0x42**	**Access : R/W**
	GW_HI_TSH[1:0]	7:6	DMA access high priority.	
	-	5	Reserved.	
	DMA_EXT[4:0]	4:0	DMA Burst length new mode: DMA_EXT [4:0]. 0: FF depth - current level. (equal the "burst all" in old mode). 31: 255. else: 8*DMA_EXT.	
1Ch (120838h)	**REG120838**	**7:0**	**Default : 0x7D**	**Access : R/W**
	-	7	Reserved.	
	DMA_BURST_LEVEL[6:0]	6:0	Target level of rdma ff each time into burst state, valid level : h0~h7d(0~125).	
1Ch (120839h)	**REG120839**	**7:0**	**Default : 0x00**	**Access : R/W**
	LB_COUPLE_EN	7	Couple RDMA ff with strch ff when strch_V off.	
	-	6:0	Reserved.	
1Dh	**REG12083A**	**7:0**	**Default : 0x20**	**Access : R/W**

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GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(12083Ah)	ACCURATE_HI_TSH_EN	7	DMA access high priority : accurate mode enable.	
	ACCURATE_GW_HI_TSH[6:0]	6:0	DMA access high priority level (unit : 1/128 FF depth).	
1Eh (12083Ch)	**REG12083C**	**7:0**	**Default : 0x20**	**Access : R/W**
	THREE_D_MIDDLE_Q[7:0]	7:0	Set three d middle.	
1Eh (12083Dh)	**REG12083D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	THREE_D_MIDDLE_Q[11:8]	3:0	See description of '12083Ch'.	
20h (120840h)	**REG120840**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRI0_Q[1:0]	1:0	1st priority GWIN number.	
24h (120848h)	**REG120848**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[7:0]	7:0	Transparent color key {R[7:0], G[7:0], B[7:0]}: for RGB source.	
24h (120849h)	**REG120849**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[15:8]	7:0	See description of '120848h'.	
25h (12084Ah)	**REG12084A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[23:16]	7:0	See description of '120848h'.	
26h (12084Ch)	**REG12084C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[7:0]	7:0	Transparent color key {V[7:0], Y[7:0], U[7:0]}: for YUV source.	
26h (12084Dh)	**REG12084D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[15:8]	7:0	See description of '12084Ch'.	
27h (12084Eh)	**REG12084E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[23:16]	7:0	See description of '12084Ch'.	
28h (120850h)	**REG120850**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	THREE_D_MODE_Q[2:0]	3:1	3D OSD mode: 0: Off. 1: L/R swith by frame. 2: L/R side by side. 3: L/R top - bottom. 4: L/R line alternative.	
	3D_FLAG_INV_Q	0	Input 3D flag L/R inverse.	
28h	**REG120851**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120851h)	YC_SWAP_Q	7	Switch Y/C when dtype is UV8Y8.	
	UV_SWAP_Q	6	Switch U/V (R/B).	
	-	5:0	Reserved.	
30h (120860h)	**REG120860**	**7:0**	**Default : 0x68**	**Access : R/W**
	STRCH_HSIZE_Q[7:0]	7:0	Stretch Window H size (unit: 2 pixel). When V stretch ratio=1, hsize has no size limit. When V stretch ratio !=1, the max hsize is limited by line buffer size.	
30h (120861h)	**REG120861**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	STRCH_HSIZE_Q[10:8]	2:0	See description of '120860h'.	
31h (120862h)	**REG120862**	**7:0**	**Default : 0x40**	**Access : R/W**
	STRCH_VSIZE_Q[7:0]	7:0	Stretch Window V size.	
31h (120863h)	**REG120863**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VSIZE_Q[11:8]	3:0	See description of '120862h'.	
32h (120864h)	**REG120864**	**7:0**	**Default : 0x64**	**Access : R/W**
	STRCH_HST_Q[7:0]	7:0	Stretch Window H coordinate.	
32h (120865h)	**REG120865**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	STRCH_HST_Q[12:8]	4:0	See description of '120864h'.	
34h (120868h)	**REG120868**	**7:0**	**Default : 0x00**	**Access : R/W**
	STRCH_VST_Q[7:0]	7:0	Stretch Window V coordinate.	
34h (120869h)	**REG120869**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VST_Q[11:8]	3:0	See description of '120868h'.	
35h (12086Ah)	**REG12086A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSTRCH_Q[7:0]	7:0	Stretch H ratio. = In/Out* 2^12.	
35h (12086Bh)	**REG12086B**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	HSTRCH_Q[12:8]	4:0	See description of '12086Ah'.	
36h (12086Ch)	**REG12086C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTRCH_Q[7:0]	7:0	Stretch V ratio.	

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GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (12086Dh)	**REG12086D**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	VSTRCH_Q[12:8]	4:0	See description of '12086Ch'.	
38h (120870h)	**REG120870**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSTRCH_INI_Q[7:0]	7:0	Stretch H start value.	
38h (120871h)	**REG120871**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HSTRCH_INI_Q[12:8]	4:0	See description of '120870h'.	
39h (120872h)	**REG120872**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTRCH_INI_Q[7:0]	7:0	Stretch V start value.	
39h (120873h)	**REG120873**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VSTRCH_INI_Q[12:8]	4:0	See description of '120872h'.	
3Ah (120874h)	**REG120874**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TRS_STRCH	4	0: Transparent color only duplicate if stretch. 1: Stretch transparent color like normal color.	
	VSTRCH_MD[1:0]	3:2	V-stretch mode. 0: Linear. 1: Duplicate. 2: Nearest.	
	HSTRCH_MD[1:0]	1:0	H-stretch mode. 0: 6-tap (including nearest). 1: Duplicate.	
3Bh (120876h)	**REG120876**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	DYNAMIC_GATING_EN_Q	5	Enable dynamic gating.	
	-	4	Reserved.	
	OLD_ADDR	3	0: GOP DMA use new address. 1: GOP DMA use old address.	
	MIU_REQ_DISABLE	2	0: Normal gop to miu access. 1: Disable gop to miu access.	
	-	1:0	Reserved.	
3Bh	**REG120877**	**7:0**	**Default : 0x80**	**Access : R/W**

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GOPG2_0 Register (Bank = 1208)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120877h)	MIUREQ_HOLD_CYCLE_Q[3:0]	7:4	Compress mode turn on, set miu req hold time. base: 4. - >holdtime = miureq_hold_cycle x 4 x (cmpress rate).	
	-	3:0	Reserved.	
3Ch (120878h)	**REG120878**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CMQ_VS0_INT_MASK	5	CMQ VS0 interrupt mask.	
	-	4	Reserved.	
	MASK_1ST_HS_EVEN_Q	3	Mask 1st hsync in even field for GOP_VE.	
	MASK_1ST_HS_ODD_Q	2	Mask 1st hsync in odd field for GOP_VE.	
	-	1:0	Reserved.	

GOPG2_1 Register (Bank = 1209)

GOPG2_1 Register (Bank = 1209)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (120900h)	**REG120900**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_DTYPE_Q[3:0]	7:4	GWIN0 Source Data Type. 0: RGB1555/Blink. 1: RGB565. 2: ARGB4444. 3: 2266. 4. 8bit palette. 5: ARGB8888. 6: ARGB1555. 7.ABGR8888. 8: RGB1555/UV7Y8. 9: UV8Y8. 10.RGBA5551. 11.RGBA4444.	
	-	3:1	Reserved.	
	GWIN0_EN	0	Graphic window 0 Enable.	
00h	**REG120901**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG2_1 Register (Bank = 1209)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120901h)	GWIN0_TILE_16BPP_Q	7	16bpp Tile mode format. 0: Linear. 1: Tile mode.	
	GWIN0_ALPHA_EN_Q	6	GWIN0 alpha_enable. 1: Pixel alpha. 0: Constant alpha.	
	-	5:0	Reserved.	
01h (120902h)	**REG120902**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, unit 1 word.	
01h (120903h)	**REG120903**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[15:8]	7:0	See description of '120902h'.	
02h (120904h)	**REG120904**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[23:16]	7:0	See description of '120902h'.	
02h (120905h)	**REG120905**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_Q[27:24]	3:0	See description of '120902h'.	
03h (120906h)	**REG120906**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HSTR_PIX0_Q[4:0]	4:0	Delete pixel number at hstart for pixel alignment unit:1 pixel.	
03h (120907h)	**REG120907**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HEND_PIX0_Q[4:0]	4:0	Delete pixel number at hend for pixel alignment unit:1 pixel.	
04h (120908h)	**REG120908**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_HSTR_Q[7:0]	7:0	The horizontal start pixel of Display Image for GWIN0. Unit: 1 word pixels.	
04h (120909h)	**REG120909**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HSTR_Q[10:8]	2:0	See description of '120908h'.	
05h (12090Ah)	**REG12090A**	**7:0**	**Default : 0x01**	**Access : R/W**
	GWIN0_HEND_Q[7:0]	7:0	The horizontal end pixel of Display Image for GWIN0. Unit: 1 word pixels.	

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GOPG2_1 Register (Bank = 1209)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (12090Bh)	**REG12090B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HEND_Q[10:8]	2:0	See description of '12090Ah'.	
06h (12090Ch)	**REG12090C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VSTR_Q[7:0]	7:0	The vertical start line of Display Image for GWIN0. Unit: 1 line.	
06h (12090Dh)	**REG12090D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VSTR_Q[11:8]	3:0	See description of '12090Ch'.	
08h (120910h)	**REG120910**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VEND_Q[7:0]	7:0	The vertical end line of Display Image for GWIN0. Unit: 1 line.	
08h (120911h)	**REG120911**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VEND_Q[11:8]	3:0	See description of '120910h'.	
09h (120912h)	**REG120912**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK0_HSIZE_Q[7:0]	7:0	Ring Block0 line size.	
09h (120913h)	**REG120913**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RBLK0_HSIZE_Q[10:8]	2:0	See description of '120912h'.	
0Ah (120914h)	**REG120914**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_ALPHA_Q[7:0]	7:0	GWIN0 constant alpha.	
0Ch (120918h)	**REG120918**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[7:0]	7:0	GWIN0 1st data offset address after REG_DRAM_RBLK0_STR, unit: 1 word.	
0Ch (120919h)	**REG120919**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[15:8]	7:0	See description of '120918h'.	
0Dh (12091Ah)	**REG12091A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[23:16]	7:0	See description of '120918h'.	
0Dh (12091Bh)	**REG12091B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN0_VSTR_Q[27:24]	3:0	See description of '120918h'.	
16h	**REG12092C**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG2_1 Register (Bank = 1209)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(12092Ch)	-	7	Reserved.	
	GWIN0_FADE_INC_Q	6	FADE IN/OUT. 1: Stronger. 0: Weaker.	
	GWIN0_FADE_INI_Q	5	FADE Initial.	
	GWIN0_FADE_EN_Q	4	FADE enable.	
	GWIN0_FADE_RATE_Q[3:0]	3:0	FADE frame Rate for GWIN0.	
1Eh (12093Ch)	**REG12093C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, 3D L/R mode unit 1 word.	
1Eh (12093Dh)	**REG12093D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[15:8]	7:0	See description of '12093Ch'.	
1Fh (12093Eh)	**REG12093E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[23:16]	7:0	See description of '12093Ch'.	
1Fh (12093Fh)	**REG12093F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_LR_Q[27:24]	3:0	See description of '12093Ch'.	

GOPG3_0 Register (Bank = 120B)

GOPG3_0 Register (Bank = 120B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (120B00h)	**REG120B00**	**7:0**	**Default : 0x09**	**Access : R/W**
	5541_EN	7	RGB5541 alpha mask mode enable, only for RGB1555 Data type.	
	-	6	Reserved.	
	YUV_TRS_EN	5	YUV Transparent color enable.	
	GWIN_FLD_INV	4	Input Field inverse.	
	GWIN_PROG_MD	3	GWINs display mode. 0: Interlace. 1: Progress.	
	GWIN_HS_INV	2	Input Hsync inverse.	
	GWIN_VS_INV	1	Input Vsync inverse.	

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GOPG3_0 Register (Bank = 120B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GWIN_RST	0	GOP soft reset.	
00h (120B01h)	**REG120B01**	**7:0**	**Default : 0x40**	**Access : R/W**
	ALPHA_INV	7	Alpha out inverse.	
	HS_MASK	6	1: Mask Hsync when VFDE is low. 0: No mask.	
	DISP_VBACK	5	V line read out direction. 0: Down. 1: Up.	
	DISP_HBACK	4	H pixel read out direction. 0: Forward. 1: Back.	
	RGB_TRS_EN	3	RGB Transparent color enable.	
	GWIN_YUVOUT	2	GOP out format. 0: RGB. 1: VYU.	
	-	1	Reserved.	
	OUT_RDY	0	Output ready.	
01h (120B02h)	**REG120B02**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_PINPON_DWIN	7	GWIN1 PINPON mode (with DWIN).	
	-	6:3	Reserved.	
	GWIN_DEST[2:0]	2:0	GOP destination. 0: SC0_IP_MAIN. 1: SC0_IP_SUB. 2: SC0_OP. 3: MVOP. 4: SC1_IP_MAIN. 5: SC1_OP. 6: SC2_OP. 7: DIP.	
08h (120B10h)	**REG120B10**	**7:0**	**Default : 0xBB**	**Access : R/W**
	-	7:5	Reserved.	
	DUMMY0_INT_MASK	4	Dummy0 interrupt mask.	
	FLD_INT_MASK	3	Fld interrupt mask.	
	-	2	Reserved.	
	VS1_INT_MASK	1	VS1 interrupt mask.	
	VS0_INT_MASK	0	VS0 interrupt mask.	

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GOPG3_0 Register (Bank = 120B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (120B11h)	**REG120B11**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	FLD	6	Field info.	
	-	5:4	Reserved.	
	FLD_ERR_INT	3	Field interrupt.	
	-	2	Reserved.	
	VS1_INT	1	VS1 interrupt flag.	
	VS0_INT	0	VS0 interrupt flag.	
09h (120B12h)	**REG120B12**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	RDMA_STATE[2:0]	2:0	RDMA state. 0: REGDMA_STR. 1: REGDMA_SEND0. 2: REGDMA_SEND1. 4: WAIT_RDMA_GO. 6: WAIT_MIU_ACK. 7: DMA_IDLE.	
09h (120B13h)	**REG120B13**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	LB0_BIST_FAIL	6	LB0 BIST.	
	PSRAM_BIST_FAIL	5	PSRAM BIST.	
	GW_FF_BIST_FAIL	4	Buffer BIST.	
	LB_UF	3	Line buffer underflow.	
	LB_OF	2	Line buffer overflow.	
	GW_UF	1	Buffer underflow.	
	GW_OF	0	Buffer overflow.	
0Bh (120B16h)	**REG120B16**	**7:0**	**Default : 0x00**	**Access : R/W**
	THREE_D_MIDDLE_OFFSET_Q[7:0]	7:0	Garbage line num in top bottom mode. (offset shoud be set to 0 on ip).	
0Bh (120B17h)	**REG120B17**	**7:0**	**Default : 0x00**	**Access : R/W**
	RDMA_FF_CMPRS_EN_Q[1:0]	7:6	Enable rdma ff compress. 00: Compress mode off. 01: Transparent mode. 10: Uni color mode. 11: Both transparent/ uni color mode.	

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GOPG3_0 Register (Bank = 120B)

Index (Absolute)	Mnemonic	Bit	Description	
	HANDSHAKE_MODE_Q	5	Enable hand-shaking valid bit =1.	
	THREE_D_PIX_INI_Q[4:0]	4:0	Set initial start pix in side by side mode.	
0Ch (120B18h)	**REG120B18**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_PIX_NUM_Q[7:0]	7:0	Set output valid bit num in one line.	
0Ch (120B19h)	**REG120B19**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_PIX_NUM_Q[11:8]	3:0	See description of '120B18h'.	
0Dh (120B1Ah)	**REG120B1A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VALID_LINE_NUM_Q[7:0]	7:0	Set output valid line num in one frame.	
0Dh (120B1Bh)	**REG120B1B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VALID_LINE_NUM_Q[11:8]	3:0	See description of '120B1Ah'.	
0Eh (120B1Ch)	**REG120B1C**	**7:0**	**Default : 0x69**	**Access : R/W**
	RDMA_HT[7:0]	7:0	RDMA H total (unit: 2 pixels) > reg_strch_size.	
0Eh (120B1Dh)	**REG120B1D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	RDMA_HT[10:8]	2:0	See description of '120B1Ch'.	
0Fh (120B1Eh)	**REG120B1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PIPE_Q[7:0]	7:0	Hsync input pipe delay.	
0Fh (120B1Fh)	**REG120B1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HS_PIPE_Q[9:8]	1:0	See description of '120B1Eh'.	
10h (120B20h)	**REG120B20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SLOW_RATIO[5:0]	5:0	FIFO read out slow ratio.	
10h (120B21h)	**REG120B21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SLOW_THD[6:0]	6:0	FIFO out speed slow down when data counts <= SLOW_THD.	
11h (120B22h)	**REG120B22**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_Q[7:0]	7:0	Brightness value: -256~255. Use 2's complement.	
11h	**REG120B23**	**7:0**	**Default : 0x20**	**Access : R/W**

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GOPG3_0 Register (Bank = 120B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120B23h)	-	7	Reserved.	
	CON_YG_Q[5:0]	6:1	Y Contrast gain. Gain = REG_CON / 16.	
	BRI_Q[8]	0	See description of '120B22h'.	
12h (120B24h)	**REG120B24**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_UB_Q[5:0]	5:0	U Contrast gain. Gain = REG_CON / 16.	
12h (120B25h)	**REG120B25**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON_VR_Q[5:0]	5:0	V Contrast gain. Gain = REG_CON / 16.	
19h (120B32h)	**REG120B32**	**7:0**	**Default : 0xF0**	**Access : R/W**
	DMA_THD[7:0]	7:0	DMA FIFO threshold.	
19h (120B33h)	**REG120B33**	**7:0**	**Default : 0x42**	**Access : R/W**
	GW_HI_TSH[1:0]	7:6	DMA access high priority.	
	-	5	Reserved.	
	DMA_EXT[4:0]	4:0	DMA Burst length new mode: DMA_EXT [4:0]. 0: FF depth - current level. (equal the "burst all" in old mode). 31: 255. else: 8*DMA_EXT.	
1Ch (120B38h)	**REG120B38**	**7:0**	**Default : 0x7D**	**Access : R/W**
	-	7	Reserved.	
	DMA_BURST_LEVEL[6:0]	6:0	Target level of rdma ff each time into burst state, valid level : h0~h7d(0~125).	
1Ch (120B39h)	**REG120B39**	**7:0**	**Default : 0x00**	**Access : R/W**
	LB_COUPLE_EN	7	Couple RDMA ff with strch ff when strch_V off.	
	-	6:0	Reserved.	
1Dh (120B3Ah)	**REG120B3A**	**7:0**	**Default : 0x20**	**Access : R/W**
	ACCURATE_HI_TSH_EN	7	DMA access high priority : accurate mode enable.	
	ACCURATE_GW_HI_TSH[6:0]	6:0	DMA access high priority level (unit : 1/128 FF depth).	
1Eh (120B3Ch)	**REG120B3C**	**7:0**	**Default : 0x20**	**Access : R/W**
	THREE_D_MIDDLE_Q[7:0]	7:0	Set three d middle.	

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GOPG3_0 Register (Bank = 120B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Eh (120B3Dh)	**REG120B3D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	THREE_D_MIDDLE_Q[11:8]	3:0	See description of '120B3Ch'.	
20h (120B40h)	**REG120B40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRI0_Q[1:0]	1:0	1st priority GWIN number.	
24h (120B48h)	**REG120B48**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[7:0]	7:0	Transparent color key {R[7:0], G[7:0], B[7:0]}: for RGB source.	
24h (120B49h)	**REG120B49**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[15:8]	7:0	See description of '120B48h'.	
25h (120B4Ah)	**REG120B4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_RGB_Q[23:16]	7:0	See description of '120B48h'.	
26h (120B4Ch)	**REG120B4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[7:0]	7:0	Transparent color key {V[7:0], Y[7:0], U[7:0]}: for YUV source.	
26h (120B4Dh)	**REG120B4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[15:8]	7:0	See description of '120B4Ch'.	
27h (120B4Eh)	**REG120B4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR_YUV_Q[23:16]	7:0	See description of '120B4Ch'.	
28h (120B50h)	**REG120B50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	THREE_D_MODE_Q[2:0]	3:1	3D OSD mode: 0: Off. 1: L/R swith by frame. 2: L/R side by side. 3: L/R top - bottom. 4: L/R line alternative.	
	3D_FLAG_INV_Q	0	Input 3D flag L/R inverse.	
28h (120B51h)	**REG120B51**	**7:0**	**Default : 0x00**	**Access : R/W**
	YC_SWAP_Q	7	Switch Y/C when dtype is UV8Y8.	
	UV_SWAP_Q	6	Switch U/V (R/B).	
	-	5:0	Reserved.	
30h	**REG120B60**	**7:0**	**Default : 0x68**	**Access : R/W**

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GOPG3_0 Register (Bank = 120B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120B60h)	STRCH_HSIZE_Q[7:0]	7:0	Stretch Window H size (unit: 2 pixel). When V stretch ratio=1, hsize has no size limit. When V stretch ratio !=1, the max hsize is limited by line buffer size.	
30h (120B61h)	**REG120B61**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	STRCH_HSIZE_Q[10:8]	2:0	See description of '120B60h'.	
31h (120B62h)	**REG120B62**	**7:0**	**Default : 0x40**	**Access : R/W**
	STRCH_VSIZE_Q[7:0]	7:0	Stretch Window V size.	
31h (120B63h)	**REG120B63**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VSIZE_Q[11:8]	3:0	See description of '120B62h'.	
32h (120B64h)	**REG120B64**	**7:0**	**Default : 0x64**	**Access : R/W**
	STRCH_HST_Q[7:0]	7:0	Stretch Window H coordinate.	
32h (120B65h)	**REG120B65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	STRCH_HST_Q[12:8]	4:0	See description of '120B64h'.	
34h (120B68h)	**REG120B68**	**7:0**	**Default : 0x00**	**Access : R/W**
	STRCH_VST_Q[7:0]	7:0	Stretch Window V coordinate.	
34h (120B69h)	**REG120B69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_VST_Q[11:8]	3:0	See description of '120B68h'.	
35h (120B6Ah)	**REG120B6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSTRCH_Q[7:0]	7:0	Stretch H ratio. = In/Out* 2^12.	
35h (120B6Bh)	**REG120B6B**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	HSTRCH_Q[12:8]	4:0	See description of '120B6Ah'.	
36h (120B6Ch)	**REG120B6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTRCH_Q[7:0]	7:0	Stretch V ratio.	
36h (120B6Dh)	**REG120B6D**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	VSTRCH_Q[12:8]	4:0	See description of '120B6Ch'.	
38h	**REG120B70**	**7:0**	**Default : 0x00**	**Access : R/W**

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GOPG3_0 Register (Bank = 120B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(120B70h)	HSTRCH_INI_Q[7:0]	7:0	Stretch H start value.	
38h (120B71h)	**REG120B71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HSTRCH_INI_Q[12:8]	4:0	See description of '120B70h'.	
3Ah (120B74h)	**REG120B74**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TRS_STRCH	4	0: Transparent color only duplicate if stretch. 1: Stretch transparent color like normal color.	
	-	3:2	Reserved.	
	HSTRCH_MD[1:0]	1:0	H-stretch mode. 0: 6-tap (including nearest). 1: Duplicate.	
3Bh (120B76h)	**REG120B76**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	DYNAMIC_GATING_EN_Q	5	Enable dynamic gating.	
	-	4	Reserved.	
	OLD_ADDR	3	0: GOP DMA use new address. 1: GOP DMA use old address.	
	MIU_REQ_DISABLE	2	0: Normal gop to miu access. 1: Disable gop to miu access.	
	-	1:0	Reserved.	
3Bh (120B77h)	**REG120B77**	**7:0**	**Default : 0x80**	**Access : R/W**
	MIUREQ_HOLD_CYCLE_Q[3:0]	7:4	Compress mode turn on, set miu req hold time. base: 4. - >holdtime = miureq_hold_cycle x 4 x (cmpress rate).	
	-	3:0	Reserved.	
3Ch (120B78h)	**REG120B78**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CMQ_VS0_INT_MASK	5	CMQ VS0 interrupt mask.	
	-	4	Reserved.	
	MASK_1ST_HS_EVEN_Q	3	Mask 1st hsync in even field for GOP_VE.	
	MASK_1ST_HS_ODD_Q	2	Mask 1st hsync in odd field for GOP_VE.	
	-	1:0	Reserved.	

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GOPG3_1 Register (Bank = 120C)

GOPG3_1 Register (Bank = 120C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (120C00h)	**REG120C00**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_DTYPE_Q[3:0]	7:4	GWIN0 Source Data Type. 0: RGB1555/Blink. 1: RGB565. 2: ARGB4444. 3: 2266. 4. 8bit palette. 5: ARGB8888. 6: ARGB1555. 7.ABGR8888. 8: RGB1555/UV7Y8. 9: UV8Y8. 10.RGBA5551. 11.RGBA4444.	
	-	3:1	Reserved.	
	GWIN0_EN	0	Graphic window 0 Enable.	
00h (120C01h)	**REG120C01**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_TILE_16BPP_Q	7	16bpp Tile mode format. 0: Linear. 1: Tile mode.	

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GOPG3_1 Register (Bank = 120C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GWIN0_ALPHA_EN_Q	6	GWIN0 alpha_enable. 1: Pixel alpha. 0: Constant alpha.	
	-	5:0	Reserved.	
01h (120C02h)	**REG120C02**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, unit 1 word.	
01h (120C03h)	**REG120C03**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[15:8]	7:0	See description of '120C02h'.	
02h (120C04h)	**REG120C04**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_Q[23:16]	7:0	See description of '120C02h'.	
02h (120C05h)	**REG120C05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_Q[27:24]	3:0	See description of '120C02h'.	
03h (120C06h)	**REG120C06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HSTR_PIX0_Q[4:0]	4:0	Delete pixel number at hstart for pixel alignment unit:1 pixel.	
03h (120C07h)	**REG120C07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEL_HEND_PIX0_Q[4:0]	4:0	Delete pixel number at hend for pixel alignment unit:1 pixel.	
04h (120C08h)	**REG120C08**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_HSTR_Q[7:0]	7:0	The horizontal start pixel of Display Image for GWIN0. Unit: 1 word pixels.	
04h (120C09h)	**REG120C09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HSTR_Q[10:8]	2:0	See description of '120C08h'.	
05h (120C0Ah)	**REG120C0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	GWIN0_HEND_Q[7:0]	7:0	The horizontal end pixel of Display Image for GWIN0. Unit: 1 word pixels.	
05h (120C0Bh)	**REG120C0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_HEND_Q[10:8]	2:0	See description of '120C0Ah'.	

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GOPG3_1 Register (Bank = 120C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (120C0Ch)	**REG120C0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VSTR_Q[7:0]	7:0	The vertical start line of Display Image for GWIN0. Unit: 1 line.	
06h (120C0Dh)	**REG120C0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VSTR_Q[11:8]	3:0	See description of '120C0Ch'.	
08h (120C10h)	**REG120C10**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VEND_Q[7:0]	7:0	The vertical end line of Display Image for GWIN0. Unit: 1 line.	
08h (120C11h)	**REG120C11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GWIN0_VEND_Q[11:8]	3:0	See description of '120C10h'.	
09h (120C12h)	**REG120C12**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK0_HSIZE_Q[7:0]	7:0	Ring Block0 line size.	
09h (120C13h)	**REG120C13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RBLK0_HSIZE_Q[10:8]	2:0	See description of '120C12h'.	
0Ah (120C14h)	**REG120C14**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_ALPHA_Q[7:0]	7:0	GWIN0 constant alpha.	
0Ch (120C18h)	**REG120C18**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[7:0]	7:0	GWIN0 1st data offset address after REG_DRAM_RBLK0_STR, unit: 1 word.	
0Ch (120C19h)	**REG120C19**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[15:8]	7:0	See description of '120C18h'.	
0Dh (120C1Ah)	**REG120C1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_GWIN0_VSTR_Q[23:16]	7:0	See description of '120C18h'.	
0Dh (120C1Bh)	**REG120C1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_GWIN0_VSTR_Q[27:24]	3:0	See description of '120C18h'.	
16h (120C2Ch)	**REG120C2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GWIN0_FADE_INC_Q	6	FADE IN/OUT. 1: Stronger. 0: Weaker.	

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GOPG3_1 Register (Bank = 120C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GWIN0_FADE_INI_Q	5	FADE Initial.	
	GWIN0_FADE_EN_Q	4	FADE enable.	
	GWIN0_FADE_RATE_Q[3:0]	3:0	FADE frame Rate for GWIN0.	
1Eh (120C3Ch)	**REG120C3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[7:0]	7:0	Ring Block start address in dram for GWIN0 read out, 3D L/R mode unit 1 word.	
1Eh (120C3Dh)	**REG120C3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[15:8]	7:0	See description of '120C3Ch'.	
1Fh (120C3Eh)	**REG120C3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR_LR_Q[23:16]	7:0	See description of '120C3Ch'.	
1Fh (120C3Fh)	**REG120C3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DRAM_RBLK0_STR_LR_Q[27:24]	3:0	See description of '120C3Ch'.	

SEC_R2 Register (Bank = 122A)

SEC_R2 Register (Bank = 122A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	REG_IF_INSN_QUE0_LOW_INSN[7:0]	7:0	REG_IF_INSN_QUE0_LOW_INSN.	
00h (122A01h)	**REG122A01**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_IF_INSN_QUE0_LOW_INSN[15:8]	7:0	See description of '122A00h'.	
01h (122A02h)	**REG122A02**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE0_HIGH_INSN[7:0]	7:0	IF_INSN_QUE0_HIGH_INSN.	
01h (122A03h)	**REG122A03**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE0_HIGH_INSN[15:8]	7:0	See description of '122A02h'.	
02h (122A04h)	**REG122A04**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_IF_INSN_QUE1_LOW_INSN[7:0]	7:0	REG_IF_INSN_QUE1_LOW_INSN.	
02h (122A05h)	**REG122A05**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_IF_INSN_QUE1_LOW_INSN[15:8]	7:0	See description of '122A04h'.	
03h (122A06h)	**REG122A06**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE1_HIGH_INSN[7:0]	7:0	IF_INSN_QUE1_HIGH_INSN.	
03h (122A07h)	**REG122A07**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE1_HIGH_INSN[15:8]	7:0	See description of '122A06h'.	

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SEC_R2 Register (Bank = 122A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (122A08h)	**REG122A08**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE2_LOW_INSN[7:0]	7:0	IF_INSN_QUE2_LOW_INSN.	
04h (122A09h)	**REG122A09**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE2_LOW_INSN[15:8]	7:0	See description of '122A08h'.	
05h (122A0Ah)	**REG122A0A**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE2_HIGH_INSN[7:0]	7:0	IF_INSN_QUE2_HIGH_INSN.	
05h (122A0Bh)	**REG122A0B**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE2_HIGH_INSN[15:8]	7:0	See description of '122A0Ah'.	
06h (122A0Ch)	**REG122A0C**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_LOW_INSN[7:0]	7:0	IF_INSN_QUE3_LOW_INSN.	
06h (122A0Dh)	**REG122A0D**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_LOW_INSN[15:8]	7:0	See description of '122A0Ch'.	
07h (122A0Eh)	**REG122A0E**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_HIGH_INSN[7:0]	7:0	IF_INSN_QUE3_HIGH_INSN.	
07h (122A0Fh)	**REG122A0F**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_HIGH_INSN[15:8]	7:0	See description of '122A0Eh'.	
08h (122A10h)	**REG122A10**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE0_LOW_PC[7:0]	7:0	IF_INSN_QUE0_LOW_PC.	
08h (122A11h)	**REG122A11**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE0_LOW_PC[15:8]	7:0	See description of '122A10h'.	
09h (122A12h)	**REG122A12**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE0_HIGH_PC[7:0]	7:0	IF_INSN_QUE0_HIGH_PC.	
09h (122A13h)	**REG122A13**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE0_HIGH_PC[15:8]	7:0	See description of '122A12h'.	
0Ah (122A14h)	**REG122A14**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE1_LOW_PC[7:0]	7:0	IF_INSN_QUE1_LOW_PC.	
0Ah (122A15h)	**REG122A15**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE1_LOW_PC[15:8]	7:0	See description of '122A14h'.	
0Bh (122A16h)	**REG122A16**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE1_HIGH_PC[7:0]	7:0	IF_INSN_QUE1_HIGH_PC.	
0Bh (122A17h)	**REG122A17**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE1_HIGH_PC[15:8]	7:0	See description of '122A16h'.	
0Ch	**REG122A18**	**7:0**	**Default : 0x00**	**Access : RO**

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SEC_R2 Register (Bank = 122A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(122A18h)	IF_INSN_QUE2_LOW_PC[7:0]	7:0	IF_INSN_QUE2_LOW_PC.	
0Ch (122A19h)	**REG122A19**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE2_LOW_PC[15:8]	7:0	See description of '122A18h'.	
0Dh (122A1Ah)	**REG122A1A**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE2_HIGH_PC[7:0]	7:0	IF_INSN_QUE2_HIGH_PC.	
0Dh (122A1Bh)	**REG122A1B**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE2_HIGH_PC[15:8]	7:0	See description of '122A1Ah'.	
0Eh (122A1Ch)	**REG122A1C**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_LOW_PC[7:0]	7:0	IF_INSN_QUE3_LOW_PC.	
0Eh (122A1Dh)	**REG122A1D**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_LOW_PC[15:8]	7:0	See description of '122A1Ch'.	
0Fh (122A1Eh)	**REG122A1E**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_HIGH_PC[7:0]	7:0	IF_INSN_QUE3_HIGH_PC.	
0Fh (122A1Fh)	**REG122A1F**	**7:0**	**Default : 0x00**	**Access : RO**
	IF_INSN_QUE3_HIGH_PC[15:8]	7:0	See description of '122A1Eh'.	
10h (122A20h)	**REG122A20**	**7:0**	**Default : 0x00**	**Access : RO**
	GP[1:0]	7:6	GP.	
	EP[1:0]	5:4	EP.	
	IP[1:0]	3:2	IP.	
	FP[1:0]	1:0	FP.	

MAU0 Register (Bank = 122B)

MAU0 Register (Bank = 122B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (122B00h)	**REG122B00**	**7:0**	**Default : 0x10**	**Access : R/W**
	BURST_EN	7	Enable of burst-cascade function. 0: Disable. 1: Enable.	
	-	6:5	Reserved.	
	BURST_LENGTH[4:0]	4:0	Burst length of burst-cascade function.	
00h (122B01h)	**REG122B01**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	

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MAU0 Register (Bank = 122B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RQ_LENGTH[4:0]	4:0	The maximal length of continuous request. For single master.	
01h (122B02h)	**REG122B02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MST3_RD_BLOCK_WR_EN	3	MST3 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST2_RD_BLOCK_WR_EN	2	MST2 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST1_RD_BLOCK_WR_EN	1	MST1 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST0_RD_BLOCK_WR_EN	0	MST0 enable of RD block WR function. 0: Disable. 1: Enable.	
01h (122B03h)	**REG122B03**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MIU0_SIZE	0	MIU0 size. It's for continuous address mapping when miu0 size is smaller than the maximum of one miu entry. 0: 64MB. 1: 128MB.	
02h (122B04h)	**REG122B04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RST	0	S/W reset of all MAU. 0: Not reset. 1: Reset.	
03h (122B06h)	**REG122B06**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_TOP_DEBUG[7:0]	7:0	Debug status: MAU_TOP_DEBUG.	
03h (122B07h)	**REG122B07**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_TOP_DEBUG[15:8]	7:0	See description of '122B06h'.	
04h (122B08h)	**REG122B08**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX0_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX0_DEBUG.	
04h (122B09h)	**REG122B09**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX0_DEBUG[15:8]	7:0	See description of '122B08h'.	

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MAU0 Register (Bank = 122B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (122B0Ah)	**REG122B0A**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX1_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX1_DEBUG.	
05h (122B0Bh)	**REG122B0B**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX1_DEBUG[15:8]	7:0	See description of '122B0Ah'.	
06h (122B0Ch)	**REG122B0C**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX2_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX2_DEBUG.	
06h (122B0Dh)	**REG122B0D**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX2_DEBUG[15:8]	7:0	See description of '122B0Ch'.	
07h (122B0Eh)	**REG122B0E**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX3_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX3_DEBUG.	
07h (122B0Fh)	**REG122B0F**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX3_DEBUG[15:8]	7:0	See description of '122B0Eh'.	
08h (122B10h)	**REG122B10**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG0[7:0]	7:0	Debug status: MAU_ARB0_DEBUG0.	
08h (122B11h)	**REG122B11**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG0[15:8]	7:0	See description of '122B10h'.	
09h (122B12h)	**REG122B12**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG1[7:0]	7:0	Debug status: MAU_ARB0_DEBUG1.	
09h (122B13h)	**REG122B13**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG1[15:8]	7:0	See description of '122B12h'.	
0Ah (122B14h)	**REG122B14**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG0[7:0]	7:0	Debug status: MAU_ARB1_DEBUG0.	
0Ah (122B15h)	**REG122B15**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG0[15:8]	7:0	See description of '122B14h'.	
0Bh (122B16h)	**REG122B16**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG1[7:0]	7:0	Debug status: MAU_ARB1_DEBUG1.	
0Bh (122B17h)	**REG122B17**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG1[15:8]	7:0	See description of '122B16h'.	
0Ch (122B18h)	**REG122B18**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV0[7:0]	7:0	Reserved register 0.	
0Ch (122B19h)	**REG122B19**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV0[15:8]	7:0	See description of '122B18h'.	
0Dh	**REG122B1A**	**7:0**	**Default : 0x00**	**Access : R/W**

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MAU0 Register (Bank = 122B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(122B1Ah)	REV1[7:0]	7:0	Reserved register 1.	
0Dh (122B1Bh)	**REG122B1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV1[15:8]	7:0	See description of '122B1Ah'.	
0Eh (122B1Ch)	**REG122B1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV2[7:0]	7:0	Reserved register 2.	
0Eh (122B1Dh)	**REG122B1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV2[15:8]	7:0	See description of '122B1Ch'.	
0Fh (122B1Eh)	**REG122B1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV3[7:0]	7:0	Reserved register 3.	
0Fh (122B1Fh)	**REG122B1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV3[15:8]	7:0	See description of '122B1Eh'.	

MAU1 Register (Bank = 1234)

MAU1 Register (Bank = 1234)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (123440h)	**REG123440**	**7:0**	**Default : 0x10**	**Access : R/W**
	BURST_EN	7	Enable of burst-cascade function. 0: Disable. 1: Enable.	
	-	6:5	Reserved.	
	BURST_LENGTH[4:0]	4:0	Burst length of burst-cascade function.	
20h (123441h)	**REG123441**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	RQ_LENGTH[4:0]	4:0	The maximal length of continuous request. For single master.	
21h (123442h)	**REG123442**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MST3_RD_BLOCK_WR_EN	3	MST3 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST2_RD_BLOCK_WR_EN	2	MST2 enable of RD block WR function. 0: Disable. 1: Enable.	

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MAU1 Register (Bank = 1234)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MST1_RD_BLOCK_WR_EN	1	MST1 enable of RD block WR function. 0: Disable. 1: Enable.	
	MST0_RD_BLOCK_WR_EN	0	MST0 enable of RD block WR function. 0: Disable. 1: Enable.	
21h (123443h)	**REG123443**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MIU0_SIZE	0	MIU0 size. It's for continuous address mapping when miu0 size is smaller than the maximum of one miu entry. 0: 64MB. 1: 128MB.	
22h (123444h)	**REG123444**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RST	0	S/W reset of all MAU. 0: Not reset. 1: Reset.	
23h (123446h)	**REG123446**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_TOP_DEBUG[7:0]	7:0	Debug status: MAU_TOP_DEBUG.	
23h (123447h)	**REG123447**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_TOP_DEBUG[15:8]	7:0	See description of '123446h'.	
24h (123448h)	**REG123448**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX0_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX0_DEBUG.	
24h (123449h)	**REG123449**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX0_DEBUG[15:8]	7:0	See description of '123448h'.	
25h (12344Ah)	**REG12344A**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX1_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX1_DEBUG.	
25h (12344Bh)	**REG12344B**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX1_DEBUG[15:8]	7:0	See description of '12344Ah'.	
26h (12344Ch)	**REG12344C**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX2_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX2_DEBUG.	
26h (12344Dh)	**REG12344D**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX2_DEBUG[15:8]	7:0	See description of '12344Ch'.	
27h	**REG12344E**	**7:0**	**Default : 0x00**	**Access : RO**

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MAU1 Register (Bank = 1234)

Index (Absolute)	Mnemonic	Bit	Description	
(12344Eh)	MAU_DEMUX3_DEBUG[7:0]	7:0	Debug status: MAU_DEMUX3_DEBUG.	
27h (12344Fh)	**REG12344F**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_DEMUX3_DEBUG[15:8]	7:0	See description of '12344Eh'.	
28h (123450h)	**REG123450**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG0[7:0]	7:0	Debug status: MAU_ARB0_DEBUG0.	
28h (123451h)	**REG123451**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG0[15:8]	7:0	See description of '123450h'.	
29h (123452h)	**REG123452**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG1[7:0]	7:0	Debug status: MAU_ARB0_DEBUG1.	
29h (123453h)	**REG123453**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB0_DEBUG1[15:8]	7:0	See description of '123452h'.	
2Ah (123454h)	**REG123454**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG0[7:0]	7:0	Debug status: MAU_ARB1_DEBUG0.	
2Ah (123455h)	**REG123455**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG0[15:8]	7:0	See description of '123454h'.	
2Bh (123456h)	**REG123456**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG1[7:0]	7:0	Debug status: MAU_ARB1_DEBUG1.	
2Bh (123457h)	**REG123457**	**7:0**	**Default : 0x00**	**Access : RO**
	MAU_ARB1_DEBUG1[15:8]	7:0	See description of '123456h'.	
2Ch (123458h)	**REG123458**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV0[7:0]	7:0	Reserved register 0.	
2Ch (123459h)	**REG123459**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV0[15:8]	7:0	See description of '123458h'.	
2Dh (12345Ah)	**REG12345A**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV1[7:0]	7:0	Reserved register 1.	
2Dh (12345Bh)	**REG12345B**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV1[15:8]	7:0	See description of '12345Ah'.	
2Eh (12345Ch)	**REG12345C**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV2[7:0]	7:0	Reserved register 2.	
2Eh (12345Dh)	**REG12345D**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV2[15:8]	7:0	See description of '12345Ch'.	
2Fh (12345Eh)	**REG12345E**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV3[7:0]	7:0	Reserved register 3.	

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MAU1 Register (Bank = 1234)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (12345Fh)	**REG12345F**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV3[15:8]	7:0	See description of '12345Eh'.	

ROTATE Register (Bank = 150E)

ROTATE Register (Bank = 150E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (150E00h)	**REG150E00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ROT_SW_RST	1	SW reset.	
	TRIG_ROT	0	Trigger rotate engine start.	
00h (150E01h)	**REG150E01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IMI1_WLIMIT_EN	2	Imi buffer1 write protect enable.	
	IMI0_WLIMIT_EN	1	Imi buffer0 write protect enable.	
	EMI_WLIMIT_EN	0	Emi write protect enable.	
01h (150E02h)	**REG150E02**	**7:0**	**Default : 0xE0**	**Access : R/W**
	SRC_VSIZE[7:0]	7:0	Source height.	
01h (150E03h)	**REG150E03**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	SRC_VSIZE[12:8]	4:0	See description of '150E02h'.	
02h (150E04h)	**REG150E04**	**7:0**	**Default : 0xD0**	**Access : R/W**
	SRC_HSIZE[7:0]	7:0	Source width.	
02h (150E05h)	**REG150E05**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	SRC_HSIZE[12:8]	4:0	See description of '150E04h'.	
03h (150E06h)	**REG150E06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ROT_DEGREE[1:0]	5:4	Rotate degree (clockwise) : 0: 0. 1: 90. 2: 180. 3: 270.	
	-	3:2	Reserved.	

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ROTATE Register (Bank = 150E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SRC_FMT[1:0]	1:0	Source format. 0: YUV422. 1: RGB565. 2: 8888 (32bpp).	
03h (150E07h)	**REG150E07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	EMI_BURST_WLEN	6	EMI request burst write length. 0: 8. 1: 16.	
	-	5	Reserved.	
	EMI_BURST_RLEN	4	EMI request burst read length. 0: 8. 1: 16.	
	-	3:0	Reserved.	
04h (150E08h)	**REG150E08**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRC_BASE[7:0]	7:0	Source buffer base address.	
04h (150E09h)	**REG150E09**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRC_BASE[15:8]	7:0	See description of '150E08h'.	
05h (150E0Ah)	**REG150E0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRC_BASE[23:16]	7:0	See description of '150E08h'.	
05h (150E0Bh)	**REG150E0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SRC_BASE[27:24]	3:0	See description of '150E08h'.	
06h (150E0Ch)	**REG150E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DST_BASE[7:0]	7:0	Destination buffer base address.	
06h (150E0Dh)	**REG150E0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DST_BASE[15:8]	7:0	See description of '150E0Ch'.	
07h (150E0Eh)	**REG150E0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DST_BASE[23:16]	7:0	See description of '150E0Ch'.	
07h (150E0Fh)	**REG150E0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DST_BASE[27:24]	3:0	See description of '150E0Ch'.	
08h (150E10h)	**REG150E10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRC_PITCH[7:0]	7:0	Source buffer pitch.	

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ROTATE Register (Bank = 150E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (150E11h)	**REG150E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SRC_PITCH[11:8]	3:0	See description of '150E10h'.	
09h (150E12h)	**REG150E12**	**7:0**	**Default : 0x00**	**Access : R/W**
	DST_PITCH[7:0]	7:0	Destination buffer pitch.	
09h (150E13h)	**REG150E13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DST_PITCH[11:8]	3:0	See description of '150E12h'.	
0Ah (150E14h)	**REG150E14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMI_BASE0[7:0]	7:0	IMI buffer base address0.	
0Ah (150E15h)	**REG150E15**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMI_BASE0[15:8]	7:0	See description of '150E14h'.	
0Bh (150E16h)	**REG150E16**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMI_BASE0[23:16]	7:0	See description of '150E14h'.	
0Bh (150E17h)	**REG150E17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IMI_BASE0[27:24]	3:0	See description of '150E14h'.	
0Ch (150E18h)	**REG150E18**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMI_BASE1[7:0]	7:0	IMI buffer base address1.	
0Ch (150E19h)	**REG150E19**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMI_BASE1[15:8]	7:0	See description of '150E18h'.	
0Dh (150E1Ah)	**REG150E1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMI_BASE1[23:16]	7:0	See description of '150E18h'.	
0Dh (150E1Bh)	**REG150E1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IMI_BASE1[27:24]	3:0	See description of '150E18h'.	
0Fh (150E1Eh)	**REG150E1E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	BIST_FAIL[1:0]	1:0	BIST_FAIL status : 0: Emi read fifo. 1: Emi write fifo.	
10h (150E20h)	**REG150E20**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_EMI_WADR[7:0]	7:0	Emi write protect address.	

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ROTATE Register (Bank = 150E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (150E21h)	**REG150E21**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_EMI_WADR[15:8]	7:0	See description of '150E20h'.	
11h (150E22h)	**REG150E22**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_EMI_WADR[23:16]	7:0	See description of '150E20h'.	
11h (150E23h)	**REG150E23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LIMIT_EMI_WADR[27:24]	3:0	See description of '150E20h'.	
12h (150E24h)	**REG150E24**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_IMI0_WADR[7:0]	7:0	Imi buffer0 write protect address.	
12h (150E25h)	**REG150E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_IMI0_WADR[15:8]	7:0	See description of '150E24h'.	
13h (150E26h)	**REG150E26**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_IMI0_WADR[23:16]	7:0	See description of '150E24h'.	
13h (150E27h)	**REG150E27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LIMIT_IMI0_WADR[27:24]	3:0	See description of '150E24h'.	
14h (150E28h)	**REG150E28**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_IMI1_WADR[7:0]	7:0	Imi buffer1 write protect address.	
14h (150E29h)	**REG150E29**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_IMI1_WADR[15:8]	7:0	See description of '150E28h'.	
15h (150E2Ah)	**REG150E2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_IMI1_WADR[23:16]	7:0	See description of '150E28h'.	
15h (150E2Bh)	**REG150E2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LIMIT_IMI1_WADR[27:24]	3:0	See description of '150E28h'.	
20h (150E40h)	**REG150E40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	422_CBCR_SWAP	1	422_CBCR_SWAP.	
	422_YC_SWAP	0	422_YC_SWAP.	
70h (150EE0h)	**REG150EE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROT_DUMMY0[7:0]	7:0	ROT_DUMMY0.	
70h (150EE1h)	**REG150EE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROT_DUMMY0[15:8]	7:0	See description of '150EE0h'.	

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ROTATE Register (Bank = 150E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
71h (150EE2h)	**REG150EE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROT_DUMMY1[7:0]	7:0	ROT_DUMMY1.	
71h (150EE3h)	**REG150EE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROT_DUMMY1[15:8]	7:0	See description of '150EE2h'.	

HDMITX Register (Bank = 1515)

HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (151500h)	**REG151500**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC_MODE[1:0]	7:6	HDMI Deep Color mode. 00 = 24-bits. 01 = 30-bits. 10 = 36-bits. 11 = reserved.	
	-	5	Reserved.	
	PKT_MANUAL_MODE	4	0 = follow specification to send HDMI packets. 1 = send HDMI packets within each blank.	
	USER_ENABLE	3	0 = disable User packet generation. 1 = enable User packet generation. User packet is specified by modifying USER_TYPE, USER_HB and vender specific packet registers.	
	PACKET_ENABLE	2	0 = stop all packet generation. 1 = all packet command are normal.	
	-	1	Reserved.	
	DVI_MODE	0	0 = HDMI mode. 1 = DVI mode.	
00h (151501h)	**REG151501**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	BYPASS_DC_FIFO	4	Bypass Deep Color FIFO. 0: Normal. 1: Bypass.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HPLL_LOCK_CHK	3	Enable/Disable Deep Color FIFO if HDMI Deep Color PLL (HPLL) is lock/unlock. 0: Ignore HPLL lock status (always enable Deep Color FIFO). 1: Check HPLL lock status.	
	DC_FIFO_RST	2	Deep color FIFO reset. 0: No action. 1: Reset.	
	START_DE_PH[1:0]	1:0	The start phase of video data period (DE). Only valid at mode change. 00: 10P0/12P0. 01: 10P1/12P1. 10: 10P2/12P0.	
01h (151502h)	**REG151502**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACT_NULL_CMD	7	Write 1 to active NULL packet command. Read back for command status. 0 = command done. 1 = command in progress.	
	ACT_VSP_CMD	6	Write 1 to active VSP packet command. Read back for command status. 0 = command done. 1 = command in progress.	
	ACT_MPG_CMD	5	Write 1 to active MPG packet command. Read back for command status. 0 = command done. 1 = command in progress.	
	ACT_SPD_CMD	4	Write 1 to active SPD packet command. Read back for command status. 0 = command done. 1 = command in progress.	
	ACT_AUD_CMD	3	Write 1 to active AUD packet command. Read back for command status. 0 = command done. 1 = command in progress.	
	ACT_AVI_CMD	2	Write 1 to active AVI packet command. Read back for command status. 0 = command done. 1 = command in progress.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ACT_ACR_CMD	1	Write 1 to active ACR packet command. Read back for command status. 0 = command done. 1 = command in progress.	
	ACT_GCP_CMD	0	Write 1 to active GCP packet command. Read back for command status. 0 = command done. 1 = command in progress.	
01h (151503h)	**REG151503**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ACT_GMP_CMD	3	Write 1 to active GM packet command. 0: Command done. 1 = command in progress.	
	ACT_GCP_DC_CMD	2	Write 1 to active GCP packet command with non-zero CD value (Deep Color information). 0 = command done. 1 = command in progress.	
	ACT_ISP_CMD	1	Write 1 to active ISP1/2 packet command. Read back for command status. 0 = command done. 1 = command in progress.	
	ACT_ACP_CMD	0	Write 1 to active ACP packet command. Read back for command status. 0 = command done. 1 = command in progress.	
02h (151504h)	**REG151504**	**7:0**	**Default : 0x05**	**Access : R/W**
	NULL_FCNT[4:0]	7:3	Frame count for null packet generation.	
	NULL_CFG	2	Set/clear null packet send command. 0 = clear send command. 1 = set send command.	
	-	1	Reserved.	
	NULL_SEND_CMD	0	Set/clear null packet send command. 0 = clear send command. 1 = set send command.	
03h (151506h)	**REG151506**	**7:0**	**Default : 0x21**	**Access : R/W**
	-	7	Reserved.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EN_GC_DC_REQ	6	Enable to transmit a GCP with only non-Deep Color information (e.g. AVMUTE). 0: Disable. 1: Enable.	
	GC_FOLLOW_SPEC	5	GC packet test mode. 0 = test mode. 1 = normal mode.	
	GC_FCNT	4	Frame count for general control packet generation.	
	GC_CFG	3	0 = send GC packet single. 1 = send GC packet per GC_FCNT+1 frames.	
	AVMUTE_MODE[1:0]	2:1	00 = no setting command. 01 = Set_AVMUTE bit in General Control packet. 10 = Clear_AVMUTE bit in General Control packet. 11 = NA.	
	GC_SEND_CMD	0	Set/clear GC packet send command. 0 = clear send command. 1 = set send command.	
03h (151507h)	**REG151507**	**7:0**	**Default : 0x00**	**Access : R/W**
	GC_DC_FCNT[3:0]	7:4	Frame count for general control packet generation.	
	-	3:2	Reserved.	
	GC_DC_CFG	1	0 = send GC packet single. 1 = send GC packet per GC_FCNT+1 frames.	
	GC_DC_SEND_CMD	0	Set/clear GC packet send command. 0 = clear send command. 1 = set send command.	
04h (151508h)	**REG151508**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	PP_VAL[3:0]	7:4	Pixel packing phase. 0000: Phase 4 (10P4). 0001: Phase 1 (10P1, 12P1). 0010: Phase 2 (10P2, 12P2). 0011: Phase 3 (10P3). Others: Reserved.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CD_VAL[3:0]	3:0	Color depth. 0000: Color depth not indicated. 0100: 24 bits per pixel. 0101: 30 bits per pixel. 0110: 36 bits per pixel. Others: Reserved.	
04h (151509h)	**REG151509**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DEFAULT_PHASE	0	Default phase value.	
05h (15150Ah)	**REG15150A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTS_0[7:0]	7:0	CTS[15:0] for audio clock regeneration.	
05h (15150Bh)	**REG15150B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTS_0[15:8]	7:0	See description of '15150Ah'.	
06h (15150Ch)	**REG15150C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTS_1[3:0]	3:0	CTS[19:16] for audio clock regeneration.	
06h (15150Dh)	**REG15150D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	N_1[3:0]	3:0	N[19:16] code for audio clock regeneration.	
07h (15150Eh)	**REG15150E**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_0[7:0]	7:0	N[15:0] code for audio clock regeneration.	
07h (15150Fh)	**REG15150F**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_0[15:8]	7:0	See description of '15150Eh'.	
08h (151510h)	**REG151510**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACR_FCNT[3:0]	7:4	Frame count for ACR packet generation.	
	SEL_CTS_GEN	3	0 = automatically sent CTS value. 1 = manual mode sent CTS values.	
	ACR_CFG	2	0 = send ACR packet single. 1 = send ACR packet per ACR_FCNT+1 frames.	
	-	1	Reserved.	
	ACR_SEND_CMD	0	Set/clear ACR packet send command. 0 = clear send command. 1 = set send command.	
09h	**REG151512**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151512h)	AVI_IF1[7:0]	7:0	AVI InfoFrame byte 1. [1:0]: Scan info. [3:2]: Ban info. [4]: Active format info present. [6:5]: RGB or YCbCr. [7]: Version.	
09h (151513h)	**REG151513**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF2[7:0]	7:0	AVI InfoFrame byte 2. [3:0]: Active format aspect ratio. [5:4]: Picture aspect ratio. [7:6]: Colorimetry.	
0Ah (151514h)	**REG151514**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF3[7:0]	7:0	AVI InfoFrame byte 3. [1:0]: Non-conforming Picture Scaling. 00: No known non-uniform scaling. 01: Picture has been scaled horizontally. 10: Picture has been scaled vertically. 11: Picture has been scaled horizontally and vertically. [3:2]: Quantization range. [5:4]: Extended colorimetry. [7]: IT content.	
0Ah (151515h)	**REG151515**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF4[7:0]	7:0	AVI InfoFrame byte 4. [6:0]: Video Identification Code. Refer to EIA/CEA 861B specification. [7]: Reserved.	
0Bh (151516h)	**REG151516**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF5[7:0]	7:0	AVI InfoFrame byte 5. [3:0]: Pixel repetition; pixel sent (PR+1) times. [7:4]: Reserved.	
0Ch (151518h)	**REG151518**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF6[7:0]	7:0	AVI InfoFrame byte 6. Line Number of end of Top bar [7:0].	
0Ch (151519h)	**REG151519**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF7[7:0]	7:0	AVI InfoFrame byte 7. Line Number of end of Top bar [15:8].	
0Dh	**REG15151A**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15151Ah)	AVI_IF8[7:0]	7:0	AVI InfoFrame byte 8. Line Number of start of Bottom bar [7:0].	
0Dh (15151Bh)	**REG15151B**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF9[7:0]	7:0	AVI InfoFrame byte 9. Line Number of start of Bottom bar [15:8].	
0Eh (15151Ch)	**REG15151C**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF10[7:0]	7:0	AVI InfoFrame byte 10. Pixel Number of end of Left bar [7:0].	
0Eh (15151Dh)	**REG15151D**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF11[7:0]	7:0	AVI InfoFrame byte 11. Pixel Number of end of Left bar [15:8].	
0Fh (15151Eh)	**REG15151E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF12[7:0]	7:0	AVI InfoFrame byte 12. Pixel Number of end of Right bar [7:0].	
0Fh (15151Fh)	**REG15151F**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_IF13[7:0]	7:0	AVI InfoFrame byte 13. Pixel Number of end of Left bar [15:8].	
10h (151520h)	**REG151520**	**7:0**	**Default : 0x01**	**Access : R/W**
	AVI_FCNT[4:0]	7:3	Frame count for AVI packet generation.	
	AVI_CFG	2	0 = send AVI packet single. 1 = send AVI packet per AVI_FCNT+1 frames.	
	-	1	Reserved.	
	AVI_SEND_CMD	0	Set/clear AVI packet send command. 0 = clear send command. 1 = set send command.	
10h (151521h)	**REG151521**	**7:0**	**Default : 0x00**	**Access : R/W**
	AVI_CHK_SUM[7:0]	7:0	AVI packet check sum.	
11h	**REG151522**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151522h)	AUD_IF1[7:0]	7:0	Audio InfoFrame byte 1. [2:0]: Audio channel count. 000 = refer to stream header. Else channel count = CC +1. [3]: Reserved. [7:4]: Audio coding type. 0000 = refer to stream header. 0001 = IEC60958 PCM. 0010 = AC-3. 0011 = MPEG1 (Layer 1 & 2). 0100 = MP3 (MPEG1 Layer 3). 0101 = MPEG2 (multi-channel). 0110 = AAC. 0111 = DTS. 1000 = ATRAC. Others = Reserved.	
11h (151523h)	**REG151523**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUD_IF2[7:0]	7:0	Audio InfoFrame byte 2. [1:0]: Sample size. 00 = refer to stream header (or compressed stream). 01 = 16-bit. 10 = 20-bit. 11 = 24-bit. [4:2]: Sampling frequency. 000 = refer to stream header. 001 = 32k Hz. 010 = 44.1k Hz (CD). 011 = 48k Hz. 100 = 88.2k Hz. 101 = 96k Hz. 110 = 176.4k Hz. 111 = 192k Hz.	
12h (151524h)	**REG151524**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUD_IF3[7:0]	7:0	Audio InfoFrame byte 3. Max bit rate depending on Audio coding type. For compressed bit stream only. Max bit rate = MBR * 8k Hz.	
12h	**REG151525**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151525h)	AUD_IF4[7:0]	7:0	Audio InfoFrame byte 4. Channel allocation refer to EIA/CEA-861-B Table 22.	
13h (151526h)	**REG151526**	**7:0**	**Default : 0x01**	**Access : R/W**
	AUD_IF5[7:0]	7:0	Audio InfoFrame byte 4. [2:0]: Reserved. Must be 0. [6:3]: Level shift value. Attenuated value = LSV * (dB). [7]: Down-mix inhibit flag. 0 = Permitted or no data. 1 = Prohibited.	
14h (151528h)	**REG151528**	**7:0**	**Default : 0x01**	**Access : R/W**
	AUD_FCNT[4:0]	7:3	Frame count for audio info packet generation.	
	AUD_CFG	2	0 = send audio info packet single. 1 = send audio info packet per AUD_FCNT+1 frames.	
	-	1	Reserved.	
	AUD_SNED_CMD	0	Set/clear AUD packet send command. 0 = clear send command. 1 = set send command.	
14h (151529h)	**REG151529**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUD_CHK_SUM[7:0]	7:0	Audio InfoFrame packet check sum.	
15h (15152Ah)	**REG15152A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF1[6:0]	6:0	SPD InfoFrame byte 1.	
15h (15152Bh)	**REG15152B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF2[6:0]	6:0	SPD InfoFrame byte 2.	
16h (15152Ch)	**REG15152C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF3[6:0]	6:0	SPD InfoFrame byte 3.	
16h (15152Dh)	**REG15152D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF4[6:0]	6:0	SPD InfoFrame byte 4.	
17h (15152Eh)	**REG15152E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPD_IF5[6:0]	6:0	SPD InfoFrame byte 5.	
17h (15152Fh)	**REG15152F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF6[6:0]	6:0	SPD InfoFrame byte 6.	
18h (151530h)	**REG151530**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF7[6:0]	6:0	SPD InfoFrame byte 7.	
18h (151531h)	**REG151531**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF8[6:0]	6:0	SPD InfoFrame byte 8.	
19h (151532h)	**REG151532**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF9[6:0]	6:0	SPD InfoFrame byte 9.	
19h (151533h)	**REG151533**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF10[6:0]	6:0	SPD InfoFrame byte 10.	
1Ah (151534h)	**REG151534**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF11[6:0]	6:0	SPD InfoFrame byte 11.	
1Ah (151535h)	**REG151535**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF12[6:0]	6:0	SPD InfoFrame byte 12.	
1Bh (151536h)	**REG151536**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF13[6:0]	6:0	SPD InfoFrame byte 13.	
1Bh (151537h)	**REG151537**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF14[6:0]	6:0	SPD InfoFrame byte 14.	
1Ch (151538h)	**REG151538**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF15[6:0]	6:0	SPD InfoFrame byte 15.	
1Ch (151539h)	**REG151539**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPD_IF16[6:0]	6:0	SPD InfoFrame byte 16.	
1Dh (15153Ah)	**REG15153A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF17[6:0]	6:0	SPD InfoFrame byte 17.	
1Dh (15153Bh)	**REG15153B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF18[6:0]	6:0	SPD InfoFrame byte 18.	
1Eh (15153Ch)	**REG15153C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF19[6:0]	6:0	SPD InfoFrame byte 19.	
1Eh (15153Dh)	**REG15153D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF20[6:0]	6:0	SPD InfoFrame byte 20.	
1Fh (15153Eh)	**REG15153E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF21[6:0]	6:0	SPD InfoFrame byte 21.	
1Fh (15153Fh)	**REG15153F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF22[6:0]	6:0	SPD InfoFrame byte 22.	
20h (151540h)	**REG151540**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF23[6:0]	6:0	SPD InfoFrame byte 23.	
20h (151541h)	**REG151541**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF24[6:0]	6:0	SPD InfoFrame byte 24.	
21h (151542h)	**REG151542**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPD_IF25[6:0]	6:0	SPD InfoFrame byte 25.	
22h (151544h)	**REG151544**	**7:0**	**Default : 0x78**	**Access : R/W**
	SPD_FCNT[4:0]	7:3	Frame count for source product packet generation.	
	SPD_CFG	2	0 = send source product packet single. 1 = send source packet per SPD_FCNT+1 frames.	
	-	1	Reserved.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPD_SEND_CMD	0	Set/clear SPD packet send command. 0 = clear send command. 1 = set send command.	
22h (151545h)	**REG151545**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPD_CHK_SUM[7:0]	7:0	Source product packet check sum.	
23h (151546h)	**REG151546**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPEG_IF1[7:0]	7:0	MPEG InfoFrame byte 1.	
23h (151547h)	**REG151547**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPEG_IF2[7:0]	7:0	MPEG InfoFrame byte 2.	
24h (151548h)	**REG151548**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPEG_IF3[7:0]	7:0	MPEG InfoFrame byte 3.	
24h (151549h)	**REG151549**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPEG_IF4[7:0]	7:0	MPEG InfoFrame byte 4.	
25h (15154Ah)	**REG15154A**	**7:0**	**Default : 0x01**	**Access : R/W**
	MPEG_IF5[7:0]	7:0	MPEG InfoFrame byte 5.	
26h (15154Ch)	**REG15154C**	**7:0**	**Default : 0x01**	**Access : R/W**
	MPG_FCNT[4:0]	7:3	Frame count for MPEG source packet generation.	
	MPG_CFG	2	0 = send MPEG source packet single. 1 = send MPEG packet per MPG _FCNT+1 frames.	
	-	1	Reserved.	
	MPG_SEND_CMD	0	Set/clear MPG packet send command. 0 = clear send command. 1 = set send command.	
26h (15154Dh)	**REG15154D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPG_CHK_SUM[7:0]	7:0	MPEG source packet check sum.	
27h (15154Eh)	**REG15154E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF1[7:0]	7:0	Vendor Specific Packet payload byte 1. Payload byte 1 - IEEE Registration ID [7:0].	
27h (15154Fh)	**REG15154F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF2[7:0]	7:0	Vendor Specific Packet payload byte 2. Payload byte 2 - IEEE Registration ID [15:8].	
28h (151550h)	**REG151550**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF3[7:0]	7:0	Vendor Specific Packet payload byte 3. Payload byte 2 - IEEE Registration ID [23:16].	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (151551h)	**REG151551**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF4[7:0]	7:0	Vendor Specific Packet payload byte 4.	
29h (151552h)	**REG151552**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF5[7:0]	7:0	Vendor Specific Packet payload byte 5.	
29h (151553h)	**REG151553**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF6[7:0]	7:0	Vendor Specific Packet payload byte 6.	
2Ah (151554h)	**REG151554**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF7[7:0]	7:0	Vendor Specific Packet payload byte 7.	
2Ah (151555h)	**REG151555**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF8[7:0]	7:0	Vendor Specific Packet payload byte 8.	
2Bh (151556h)	**REG151556**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF9[7:0]	7:0	Vendor Specific Packet payload byte 9.	
2Bh (151557h)	**REG151557**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF10[7:0]	7:0	Vendor Specific Packet payload byte 10.	
2Ch (151558h)	**REG151558**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF11[7:0]	7:0	Vendor Specific Packet payload byte 11.	
2Ch (151559h)	**REG151559**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF12[7:0]	7:0	Vendor Specific Packet payload byte 12.	
2Dh (15155Ah)	**REG15155A**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF13[7:0]	7:0	Vendor Specific Packet payload byte 13.	
2Dh (15155Bh)	**REG15155B**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF14[7:0]	7:0	Vendor Specific Packet payload byte 14.	
2Eh (15155Ch)	**REG15155C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF15[7:0]	7:0	Vendor Specific Packet payload byte 15.	
2Eh (15155Dh)	**REG15155D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF16[7:0]	7:0	Vendor Specific Packet payload byte 16.	
2Fh (15155Eh)	**REG15155E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF17[7:0]	7:0	Vendor Specific Packet payload byte 17.	
2Fh (15155Fh)	**REG15155F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF18[7:0]	7:0	Vendor Specific Packet payload byte 18.	
30h (151560h)	**REG151560**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF19[7:0]	7:0	Vendor Specific Packet payload byte 19.	
30h	**REG151561**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151561h)	VS_IF20[7:0]	7:0	Vendor Specific Packet payload byte 20.	
31h (151562h)	**REG151562**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF21[7:0]	7:0	Vendor Specific Packet payload byte 21.	
31h (151563h)	**REG151563**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF22[7:0]	7:0	Vendor Specific Packet payload byte 22.	
32h (151564h)	**REG151564**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF23[7:0]	7:0	Vendor Specific Packet payload byte 23.	
32h (151565h)	**REG151565**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF24[7:0]	7:0	Vendor Specific Packet payload byte 24.	
33h (151566h)	**REG151566**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF25[7:0]	7:0	Vendor Specific Packet payload byte 25.	
33h (151567h)	**REG151567**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF26[7:0]	7:0	Vendor Specific Packet payload byte 26.	
34h (151568h)	**REG151568**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF27[7:0]	7:0	Vendor Specific Packet payload byte 27.	
34h (151569h)	**REG151569**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_IF28[7:0]	7:0	Vendor Specific Packet payload byte 28.	
35h (15156Ah)	**REG15156A**	**7:0**	**Default : 0x01**	**Access : R/W**
	VS_FCNT[4:0]	7:3	Frame count for vender specific packet generation.	
	VS_CFG	2	0 = send vender specific packet single. 1 = send vender packet per VS _FCNT+1 frames.	
	-	1	Reserved.	
	VS_SEND_CMD	0	Set/clear vender specific packet send command. 0 = clear send command. 1 = set send command.	
35h (15156Bh)	**REG15156B**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_CHK_SUM[7:0]	7:0	Vender specific packet check sum.	
36h (15156Ch)	**REG15156C**	**7:0**	**Default : 0x00**	**Access : R/W**
	USER_TYPE[7:0]	7:0	User defined packet type (byte 0 of header bytes).	
37h (15156Eh)	**REG15156E**	**7:0**	**Default : 0x00**	**Access : R/W**
	USER_HB1[7:0]	7:0	User defined packet type (header byte 2).	
37h (15156Fh)	**REG15156F**	**7:0**	**Default : 0x00**	**Access : R/W**
	USER_HB2[7:0]	7:0	User defined packet type (header byte 2).	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (151570h)	**REG151570**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB0[7:0]	7:0	ACP packet payload byte 0. 00h = ACP_TYPE is 00 / 01 / 11. 01h = DVD-Audio Type Dependent Generation. Others = Reserved.	
38h (151571h)	**REG151571**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB1[7:0]	7:0	ACP packet payload byte 1. [0]: Audio_transaction parameter. [2:1]: Audio_quality parameter. [5:3]: Audio_copy_number parameter. [7:6]: Audio_copy_permission parameter.	
39h (151572h)	**REG151572**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB2[7:0]	7:0	ACP packet payload byte 2.	
39h (151573h)	**REG151573**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB3[7:0]	7:0	ACP packet payload byte 3.	
3Ah (151574h)	**REG151574**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB4[7:0]	7:0	ACP packet payload byte 4.	
3Ah (151575h)	**REG151575**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB5[7:0]	7:0	ACP packet payload byte 5.	
3Bh (151576h)	**REG151576**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB6[7:0]	7:0	ACP packet payload byte 6.	
3Bh (151577h)	**REG151577**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB7[7:0]	7:0	ACP packet payload byte 7.	
3Ch (151578h)	**REG151578**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB8[7:0]	7:0	ACP packet payload byte 8.	
3Ch (151579h)	**REG151579**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB9[7:0]	7:0	ACP packet payload byte 9.	
3Dh (15157Ah)	**REG15157A**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB10[7:0]	7:0	ACP packet payload byte 10.	
3Dh (15157Bh)	**REG15157B**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB11[7:0]	7:0	ACP packet payload byte 11.	
3Eh (15157Ch)	**REG15157C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB12[7:0]	7:0	ACP packet payload byte 12.	
3Eh	**REG15157D**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15157Dh)	ACP_PB13[7:0]	7:0	ACP packet payload byte 13.	
3Fh (15157Eh)	**REG15157E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB14[7:0]	7:0	ACP packet payload byte 14.	
3Fh (15157Fh)	**REG15157F**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_PB15[7:0]	7:0	ACP packet payload byte 15.	
40h (151580h)	**REG151580**	**7:0**	**Default : 0x01**	**Access : R/W**
	ACP_FCNT[4:0]	7:3	Frame count for audio content protection packet.	
	ACP_CFG	2	0 = send ACP packet single. 1 = send ACP packet per ACP_FCNT+1 frames.	
	-	1	Reserved.	
	ACP_SEND_CMD	0	. Set/clear ACP packet send command. 0 = clear send command. 1 = set send command.	
40h (151581h)	**REG151581**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACP_HB1[7:0]	7:0	ACP packet header byte 1. Content protection type field from Audio Content Protection (ACP) packet. 0x00: Generic Audio. 0x01: IEC 60958-Identified Audio. 0x02: DVD-Audio. 0x03: Reserved for Super Audio CD (SACD). 0x04...0xFF: Reserved.	
41h (151582h)	**REG151582**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB0[7:0]	7:0	ISRC packet payload byte 0.	
41h (151583h)	**REG151583**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB1[7:0]	7:0	ISRC packet payload byte 1.	
42h (151584h)	**REG151584**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB2[7:0]	7:0	ISRC packet payload byte 2.	
42h (151585h)	**REG151585**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB3[7:0]	7:0	ISRC packet payload byte 3.	
43h (151586h)	**REG151586**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB4[7:0]	7:0	ISRC packet payload byte 4.	
43h (151587h)	**REG151587**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB5[7:0]	7:0	ISRC packet payload byte 5.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
44h (151588h)	**REG151588**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB6[7:0]	7:0	ISRC packet payload byte 6.	
44h (151589h)	**REG151589**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB7[7:0]	7:0	ISRC packet payload byte 7.	
45h (15158Ah)	**REG15158A**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB8[7:0]	7:0	ISRC packet payload byte 8.	
45h (15158Bh)	**REG15158B**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB9[7:0]	7:0	ISRC packet payload byte 9.	
46h (15158Ch)	**REG15158C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB10[7:0]	7:0	ISRC packet payload byte 10.	
46h (15158Dh)	**REG15158D**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB11[7:0]	7:0	ISRC packet payload byte 11.	
47h (15158Eh)	**REG15158E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB12[7:0]	7:0	ISRC packet payload byte 12.	
47h (15158Fh)	**REG15158F**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB13[7:0]	7:0	ISRC packet payload byte 13.	
48h (151590h)	**REG151590**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB14[7:0]	7:0	ISRC packet payload byte 14.	
48h (151591h)	**REG151591**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB15[7:0]	7:0	ISRC packet payload byte 15.	
49h (151592h)	**REG151592**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB16[7:0]	7:0	ISRC packet payload byte 16.	
49h (151593h)	**REG151593**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB17[7:0]	7:0	ISRC packet payload byte 17.	
4Ah (151594h)	**REG151594**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB18[7:0]	7:0	ISRC packet payload byte 18.	
4Ah (151595h)	**REG151595**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB19[7:0]	7:0	ISRC packet payload byte 19.	
4Bh (151596h)	**REG151596**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB20[7:0]	7:0	ISRC packet payload byte 20.	
4Bh (151597h)	**REG151597**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB21[7:0]	7:0	ISRC packet payload byte 21.	
4Ch	**REG151598**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151598h)	ISRC_PB22[7:0]	7:0	ISRC packet payload byte 22.	
4Ch (151599h)	**REG151599**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB23[7:0]	7:0	ISRC packet payload byte 23.	
4Dh (15159Ah)	**REG15159A**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB24[7:0]	7:0	ISRC packet payload byte 24.	
4Dh (15159Bh)	**REG15159B**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB25[7:0]	7:0	ISRC packet payload byte 25.	
4Eh (15159Ch)	**REG15159C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB26[7:0]	7:0	ISRC packet payload byte 26.	
4Eh (15159Dh)	**REG15159D**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB27[7:0]	7:0	ISRC packet payload byte 27.	
4Fh (15159Eh)	**REG15159E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB28[7:0]	7:0	ISRC packet payload byte 28.	
4Fh (15159Fh)	**REG15159F**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB29[7:0]	7:0	ISRC packet payload byte 29.	
50h (1515A0h)	**REG1515A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB30[7:0]	7:0	ISRC packet payload byte 30.	
50h (1515A1h)	**REG1515A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_PB31[7:0]	7:0	ISRC packet payload byte 31.	
51h (1515A2h)	**REG1515A2**	**7:0**	**Default : 0x38**	**Access : R/W**
	ISRC_FCNT[4:0]	7:3	Frame count for ISRC packet.	
	ISRC_CFG	2	0 = send ISRC packet single. 1 = send ISRC packet per ISRC_FCNT+1 frames.	
	-	1	Reserved.	
	ISRC_SEND_CMD	0	Set/clear ISRC packet send command. 0 = clear send command. 1 = set send command.	
51h (1515A3h)	**REG1515A3**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC_HB1[7:0]	7:0	ISRC header byte 1. Bit[7]=ISRC_Cont. Bit[6]=ISRC_Valid. Bit[5:3]=reserved. Bit[2:0]=ISRC_Status.	
52h	**REG1515A4**	**7:0**	**Default : 0x00**	**Access : RO**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1515A4h)	TMDS_DE_CNT[7:0]	7:0	DE count in TMDS domain.	
52h (1515A5h)	**REG1515A5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TMDS_DE_CNT[11:8]	3:0	See description of '1515A4h'.	
53h (1515A6h)	**REG1515A6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HPLL_LOCK_CNT[7:0]	7:0	Delay count value for HPLL lock output.	
53h (1515A7h)	**REG1515A7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HPLL_LOCK_CNT[15:8]	7:0	See description of '1515A6h'.	
54h (1515A8h)	**REG1515A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GM_FCNT[3:0]	7:4	Frame count for GM packet.	
	-	3	Reserved.	
	GM_CFG	2	0 = send GM packet single. 1 = send GM packet per GM_FCNT+1 frames.	
	-	1	Reserved.	
	GM_SEND_CMD	0	Set/clear GM packet send command. 0 = clear send command. 1 = set send command.	
54h (1515A9h)	**REG1515A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GM_HB1[7:0]	7:0	Gamut Metatdata packet header byte 1. Bit[7]=Next_Field. Bit[6:4]=GBD_profile. Bit[3:0]=Affected_Gamut_Seq_Num.	
55h (1515AAh)	**REG1515AA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GM_HB2[7:0]	7:0	Gamut Metadata packet header byte 2. Bit[7]=No_Crnt_GBD. Bit[6]=reserved. Bit[5:4]=Packet_Seq. Bit[3:0]=Current_Gamut_Seq_Num.	
55h (1515ABh)	**REG1515AB**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB0[7:0]	7:0	GBD byte 0.	
56h (1515ACh)	**REG1515AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB1[7:0]	7:0	GBD byte 1.	
56h (1515ADh)	**REG1515AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB2[7:0]	7:0	GBD byte 2.	
57h	**REG1515AE**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1515AEh)	GBD_SB3[7:0]	7:0	GBD byte 3.	
57h (1515AFh)	**REG1515AF**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB4[7:0]	7:0	GBD byte 4.	
58h (1515B0h)	**REG1515B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB5[7:0]	7:0	GBD byte 5.	
58h (1515B1h)	**REG1515B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB6[7:0]	7:0	GBD byte 6.	
59h (1515B2h)	**REG1515B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB7[7:0]	7:0	GBD byte 7.	
59h (1515B3h)	**REG1515B3**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB8[7:0]	7:0	GBD byte 8.	
5Ah (1515B4h)	**REG1515B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB9[7:0]	7:0	GBD byte 9.	
5Ah (1515B5h)	**REG1515B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB10[7:0]	7:0	GBD byte 10.	
5Bh (1515B6h)	**REG1515B6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB11[7:0]	7:0	GBD byte 11.	
5Bh (1515B7h)	**REG1515B7**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB12[7:0]	7:0	GBD byte 12.	
5Ch (1515B8h)	**REG1515B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB13[7:0]	7:0	GBD byte 13.	
5Ch (1515B9h)	**REG1515B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB14[15:8]	7:0	GBD byte 14.	
5Dh (1515BAh)	**REG1515BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB15[7:0]	7:0	GBD byte 15.	
5Dh (1515BBh)	**REG1515BB**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB16[15:8]	7:0	GBD byte 16.	
5Eh (1515BCh)	**REG1515BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB17[7:0]	7:0	GBD byte 17.	
5Eh (1515BDh)	**REG1515BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB18[15:8]	7:0	GBD byte 18.	
5Fh (1515BEh)	**REG1515BE**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB19[7:0]	7:0	GBD byte 19.	

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HDMITX Register (Bank = 1515)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Fh (1515BFh)	**REG1515BF**	**7:0**	**Default : 0x00**	**Access : R/W**
	GBD_SB20[15:8]	7:0	GBD byte 20. Write this byte to load GBD to TX buffer.	

HDMITX_VIDEO Register (Bank = 1516)

HDMITX_VIDEO Register (Bank = 1516)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (151600h)	**REG151600**	**7:0**	**Default : 0x4E**	**Access : R/W**
	BYPASS_MD_656	7	0: Enable BT656 data enable re-generator. 1: Disable BT656 data enable re-generator.	
	BYPASS_MD	6	Select output DE from internal DE generator or external DE input. 0: From internal DE generator. 1: From external DE input.	
	VS_GEN_SEL	5	Select external input VSYNC or internal vblank_earlyV (one line earlier than input VSYNC) to generate VSYNC in ve_vgen module. 0: Select external input VSYNC. 1: Select internal vblank_earlyV.	
	FIELD_SEL	4	Field information selection. 0: Select external input FIELD information. 1: Select internal generate FIELD information.	
	VS_POL	3	Hold or change the input VSYNC polarity. 0: Change polarity. 1: Hold polarity.	
	HS_POL	2	Hold or change the input HSYNC polarity. 0: Change polarity. 1: Hold polarity.	
	FIELD_POL	1	Hold or change the input FIELD polarity. 0: Change polarity. 1: Hold polarity.	
	INTERLACE	0	Set the video mode in INTERLACE or progressive mode. 0: Progressive mode. 1: INTERLACE mode.	
00h	**REG151601**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX_VIDEO Register (Bank = 1516)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151601h)	-	7:3	Reserved.	
	RB_SWAP	2	Set the video output data bus red & blue channel swap or not. 0: Normal. 1: Enable RB swap.	
	-	1	Reserved.	
	BT656	0	Video input timing is BT656 format or not. 0: Not BT.656 8-bit format. 1: BT.656 8-bit format.	
01h (151602h)	**REG151602**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VE_TMGEN_EN	3	Disable or enable VIDEO_ENGINE timing generation. 0: Disable. 1: Enable.	
	VS_GEN_POL	2	Set re-generated VSYNC pulse negative or positive polarity. 0: Negative polarity. 1: Positive polarity.	
	HS_GEN_POL	1	Set re-generated HSYNC pulse negative or positive polarity. 0: Negative polarity. 1: Positive polarity.	
	VH_GEN_EN	0	Disable or enable VSYNC/HSYNC re-generation. 0: Disable. 1: Enable.	
01h (151603h)	**REG151603**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HDTV_EN	6	Decide the video input format is HDTV or SDTV and select the coefficient to do YCbCr to RGB conversion. 0: SDTV format. 1: HDTV format.	
	DITH_SEL_CSC[1:0]	5:4	Dithering bit selection for CSC (YCbCr to RGB). 11: Select 2-bit dither noise. 01: Select 1-bit dither noise. x0: No dither noise.	
	DITH_SEL_GAMMA[1:0]	3:2	Dithering bit selection for Gamma inversion. 00: No dither noise. 01: Select 1-bit dither noise. 1x: Select 2-bit dither noise.	

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HDMITX_VIDEO Register (Bank = 1516)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INV_GAMMA_EN	1	Disable or enable inverse Gamma transfer. 0: Disable. 1: Enable.	
	Y2R_EN	0	Convert YCbCr video format to RGB format or bypass YCbCr data. 0: Bypass. 1: YCbCr to RGB.	
02h (151604h)	**REG151604**	**7:0**	**Default : 0x02**	**Access : R/W**
	VS_WIDTH[7:0]	7:0	VSYNC re-generate pulse width (line based). The default mode is 640x480p.	
03h (151606h)	**REG151606**	**7:0**	**Default : 0x21**	**Access : R/W**
	VS_BPORCH[7:0]	7:0	Vertical DE start line from VSYNC active (VSYNC Back porch width, line based). The default mode is 640x480p.	
03h (151607h)	**REG151607**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VS_BPORCH[8]	0	See description of '151606h'.	
04h (151608h)	**REG151608**	**7:0**	**Default : 0xE0**	**Access : R/W**
	VDE_LENGTH[7:0]	7:0	Vertical DE length (line base). The default mode is 640x480p.	
04h (151609h)	**REG151609**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	VDE_LENGTH[11:8]	3:0	See description of '151608h'.	
05h (15160Ah)	**REG15160A**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_DELAY_LINE[7:0]	7:0	VSYNC re-generate pulse delay (line based).	
06h (15160Ch)	**REG15160C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_DELAY_PIX[7:0]	7:0	VSYNC re-generate pulse delay (pixel based).	
06h (15160Dh)	**REG15160D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VS_DELAY_PIX[9:8]	1:0	See description of '15160Ch'.	
07h (15160Eh)	**REG15160E**	**7:0**	**Default : 0x60**	**Access : R/W**
	HS_WIDTH[7:0]	7:0	HSYNC re-generate pulse width (pixel based). The default mode is 640x480p.	
07h (15160Fh)	**REG15160F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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HDMITX_VIDEO Register (Bank = 1516)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HS_WIDTH[9:8]	1:0	See description of '15160Eh'.	
08h (151610h)	**REG151610**	**7:0**	**Default : 0x30**	**Access : R/W**
	HS_BPORCH[7:0]	7:0	Horizontal DE start pixel from HSYNC active (pixel based). The default mode is 640x480p.	
08h (151611h)	**REG151611**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HS_BPORCH[9:8]	1:0	See description of '151610h'.	
09h (151612h)	**REG151612**	**7:0**	**Default : 0x80**	**Access : R/W**
	DE_WIDTH[7:0]	7:0	Horizontal DE width (pixel based). The default mode is 640x480p.	
09h (151613h)	**REG151613**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	DE_WIDTH[11:8]	3:0	See description of '151612h'.	
0Ah (151614h)	**REG151614**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_DELAY[7:0]	7:0	HSYNC re-generate pulse delay (pixel based).	
0Ah (151615h)	**REG151615**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HS_DELAY[9:8]	1:0	See description of '151614h'.	
0Bh (151616h)	**REG151616**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VE_PG_EN	6	Enable or disable pixel pattern generator. 0: Disable. 1: Enable.	
	PG_HREP2	5	Disable or enable pixel repeated by 2 on horizontal direction. 0: Disable. 1: Enable.	
	PG_VREP2	4	Disable or enable pixel repeated by 2 on vertical direction. 0: Disable. 1: Enable.	
	PG_HMD[1:0]	3:2	Select pixel pattern generator in horizontal mode. 00: Gradient mode. 01: Inversion mode. 1x: Line mode.	

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HDMITX_VIDEO Register (Bank = 1516)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PG_VMD[1:0]	1:0	Select pixel pattern generator in vertical mode. 00: Gradient mode. 01: Inversion mode. 1x: Line mode.	
0Ch (151618h)	**REG151618**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_INI[7:0]	7:0	Set pixel generator pixel start value.	
0Ch (151619h)	**REG151619**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_INI[15:8]	7:0	See description of '151618h'.	
0Dh (15161Ah)	**REG15161A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_HINC[7:0]	7:0	Set pixel horizontal increment for horizontal gradient mode.	
0Dh (15161Bh)	**REG15161B**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_HINC[15:8]	7:0	See description of '15161Ah'.	
0Eh (15161Ch)	**REG15161C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_VINC[7:0]	7:0	Set pixel vertical increment for vertical gradient mode.	
0Eh (15161Dh)	**REG15161D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_VINC[15:8]	7:0	See description of '15161Ch'.	
0Fh (15161Eh)	**REG15161E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_HSTEP[7:0]	7:0	Set horizontal step size for pixel increment/inversion/line.	
10h (151620h)	**REG151620**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIX_VSTEP[7:0]	7:0	Set vertical step size for pixel increment/inversion/line.	
11h (151622h)	**REG151622**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

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HDMITX_VIDEO Register (Bank = 1516)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PG_COL_SEL[5:0]	5:0	[5:4] Select pixel pattern for R channel. 00: From pattern generator. 01: 00h. 10: 80h. 11: FFh. [3:2] Select pixel pattern for G channel. 00: From pattern generator. 01: 00h. 10: 80h. 11: FFh. [1:0] Select pixel pattern for B channel. 00: From pattern generator. 01: 00h. 10: 80h. 11: FFh.	
12h (151624h)	**REG151624**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MANUAL_PIX_RP	3	Manual mode for HDMI pixel-repetition rate. 0: Disable. 1: Enable.	
	PIX_RP_SEL[2:0]	2:0	HDMI pixel-repetition rate select (from 1 to 8 times). 3'hN: Pixel-repetition rate = N+1.	
13h (151626h)	**REG151626**	**7:0**	**Default : 0x0D**	**Access : R/W**
	VE_TMGEN_VTOTAL[7:0]	7:0	The vertical line number per video frame setting for VIDEO_ENGINE timing generation function; the default mode is 640x480p.	
13h (151627h)	**REG151627**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	VE_TMGEN_VTOTAL[11:8]	3:0	See description of '151626h'.	
14h (151628h)	**REG151628**	**7:0**	**Default : 0x20**	**Access : R/W**
	VE_TMGEN_HTOTAL[7:0]	7:0	The horizontal pixel number per line setting for VIDEO_ENGINE timing generation function; the default mode is 640x480p.	
14h (151629h)	**REG151629**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	VE_TMGEN_HTOTAL[11:8]	3:0	See description of '151628h'.	
15h	**REG15162A**	**7:0**	**Default : 0x00**	**Access : RO**

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HDMITX_VIDEO Register (Bank = 1516)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15162Ah)	VTOTAL[7:0]	7:0	The result of auto detecting the vertical line number per video frame.	
15h (15162Bh)	**REG15162B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	VTOTAL[11:8]	3:0	See description of '15162Ah'.	
16h (15162Ch)	**REG15162C**	**7:0**	**Default : 0x00**	**Access : RO**
	HTOTAL[7:0]	7:0	The result of auto detecting the horizontal pixel number per line.	
16h (15162Dh)	**REG15162D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTOTAL[12:8]	4:0	See description of '15162Ch'.	
17h (15162Eh)	**REG15162E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BIT16	2	The output data bus is 16-bit width or not. 0: Not 16-bit width. 1: 16-bit width.	
	BIT12	1	The output data bus is 12-bit width or not. 0: Not 12-bit width. 1: 12-bit width.	
	BIT10	0	The output data bus is 10-bit width or not. 0: Not 10-bit width. 1: 10-bit width.	
18h (151630h)	**REG151630**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HDMI422_B12	0	0: HDMI output format to 444 8-bit. 1: HDMI output format to 422 12-bit.	
20h ~ 21h (151640h ~ 151643h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

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HDMITX_AUDIO Register (Bank = 1517)

HDMITX_AUDIO Register (Bank = 1517)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (151700h)	**REG151700**	**7:0**	**Default : 0x00**	**Access : R/W**
	AFF_CH0[7:0]	7:0	S/PDIF input channel status [0:7]. Consumer format: Bit[0]. 0: Consumer. 1: Professional format. Bit[1]. 0: PCM. 1: Non PCM format. Bit[2] Copyright. 0: Asserted. 1: Not asserted. Bit[3:5] Emphasis. 000: Emphasis not indicated. 100: Emphasis CD-type. Bit[6:7] Channel status mode. 00: Mode zero. Others: Reserved.	
01h (151702h)	**REG151702**	**7:0**	**Default : 0x00**	**Access : R/W**
	AFF_CH1[7:0]	7:0	S/PDIF input channel status [8:15]. Consumer format: Bit 8-15: category code. 1000 0000: CD player. 1100 000L: DAT player. 1100 001L: DCC player. 1001 001L: Mini disc. L-bit carries information about generation status of the material.	
02h (151704h)	**REG151704**	**7:0**	**Default : 0x00**	**Access : R/W**
	AFF_CH2[7:0]	7:0	S/PDIF input channel status [16:23]. Consumer format: Bit[16:19]: source number (bit 16 is LSB). Bit[20:23]: channel number (bit 20 is LSB).	
03h	**REG151706**	**7:0**	**Default : 0x00**	**Access : R/W**

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HDMITX_AUDIO Register (Bank = 1517)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151706h)	AFF_CH3[7:0]	7:0	S/PDIF input channel status [24:31]. Consumer format: Bit[24:27] Sampling frequency. 0000: 44.1 kHz. 0100: 48 kHz. 1100: 32 kHz. Bit[28:29] Clock accuracy. 00: Level II, +-1000ppm. 01: Level III, variable pitch shifted. 10: Level I, +-50ppm. Bit[30:31]: Reserved.	
04h (151708h)	**REG151708**	**7:0**	**Default : 0x00**	**Access : R/W**
	AFF_CH4[7:0]	7:0	S/PDIF input channel status [32:39]. Consumer format: Bit 32: word length (field size). 0: Maximum length 20 bits. 1: Maximum length 24 bits. Bit [33:35] Word length. 000: Not indicated. 101: 24 bits (bit[32]=1) or 20 bits (bit[32]=0). 001: 23 bits (bit[32]=1) or 19 bits (bit[32]=0). 010: 22 bits (bit[32]=1) or 18 bits (bit[32]=0). 011: 21 bits (bit[32]=1) or 17 bits (bit[32]=0). 100: 20 bits (bit[32]=1) or 16 bits (bit[32]=0). Bit[36:39]: reserved.	
05h (15170Ah)	**REG15170A**	**7:0**	**Default : 0x82**	**Access : R/W**
	-	7	Reserved.	
	AFF_CFG_CH_EN[1:0]	6:5	Audio channel select. 00: Ch1. 01: Ch12. 10: Ch123. 11: Ch1234.	
	AFF_CFG_LAYOUT_FORMAT	4	Layout format select. 0: 2 channels. 1: 3 ~ 8 channels.	
	-	3	Reserved.	

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HDMITX_AUDIO Register (Bank = 1517)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AFF_CFG_CTS_GEN_EN	2	Enable CTS generator or not. 0: Disable CTS generator. 1: Enable CTS generator.	
	AFF_CFG_BS_AUTO	1	Auto block start. 0: SPDIF block start. 1: Auto block start.	
	AFF_CFG_FLUSH	0	Audio FIFO flush or not. 0: Not flush audio FIFO. 1: Flush audio FIFO.	
05h (15170Bh)	**REG15170B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MANUAL_FLAT_BIT	7	Audio flat bit value.	
	EN_INSERT_FLAT_BIT	6	Audio sample packet flat bit is controlled by register. 0: Disable. 1: Enable.	
	-	5:2	Reserved.	
	AFF_CFG_AU_FMT[1:0]	1:0	Audio source format select. 00: PCM. 01: DSD. 10: HBR. 11: N/A.	
06h (15170Ch)	**REG15170C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:3	Reserved.	
	AFF_OVERFLOW	2	Audio FIFO overflow or not. 0: FIFO not overflow. 1: FIFO overflow. Note: Write 1 to clear.	
	AFF_EMPTY	1	Audio FIFO empty or not. 0: FIFO not empty. 1: FIFO empty.	
	AFF_FULL	0	Audio FIFO full or not. 0: FIFO not full. 1: FIFO full.	
06h	**REG15170D**	**7:0**	**Default : 0x00**	**Access : RO**

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HDMITX_AUDIO Register (Bank = 1517)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15170Dh)	AFF_STATUS_FIFO_SEL[3:0]	7:4	Which FIFO is selected. [0] FIFO 0 is selected or not. 0: FIFO 0 is not selected. 1: FIFO 0 is selected. [1] FIFO 1 is selected or not. 0: FIFO 1 is not selected. 1: FIFO 1 is selected. [2] FIFO 2 is selected or not. 0: FIFO 2 is not selected. 1: FIFO 2 is selected. [3] FIFO 3 is selected or not. 0: FIFO 3 is not selected. 1: FIFO 3 is selected.	
	-	3:2	Reserved.	
	AFF_STATUS_WR_FSM[1:0]	1:0	Finite state machine for writing FIFO. 00: Write FIFO 0. 01: Write FIFO 1. 10: Write FIFO 2. 11: Write FIFO 3.	
07h (15170Eh)	**REG15170E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	AFF_PTR_WR[6:0]	6:0	Write pointer.	
07h (15170Fh)	**REG15170F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	AFF_PTR_RD[6:0]	6:0	Read pointer.	
08h ~ 08h (151710h ~ 151711h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DVFS Register (Bank = 1518)

DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**REG151800**	**7:0**	**Default : 0x00**	**Access : R/W**

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151800h)	COMBO_RSTZ_COMBO_WDT_EN	7	Combo_wdt (in combo) enable for combo rstz (0: disable wdt).	
	-	6:0	Reserved.	
00h (151801h)	**REG151801**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	COMBO_ASIC_RSTZ_COMBO_WDT_EN	0	Combo_wdt (in combo) enable for combo_asic rstz (0: disable wdt).	
02h (151805h)	**REG151805**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	COMBO_WDT_RSTZ_DELAY[2:0]	2:0	Combo wdt interrupt delay (wdt in combo).	
03h (151806h)	**REG151806**	**7:0**	**Default : 0x06**	**Access : R/W, WO**
	-	7:5	Reserved.	
	MMP_CPU_HOST_SW_AUTO_RST_CFG	4	Mmp cpu slave reset work with host suicide reset (1: slave work with host, 0:only host(default)). (work no matter reg_domain_mmp_ip_ctrl_sel == 0 or 1).	
	MMP_CPU_HOST_SW_AUTO_RST	3	Mmp cpu host suicide sw reset (auto clear). (work no matter reg_domain_mmp_ip_ctrl_sel == 0 or 1).	
	MMP_CPU_HOST2_SW_RSTZ	2	Mmp cpu host sw reset2 (1: work, 0: reset). (used to reset MIPS core). (work no matter reg_domain_mmp_ip_ctrl_sel == 0 or 1).	
	MMP_CPU_HOST_SW_RSTZ	1	Mmp cpu host sw reset (1: work, 0: reset). (used to reset MIPS clkgen and MIPS core). (work no matter reg_domain_mmp_ip_ctrl_sel == 0 or 1).	
	-	0	Reserved.	
04h (151808h)	**REG151808**	**7:0**	**Default : 0x04**	**Access : R/W, WO**
	-	7:4	Reserved.	
	COMBO_HOST_SW_AUTO_RST_CFG	3	Combo slave reset work with host suicide reset (1: slave work with host, 0:only host(default)).	
	COMBO_HOST_SW_RSTZ	2	Combo host sw reset (1: work, 0: reset).	
	COMBO_HOST_SW_AUTO_RST	1	Combo host suicide sw reset (auto clear).	
	COMBO_SW_RSTZ	0	Combo sw reset (1: work, 0: reset).	

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (151820h)	**REG151820**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLK_32K_INT_CLR[1:0]	5:4	Clk_32k int control. [0]: Clear posedge (write1/write0). [1]: Clear negedge (write1/write0).	
	-	3:2	Reserved.	
	CLK_32K_INT_MASK[1:0]	1:0	Clk_32k int mask. [0]: Posedge enable. [1]: Negedge enable.	
10h (151821h)	**REG151821**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLK_32K_INT_STATUS[1:0]	1:0	Clk_32k int control. [0]: Int status posedge. [1]: Int status negedge.	
11h (151822h)	**REG151822**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWR_ON_INT_MASK[3:0]	3:0	Power domain interrupt mask. Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
12h (151824h)	**REG151824**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	PWR_ON_INT_STATUS[3:0]	3:0	Power domain interrupt status. Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
13h (151826h)	**REG151826**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	PWR_ON_INT_CLR[3:0]	3:0	Power domain interrupt clear. Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
14h	**REG151828**	**7:0**	**Default : 0x00**	**Access : R/W**

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151828h)	-	7:4	Reserved.	
	PWR_ON_INT_MAIN_MASK[3:0]	3:0	Power domain interrupt mask. {mmp_cpu, dbb_cpu, dbb_dsp, combo} => [3:0].	
15h (15182Ah)	**REG15182A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	PWR_ON_INT_MAIN_STATUS[3:0]	3:0	Power domain interrupt status. {mmp_cpu, dbb_cpu, dbb_dsp, combo} => [3:0].	
16h (15182Ch)	**REG15182C**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	PWR_ON_INT_MAIN_CLR[3:0]	3:0	Power domain interrupt clear. {mmp_cpu, dbb_cpu, dbb_dsp, combo} => [3:0].	
20h (151840h)	**REG151840**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	MMP_MODECTRL[2:0]	2:0	MMP sysctrl mode control: 3'b100: normal. 3'b010: slow. 3'b001: doze. 3'b000: sleep.	
21h (151842h)	**REG151842**	**7:0**	**Default : 0x01**	**Access : RO, R/W, WO**
	-	7:3	Reserved.	
	MMP_CHECK_SLEEP_FLAG_CLR	2	Mmp sysctrl pass sleep flag clear (1: clear flag).	
	MMP_CHECK_SLEEP_FLAG	1	Mmp sysctrl pass sleep flag (1: sysctrl have sleeped).	
	MMP_AUTO_GO_SLOW	0	Mmp sysctrl auto go slow (1: en).	
22h (151844h)	**REG151844**	**7:0**	**Default : 0x1F**	**Access : R/W**
	MMP_XTALTIME[7:0]	7:0	Mmp xtal settling time initial (to 2^16).	
22h (151845h)	**REG151845**	**7:0**	**Default : 0xFE**	**Access : R/W**
	MMP_XTALTIME[15:8]	7:0	See description of '151844h'.	
23h (151846h)	**REG151846**	**7:0**	**Default : 0x7F**	**Access : R/W**
	MMP_PLLTIME[7:0]	7:0	Mmp pll lock on time initial (to 2^25).	
23h	**REG151847**	**7:0**	**Default : 0xC7**	**Access : R/W**

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151847h)	MMP_PLLTIME[15:8]	7:0	See description of '151846h'.	
24h (151848h)	**REG151848**	**7:0**	**Default : 0xFE**	**Access : R/W**
	MMP_PLLTIME[23:16]	7:0	See description of '151846h'.	
24h (151849h)	**REG151849**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MMP_PLLTIME[24]	0	See description of '151846h'.	
25h (15184Ah)	**REG15184A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMP_PWRUP_WAIT_TIME[7:0]	7:0	Mmp sysctrl EXIT_SLEEP timer value when use pure timer without checking LDOFSM state. (set 0 to disable timer).	
25h (15184Bh)	**REG15184B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMP_PWRUP_WAIT_TIME[15:8]	7:0	See description of '15184Ah'.	
26h (15184Ch)	**REG15184C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	MMP_WFI_VALUE	7	Mmp standbywfi override value (1: force wfi to 1).	
	MMP_WFI_OVER	6	Mmp standbywfi override (1: override).	
	MMP_PLL_ON	5	Mmp PLL status.	
	MMP_PLLEN	4	Mmp PLL sw control value.	
	MMP_PLLOVER	3	Mmp PLL control override by sw.	
	MMP_XTAL_ON	2	Mmp xtal status.	
	MMP_XTALEN	1	Mmp xtal sw control value.	
	MMP_XTALOVER	0	Mmp xtal control override by sw.	
26h (15184Dh)	**REG15184D**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7	Reserved.	
	MMP_LDOFSM_ACTIVE_VALUE	6	Mmp ldofsm_active_flag (from pmu) override value (1: active).	
	MMP_LDOFSM_ACTIVE_OVER	5	Mmp ldofsm_active_flag (from pmu) override (1: override).	
	-	4:3	Reserved.	
	MMP_HW_DFS_EN	2	Mmp DFS_en controlled by HW (1: hw).	
	MMP_NIRQ_VALUE	1	Mmp nirq override value (0: force nirq to 0).	
	MMP_NIRQ_OVER	0	Mmp nirq override (1: oevrride).	
27h (15184Eh)	**REG15184E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMP_SYSCTRL_STATE[3:0]	3:0	Mmp FSM state: 4'b0000 : SLEEP. 4'b0001 : DOZE. 4'b0011 : XTAL_CTL. 4'b1011 : SW_TO_XTAL. 4'b1001 : SW_FM_XTAL. 4'b0010 : SLOW. 4'b0110 : PLL_CTL. 4'b1110 : SW_TO_PLL. 4'b1010 : SW_FM_PLL. 4'b0100 : NORMAL. 4'b0111 : EXIT_SLEEP. 4'b0101 : WAIT_CPU.	
2Ch (151858h)	**REG151858**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMP_LOW_POWER_CFG[7:0]	7:0	Mmp low power config signal. [1:0] : 01 => CA9 power status will affect DVFS. [3:2] : 01 => CA9 enter debug mode, and DVFS will not enter sleep mode anymore.	
2Ch (151859h)	**REG151859**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMP_LOW_POWER_CFG[15:8]	7:0	See description of '151858h'.	
30h (151860h)	**REG151860**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	COMBO_MODECTRL[2:0]	2:0	Combo sysctrl mode control: 3'b100: normal. 3'b010: slow. 3'b001: doze. 3'b000: sleep.	
31h (151862h)	**REG151862**	**7:0**	**Default : 0x01**	**Access : RO, R/W, WO**
	-	7:3	Reserved.	
	COMBO_CHECK_SLEEP_FLAG_CLR	2	Combo sysctrl pass sleep flag clear (1: clear flag).	
	COMBO_CHECK_SLEEP_FLAG	1	Combo sysctrl pass sleep flag (1: sysctrl have sleeped).	
	COMBO_AUTO_GO_SLOW	0	Combo sysctrl auto go slow (1: en).	
32h (151864h)	**REG151864**	**7:0**	**Default : 0x1F**	**Access : R/W**
	COMBO_XTALTIME[7:0]	7:0	Combo xtal settling time initial (to 2^16).	
32h	**REG151865**	**7:0**	**Default : 0xFE**	**Access : R/W**

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(151865h)	COMBO_XTALTIME[15:8]	7:0	See description of '151864h'.	
33h (151866h)	**REG151866**	**7:0**	**Default : 0x7F**	**Access : R/W**
	COMBO_PLLTIME[7:0]	7:0	Combo pll lock on time initial (to 2^25).	
33h (151867h)	**REG151867**	**7:0**	**Default : 0xC7**	**Access : R/W**
	COMBO_PLLTIME[15:8]	7:0	See description of '151866h'.	
34h (151868h)	**REG151868**	**7:0**	**Default : 0xFE**	**Access : R/W**
	COMBO_PLLTIME[23:16]	7:0	See description of '151866h'.	
34h (151869h)	**REG151869**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	COMBO_PLLTIME[24]	0	See description of '151866h'.	
35h (15186Ah)	**REG15186A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_PWRUP_WAIT_TIME[7:0]	7:0	Combo sysctrl EXIT_SLEEP timer value when use pure timer without checking LDOFSM state. (set 0 to disable timer).	
35h (15186Bh)	**REG15186B**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_PWRUP_WAIT_TIME[15:8]	7:0	See description of '15186Ah'.	
36h (15186Ch)	**REG15186C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	COMBO_WFI_VALUE	7	Combo standbywfi override value (1: force wfi to 1).	
	COMBO_WFI_OVER	6	Combo standbywfi override (1: override).	
	COMBO_PLL_ON	5	Combo PLL status.	
	COMBO_PLLEN	4	Combo PLL sw control value.	
	COMBO_PLLOVER	3	Combo PLL control override by sw.	
	COMBO_XTAL_ON	2	Combo xtal status.	
	COMBO_XTALEN	1	Combo xtal sw control value.	
	COMBO_XTALOVER	0	Combo xtal control override by sw.	
36h (15186Dh)	**REG15186D**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7	Reserved.	
	COMBO_LDOFSM_ACTIVE_VALUE	6	Combo ldofsm_active_flag (from pmu) override value (1: active).	
	COMBO_LDOFSM_ACTIVE_OVER	5	Combo ldofsm_active_flag (from pmu) override (1: override).	
	-	4:3	Reserved.	
	COMBO_HW_DFS_EN	2	Combo DFS_en controlled by HW (1: hw).	

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COMBO_NIRQ_VALUE	1	Combo nirq override value (0: force nirq to 0).	
	COMBO_NIRQ_OVER	0	Combo nirq override (1: oevrride).	
37h (15186Eh)	**REG15186E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	COMBO_SYSCTRL_STATE[3:0]	3:0	Combo FSM state: 4'b0000 : SLEEP. 4'b0001 : DOZE. 4'b0011 : XTAL_CTL. 4'b1011 : SW_TO_XTAL. 4'b1001 : SW_FM_XTAL. 4'b0010 : SLOW. 4'b0110 : PLL_CTL. 4'b1110 : SW_TO_PLL. 4'b1010 : SW_FM_PLL. 4'b0100 : NORMAL. 4'b0111 : EXIT_SLEEP. 4'b0101 : WAIT_CPU.	
3Ch (151878h)	**REG151878**	**7:0**	**Default : 0x20**	**Access : R/W**
	COMBO_LOW_POWER_CFG[7:0]	7:0	Combo low power config signal. [0]: LS = Light-weight Sleep mode. [1]: SD = Shut Down. [7:4]: RM = Read Margin Control.	
3Ch (151879h)	**REG151879**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_LOW_POWER_CFG[15:8]	7:0	See description of '151878h'.	
40h (151880h)	**REG151880**	**7:0**	**Default : 0x03**	**Access : R/W, WO**
	-	7:4	Reserved.	
	MMP_PWR_SWITCH_TRG	3	Mmp ACTIVE_PWR_SWITCH trigger.	
	MMP_SLEEP_OFF_EN	2	Mmp power control when sysctrl entering SLEEP mode. 0: Stay power on. 1: Power down.	
	MMP_PWRON	1	Mmp power control, the register should be triggered by reg_pwr_switch (1 is power on, 0 is power down).	

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMP_SLEEP_TO_ACTIVE	0	Mmp power control when jumping out of SLEEP state. 0: Stay power down. 1: Power on.	
41h (151882h)	**REG151882**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MMP_PWR_CTRL_ST[2:0]	2:0	Mmp power fence control state: 3'b000: ON_TRUE. 3'b001: PWROFF_GO. 3'b011: PWROFF_FENCE. 3'b010: PWROFF_REQ. 3'b110: OFF_TRUE. 3'b111: PWRON_REQ. 3'b101: PWRON_GNT. 3'b100: PWRON_FENCE.	
42h (151884h)	**REG151884**	**7:0**	**Default : 0x7F**	**Access : RO, R/W**
	MMP_PF_CHECK_OFF_FLAG	7	Mmp pf_fsm pass off flag (1: pf_fsm have passed off state).	
	MMP_PF_SLPMD_ASYNC_EN	6	Mmp power-fence FSM sleep signal async catch (0: disable, 1: enable(default)).	
	MMP_PF_ON_OFF_DELAY_ENABLE	5	Mmp power fsm pwron_req/pwroff_req timer enable.	
	MMP_PF_DELAY_ENABLE	4	Mmp power fsm delay time enable.	
	MMP_PF_DELAY[3:0]	3:0	Mmp power fsm delay time.	
42h (151885h)	**REG151885**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	-	7:1	Reserved.	
	MMP_PF_CHECK_OFF_FLAG_CLR	0	Mmp pf_fsm pass off flag clear (1: clear flag).	
4Ch (151898h)	**REG151898**	**7:0**	**Default : 0x03**	**Access : R/W, WO**
	-	7:4	Reserved.	
	COMBO_PWR_SWITCH_TRG	3	Combo ACTIVE_PWR_SWITCH trigger.	
	COMBO_SLEEP_OFF_EN	2	Combo power control when sysctrl entering SLEEP mode. 0: Stay power on. 1: Power down.	

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COMBO_PWRON	1	Combo power control, the register should be triggered by reg_pwr_switch (1 is power on, 0 is power down).	
	COMBO_SLEEP_TO_ACTIVE	0	Combo power control when jumping out of SLEEP state. 0: Stay power down. 1: Power on.	
4Dh (15189Ah)	**REG15189A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	COMBO_PWR_CTRL_ST[2:0]	2:0	Combo power fence control state: 3'b000: ON_TRUE. 3'b001: PWROFF_GO. 3'b011: PWROFF_FENCE. 3'b010: PWROFF_REQ. 3'b110: OFF_TRUE. 3'b111: PWRON_REQ. 3'b101: PWRON_GNT. 3'b100: PWRON_FENCE.	
4Eh (15189Ch)	**REG15189C**	**7:0**	**Default : 0x7F**	**Access : RO, R/W**
	COMBO_PF_CHECK_OFF_FLAG	7	Combo pf_fsm pass off flag (1: pf_fsm have passed off state).	
	COMBO_PF_SLPMD_ASYNC_EN	6	Combo power-fence FSM sleep signal async catch (0: disable, 1: enable(default)).	
	COMBO_PF_ON_OFF_DELAY_ENABLE	5	Combo power fsm pwron_req/pwroff_req timer enable.	
	COMBO_PF_DELAY_ENABLE	4	Combo power fsm delay time enable.	
	COMBO_PF_DELAY[3:0]	3:0	Combo power fsm delay time.	
4Eh (15189Dh)	**REG15189D**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	-	7:1	Reserved.	
	COMBO_PF_CHECK_OFF_FLAG_CLR	0	Combo pf_fsm pass off flag clear (1: clear flag).	
50h (1518A0h)	**REG1518A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMP_WAKEUP_HWIMASK[7:0]	7:0	Mmp wakeup HW interrupt mask (1: enable interrupt).	
50h (1518A1h)	**REG1518A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMP_WAKEUP_HWIMASK[15:8]	7:0	See description of '1518A0h'.	
51h	**REG1518A2**	**7:0**	**Default : 0x00**	**Access : R/W**

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1518A2h)	MMP_WAKEUP_HWIMASK[23:16]	7:0	See description of '1518A0h'.	
52h (1518A4h)	**REG1518A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MMP_WAKEUP_FIQ_MCU_DLY[5:0]	5:0	Mmp wakeup fiq mcu delay value.	
53h (1518A6h)	**REG1518A6**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MMP_WAKEUP_SW_RESET	0	Mmp wakeup software reset (1: reset).	
54h (1518A8h)	**REG1518A8**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:2	Reserved.	
	MMP_WAKEUP_FIQSYS_CLR	1	Mmp wakeup fiq sys clear.	
	MMP_WAKEUP_FIQMCU_CLR	0	Mmp wakeup fiq mcu clear.	
54h (1518A9h)	**REG1518A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MMP_WAKEUP_COMBINED_FIQIRQ_EN	0	mmp: Enable for combined irqirq to fiqirq.	
55h (1518AAh)	**REG1518AA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MMP_WAKEUP_CLKON_MASK	0	Mmp clkon wakeup mask. 0: Non-mask / 1: mask.	
56h (1518ACh)	**REG1518AC**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	MMP_WAKEUP_STATUS[5:0]	5:0	Mmp wakeup status. [0]: ClkOn, [1]: FiqMcuReg, [2]: FiqSys, [3]: HwiOr, [4]: NFiqIrqCtrl, [5]: StandbyWfi.	
68h (1518D0h)	**REG1518D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_WAKEUP_HWIMASK[7:0]	7:0	Combo wakeup HW interrupt mask (1: enable interrupt).	
68h (1518D1h)	**REG1518D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_WAKEUP_HWIMASK[15:8]	7:0	See description of '1518D0h'.	
69h (1518D2h)	**REG1518D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBO_WAKEUP_HWIMASK[23:16]	7:0	See description of '1518D0h'.	

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Ah (1518D4h)	**REG1518D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	COMBO_WAKEUP_FIQ_MCU_DLY[5:0]	5:0	Combo wakeup fiq mcu delay value.	
6Bh (1518D6h)	**REG1518D6**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	COMBO_WAKEUP_SW_RESET	0	Combo wakeup software reset (1: reset).	
6Ch (1518D8h)	**REG1518D8**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:2	Reserved.	
	COMBO_WAKEUP_FIQSYS_CLR	1	Combo wakeup fiq sys clear.	
	COMBO_WAKEUP_FIQMCU_CLR	0	Combo wakeup fiq mcu clear.	
6Ch (1518D9h)	**REG1518D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	COMBO_WAKEUP_COMBINED_FIQIRQ_EN	0	combo: Enable for combined irqirq to fiqirq.	
6Dh (1518DAh)	**REG1518DA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	COMBO_WAKEUP_CLKON_MASK	0	Combo clkon wakeup mask. 0: Non-mask / 1: mask.	
6Eh (1518DCh)	**REG1518DC**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	COMBO_WAKEUP_STATUS[5:0]	5:0	Combo wakeup status. [0]: ClkOn, [1]: FiqMcuReg, [2]: FiqSys, [3]: HwiOr, [4]: NFiqIrqCtrl, [5]: StandbyWfi.	
70h (1518E0h)	**REG1518E0**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	NORMAL_PWRREQ_ON_TRIG[3:0]	3:0	Sw power domain power switch on trigger, (1: turn on corresponding domain, 0: untouched). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
71h (1518E2h)	**REG1518E2**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	NORMAL_PWRREQ_OFF_TRIG[3:0]	3:0	Sw power domain power switch off trigger, (1: turn off corresponding domain, 0: untouched). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
72h (1518E4h)	**REG1518E4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	NORMAL_PWRREQ_STATUS[3:0]	3:0	Sw power domain power switch status, (1: power on, 0: power off). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
73h (1518E6h)	**REG1518E6**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	NORMAL_PF_ON_TRIG[3:0]	3:0	Sw power domain power fence on trigger, (1: turn on corresponding pf, 0: untouched). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
74h (1518E8h)	**REG1518E8**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	NORMAL_PF_OFF_TRIG[3:0]	3:0	Sw power domain power fence off trigger, (1: turn off corresponding pf, 0: untouched). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
75h	**REG1518EA**	**7:0**	**Default : 0x00**	**Access : RO**

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DVFS Register (Bank = 1518)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1518EAh)	-	7:4	Reserved.	
	NORMAL_PF_STATUS[3:0]	3:0	Sw power domain power fence status, (1: fence on, 0: fence off). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
76h (1518ECh)	**REG1518EC**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	NORMAL_PWRRST_HIGH_TRIG[3:0]	3:0	Sw power domain power reset high trigger, (1: release reset of corresponding domain, 0: untouched). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
77h (1518EEh)	**REG1518EE**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	NORMAL_PWRRST_LOW_TRIG[3:0]	3:0	Sw power domain power reset low trigger, (1: reset the corresponding domain, 0: untouched). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
78h (1518F0h)	**REG1518F0**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	NORMAL_PWRRST_STATUS[3:0]	3:0	Sw power domain power reset status, (1: reset high (normal working), 0: reset low (under reset)). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.	
79h	**REG1518F2**	**7:0**	**Default : 0x00**	**Access : RO**

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DVFS Register (Bank = 1518)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(1518F2h)	-	7:4	Reserved.
	NORMAL_PWRGNT[3:0]	3:0	Sw power domain power grant (1: power is ready, 0: no power). Definition is as below: Sw_domain_3_peri_top. Sw_domain_2_g3d_top. Sw_domain_1_tsp_top. Sw_domain_0_sc_top.

TIMER_TOP0 Register (Bank = 151B)

TIMER_TOP0 Register (Bank = 151B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (151B00h)	**REG151B00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER_TRIG	1	set: Enable timer counting one time (from 0 to max, then stop). clear: By reset itself OR set reg_timer_en.	
	TIMER_EN	0	set: Enable timer counting rolled (from 0 to max, then rolled). clear: By reset itself OR set reg_timer_trig.	
00h (151B01h)	**REG151B01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TIMER_INT_EN	0	set: Enable interrupt. clear: By reset itself.	
01h (151B02h)	**REG151B02**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	TIMER_HIT	0	assert: When counter enabled and matches reg_timer_max. deassert: By write 1 OR set reg_timer_en, reg_timer_once, reg_timer_max.	
02h (151B04h)	**REG151B04**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
02h (151B05h)	**REG151B05**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[15:8]	7:0	See description of '151B04h'.	

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TIMER_TOP0 Register (Bank = 151B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (151B06h)	**REG151B06**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[23:16]	7:0	See description of '151B04h'.	
03h (151B07h)	**REG151B07**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[31:24]	7:0	See description of '151B04h'.	
04h (151B08h)	**REG151B08**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
04h (151B09h)	**REG151B09**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[15:8]	7:0	See description of '151B08h'.	
05h (151B0Ah)	**REG151B0A**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[23:16]	7:0	See description of '151B08h'.	
05h (151B0Bh)	**REG151B0B**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[31:24]	7:0	See description of '151B08h'.	

TIMER_TOP1 Register (Bank = 151B)

TIMER_TOP1 Register (Bank = 151B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (151B00h)	**REG151B00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER_TRIG	1	set: Enable timer counting one time (from 0 to max, then stop). clear: By reset itself OR set reg_timer_en.	
	TIMER_EN	0	set: Enable timer counting rolled (from 0 to max, then rolled). clear: By reset itself OR set reg_timer_trig.	
00h (151B01h)	**REG151B01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TIMER_INT_EN	0	set: Enable interrupt. clear: By reset itself.	
01h (151B02h)	**REG151B02**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

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TIMER_TOP1 Register (Bank = 151B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TIMER_HIT	0	assert: When counter enabled and matches reg_timer_max. deassert: By write 1 OR set reg_timer_en, reg_timer_once, reg_timer_max.	
02h (151B04h)	**REG151B04**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
02h (151B05h)	**REG151B05**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[15:8]	7:0	See description of '151B04h'.	
03h (151B06h)	**REG151B06**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[23:16]	7:0	See description of '151B04h'.	
03h (151B07h)	**REG151B07**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[31:24]	7:0	See description of '151B04h'.	
04h (151B08h)	**REG151B08**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
04h (151B09h)	**REG151B09**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[15:8]	7:0	See description of '151B08h'.	
05h (151B0Ah)	**REG151B0A**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[23:16]	7:0	See description of '151B08h'.	
05h (151B0Bh)	**REG151B0B**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[31:24]	7:0	See description of '151B08h'.	

DW_SPI_DMA Register (Bank = 151C)

DW_SPI_DMA Register (Bank = 151C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (151C00h)	**REG151C00**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_SW_RST	7	RX Engine software reset. 0: De-assert. 1: Assert.	
	TX_SW_RST	6	TX Engine software reset. 0: De-assert. 1: Assert.	

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DW_SPI_DMA Register (Bank = 151C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RX_ENDINA	5	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	TX_ENDINA	4	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	RX_URDMA_EN	3	URDMA RX Hardware Enable. 0: Disable. 1: Enable.	
	TX_URDMA_EN	2	URDMA TX Hardware Enable. 0: Disable. 1: Enable.	
	URDMA_MODE	1	URDMA Mode selects, when mode enable, URDMA hardware will replace MCU to access UART, otherwise MCU still control UART directly. 0: Disable. 1: Enable.	
	SW_RST	0	URDMA software reset. 0: De-assert. 1: Assert.	
00h (151C01h)	**REG151C01**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	RX_BUSY	5	RX controller in BUSY state.	
	TX_BUSY	4	TX controller in BUSY state.	
	RX_OP_MODE	3	RX controller operation mode. 0: Default. 1: Stop RX DMA activity when threshold interrupt occurs, until update RX_BUF_BASE.	
	RESERVE0[2:0]	2:0	Reserve.	
01h (151C02h)	**REG151C02**	**7:0**	**Default : 0x40**	**Access : R/W**
	INTR_THRESHOLD[7:0]	7:0	Interrupt threshold, to configure interrupt MCU period. Setting how much. Data received from UART, and alert MCU, byte unit.	
01h (151C03h)	**REG151C03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INTR_THRESHOLD[11:8]	3:0	See description of '151C02h'.	

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DW_SPI_DMA Register (Bank = 151C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (151C04h)	**REG151C04**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_H[7:0]	7:0	Configure TX buffer base address[26:16] in DRAM, 8byte unit.	
02h (151C05h)	**REG151C05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TX_BUF_BASE_H[10:8]	2:0	See description of '151C04h'.	
03h (151C06h)	**REG151C06**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[7:0]	7:0	Configure TX buffer base address[15:0] in DRAM, 8byte unit.	
03h (151C07h)	**REG151C07**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[15:8]	7:0	See description of '151C06h'.	
04h (151C08h)	**REG151C08**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_SIZE[7:0]	7:0	Configure TX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
04h (151C09h)	**REG151C09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TX_BUF_SIZE[12:8]	4:0	See description of '151C08h'.	
05h (151C0Ah)	**REG151C0A**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[7:0]	7:0	Read TX buffer read pointer from URDMA, byte unit.	
05h (151C0Bh)	**REG151C0B**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[15:8]	7:0	See description of '151C0Ah'.	
06h (151C0Ch)	**REG151C0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[7:0]	7:0	Update TX buffer write pointer to URDMA, byte unit.	
06h (151C0Dh)	**REG151C0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[15:8]	7:0	See description of '151C0Ch'.	
07h (151C0Eh)	**REG151C0E**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	TX_TIMEOUT[3:0]	3:0	Configure TX time out value, to clean TX buffer data and send to UART. 2^(TX_TIMEOUT) Cycle unit.	
08h (151C10h)	**REG151C10**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_H[7:0]	7:0	Configure RX buffer base address[26:16] in DRAM, 8byte unit.	

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DW_SPI_DMA Register (Bank = 151C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (151C11h)	**REG151C11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RX_BUF_BASE_H[10:8]	2:0	See description of '151C10h'.	
09h (151C12h)	**REG151C12**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[7:0]	7:0	Configure RX buffer base address[15:0] in DRAM, 8byte unit.	
09h (151C13h)	**REG151C13**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[15:8]	7:0	See description of '151C12h'.	
0Ah (151C14h)	**REG151C14**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_SIZE[7:0]	7:0	Configure RX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
0Ah (151C15h)	**REG151C15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RX_BUF_SIZE[12:8]	4:0	See description of '151C14h'.	
0Bh (151C16h)	**REG151C16**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[7:0]	7:0	Read RX buffer write pointer from URDMA, byte unit.	
0Bh (151C17h)	**REG151C17**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[15:8]	7:0	See description of '151C16h'.	
0Ch (151C18h)	**REG151C18**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	RX_TIMEOUT[3:0]	3:0	Configure RX time out value, to clean UART RX FIFO and write to DRAM. 2^(RX_TIMEOUT) Cycle unit.	
0Dh (151C1Ah)	**REG151C1A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RX_MCU_INTR	7	Identify rx controller to MCU interrupt event, this bit is logical OR of RX_INTR1~2 flag, and clear by RX_INTR_CLR.	
	RESERVE1	6	Reserve.	
	RX_INTR2	5	Identify Rx interrupt is cause by interrupt threshold function.	
	RX_INTR1	4	Identify Rx interrupt is cause by timeout function.	
	RESERVE	3	RESERVE.	
	RX_INTR2_EN	2	Rx interrupt threshold function enable.	
	RX_INTR1_EN	1	Rx timeout interrupt function enable.	

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DW_SPI_DMA Register (Bank = 151C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RX_INTR_CLR	0	MCU clear rx control interrupt signal. Once write and auto clear.	
0Dh (151C1Bh)	**REG151C1B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TX_MCU_INTR	7	Identify tx controller to MCU interrupt event.	
	RESERVE2[4:0]	6:2	Reserve.	
	TX_INTR_EN	1	TX controller to MCU interrupt enable.	
	TX_INTR_CLR	0	MCU clear tx control interrupt signal. Once write and auto clear.	
0Eh (151C1Ch)	**REG151C1C**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE3[7:0]	7:0	Reserve.	
0Eh (151C1Dh)	**REG151C1D**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE3[15:8]	7:0	See description of '151C1Ch'.	
0Fh (151C1Eh)	**REG151C1E**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[7:0]	7:0	Reserve.	
0Fh (151C1Fh)	**REG151C1F**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[15:8]	7:0	See description of '151C1Eh'.	
10h (151C20h)	**REG151C20**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	RESERVE5[4:0]	7:3	Reserve.	
	PREFCH_CLK_GATE1	2	Gated clock MINF post-write module. 0: Clock enable. 1: Clock gated.	
	PREFCH_CLK_GATE	1	Gated clock MINF pre-fetch module. 0: Clock enable. 1: Clock gated.	
	MINF_SW_RSTZ	0	MINF pre-fetch / post-write module SW reset. 0: SW reset. 1: Normal.	
10h (151C21h)	**REG151C21**	**7:0**	**Default : 0x00**	**Access : RO**
	POSTWR_BUSY	7	Identify MINF post write in busy state.	
	RESERVE5[11:5]	6:0	See description of '151C20h'.	
11h (151C22h)	**REG151C22**	**7:0**	**Default : 0x46**	**Access : R/W**
	PREFCH_PATCH	7	SW patch control bit.	

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DW_SPI_DMA Register (Bank = 151C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PREFCH_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	PREFCH_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	PREFCH_PRI	3	Define DRAM access priority.	
	PREFCH_RASTRD	2	MINF pre-fetch fast read enable.	
	PREFCH_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	PREFCH_CLR	0	SW clear MINF pre-fetch buffer. 0: Normal. 1: Clear.	
11h (151C23h)	**REG151C23**	**7:0**	**Default : 0x46**	**Access : R/W**
	POSTWR_FLUSH1_PATCH	7	SW flush path.	
	POSTWR_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	POSEWR_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	POSTWR_PRI	3	Define DRAM access priority.	
	POSTWR_FLUSH1	2	SW flush path.	
	POSTWR_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	POSTWR_FLUSH	0	SW flush MINF post write buffer. 0: Normal. 1: Flush.	

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SDIO20P_0 Register (Bank = 1520)

SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152000h)	**REG152000**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152001h)	**REG152001**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152002h)	**REG152002**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152003h)	**REG152003**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152004h)	**REG152004**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152005h)	**REG152005**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (152006h)	**REG152006**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152007h)	**REG152007**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152006h'.	
04h (152008h)	**REG152008**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h	**REG152009**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152009h)	DMA_ADDR_15_0[15:8]	7:0	See description of '152008h'.	
05h (15200Ah)	**REG15200A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15200Dh)	**REG15200D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15200Eh)	**REG15200E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152011h ~ 152013h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152014h)	**REG152014**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (152016h)	**REG152016**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152017h)	**REG152017**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152016h'.	
0Ch (152018h)	**REG152018**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152019h)	**REG152019**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '152018h'.	
0Dh (15201Ah)	**REG15201A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15201Bh)	**REG15201B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15201Ch)	**REG15201C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15201Dh)	**REG15201D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh	**REG15201E**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15201Eh)	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152020h)	**REG152020**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152021h)	**REG152021**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152022h)	**REG152022**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152023h)	**REG152023**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152024h)	**REG152024**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152025h)	**REG152025**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (152036h)	**REG152036**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152037h)	**REG152037**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152036h'.	
1Ch (152038h)	**REG152038**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152039h)	**REG152039**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152038h'.	

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (15203Ah)	**REG15203A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15203Bh)	**REG15203B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15203Ah'.	
1Eh (15203Ch)	**REG15203C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152058h ~ 152059h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15205Ah)	**REG15205A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (15205Ch)	**REG15205C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh	**REG15205E**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15205Eh)	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh (15205Fh)	**REG15205F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152060h)	**REG152060**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152061h)	**REG152061**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (152062h)	**REG152062**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152063h)	**REG152063**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152062h'.	
32h (152064h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152065h)	**REG152065**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152066h ~ 152067h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (152068h)	**REG152068**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152069h)	**REG152069**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152068h'.	
35h (15206Ah)	**REG15206A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	

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SDIO20P_0 Register (Bank = 1520)

Index (Absolute)	Mnemonic	Bit	Description	
38h (152070h)	**REG152070**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (152071h)	**REG152071**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152070h'.	
39h (152072h)	**REG152072**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152073h)	**REG152073**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152072h'.	
3Ah (152074h)	**REG152074**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152075h)	**REG152075**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152074h'.	
3Bh (152076h)	**REG152076**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152077h)	**REG152077**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152076h'.	
3Ch (152078h)	**REG152078**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152079h)	**REG152079**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152078h'.	

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SDIO20P_0 Register (Bank = 1520)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (15207Ah)	**REG15207A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15207Bh)	**REG15207B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15207Ah'.	

SDIO20P_1 Register (Bank = 1521)

SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152100h)	**REG152100**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152101h)	**REG152101**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152102h)	**REG152102**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152103h)	**REG152103**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152104h)	**REG152104**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152105h)	**REG152105**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (152106h)	**REG152106**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152107h)	**REG152107**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152106h'.	
04h (152108h)	**REG152108**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152109h)	**REG152109**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152108h'.	
05h (15210Ah)	**REG15210A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15210Dh)	**REG15210D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15210Eh)	**REG15210E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152111h ~ 152113h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152114h)	**REG152114**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh	**REG152116**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_1 Register (Bank = 1521)

Index (Absolute)	Mnemonic	Bit	Description	
(152116h)	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152117h)	**REG152117**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152116h'.	
0Ch (152118h)	**REG152118**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152119h)	**REG152119**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '152118h'.	
0Dh (15211Ah)	**REG15211A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15211Bh)	**REG15211B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15211Ch)	**REG15211C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15211Dh)	**REG15211D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (15211Eh)	**REG15211E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152120h)	**REG152120**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152121h)	**REG152121**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152122h)	**REG152122**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152123h)	**REG152123**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152124h)	**REG152124**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152125h)	**REG152125**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh	**REG152136**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152136h)	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152137h)	**REG152137**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152136h'.	
1Ch (152138h)	**REG152138**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152139h)	**REG152139**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152138h'.	
1Dh (15213Ah)	**REG15213A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15213Bh)	**REG15213B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15213Ah'.	
1Eh (15213Ch)	**REG15213C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152158h ~ 152159h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15215Ah)	**REG15215A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh	**REG15215C**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15215Ch)	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (15215Eh)	**REG15215E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh (15215Fh)	**REG15215F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152160h)	**REG152160**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152161h)	**REG152161**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (152162h)	**REG152162**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152163h)	**REG152163**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152162h'.	
32h (152164h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152165h)	**REG152165**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152166h ~ 152167h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h	**REG152168**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152168h)	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152169h)	**REG152169**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152168h'.	
35h (15216Ah)	**REG15216A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152170h)	**REG152170**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (152171h)	**REG152171**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152170h'.	
39h (152172h)	**REG152172**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152173h)	**REG152173**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152172h'.	
3Ah	**REG152174**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_1 Register (Bank = 1521)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152174h)	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152175h)	**REG152175**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152174h'.	
3Bh (152176h)	**REG152176**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152177h)	**REG152177**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152176h'.	
3Ch (152178h)	**REG152178**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152179h)	**REG152179**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152178h'.	
3Dh (15217Ah)	**REG15217A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15217Bh)	**REG15217B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15217Ah'.	

SDIO20P_2 Register (Bank = 1522)

SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152200h)	**REG152200**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152201h)	**REG152201**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152202h)	**REG152202**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152203h)	**REG152203**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152204h)	**REG152204**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152205h)	**REG152205**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (152206h)	**REG152206**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152207h)	**REG152207**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152206h'.	
04h (152208h)	**REG152208**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152209h)	**REG152209**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152208h'.	
05h (15220Ah)	**REG15220A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15220Dh)	**REG15220D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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SDIO20P_2 Register (Bank = 1522)

Index (Absolute)	Mnemonic	Bit	Description	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15220Eh)	**REG15220E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152211h ~ 152213h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152214h)	**REG152214**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (152216h)	**REG152216**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152217h)	**REG152217**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152216h'.	
0Ch (152218h)	**REG152218**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152219h)	**REG152219**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TR_BK_CNT[11:8]	3:0	See description of '152218h'.	
0Dh (15221Ah)	**REG15221A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15221Bh)	**REG15221B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15221Ch)	**REG15221C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15221Dh)	**REG15221D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (15221Eh)	**REG15221E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152220h)	**REG152220**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152221h)	**REG152221**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152222h)	**REG152222**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152223h)	**REG152223**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152224h)	**REG152224**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152225h)	**REG152225**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (152236h)	**REG152236**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152237h)	**REG152237**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152236h'.	
1Ch (152238h)	**REG152238**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152239h)	**REG152239**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152238h'.	
1Dh (15223Ah)	**REG15223A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15223Bh)	**REG15223B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15223Ah'.	
1Eh (15223Ch)	**REG15223C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152258h ~ 152259h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15225Ah)	**REG15225A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (15225Ch)	**REG15225C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (15225Eh)	**REG15225E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (15225Fh)	**REG15225F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152260h)	**REG152260**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152261h)	**REG152261**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h	**REG152262**	**7:0**	**Default : 0x00**	**Access : RO**

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152262h)	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152263h)	**REG152263**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152262h'.	
32h (152264h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152265h)	**REG152265**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152266h ~ 152267h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (152268h)	**REG152268**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152269h)	**REG152269**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152268h'.	
35h (15226Ah)	**REG15226A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152270h)	**REG152270**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h	**REG152271**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_2 Register (Bank = 1522)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152271h)	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152270h'.	
39h (152272h)	**REG152272**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152273h)	**REG152273**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152272h'.	
3Ah (152274h)	**REG152274**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152275h)	**REG152275**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152274h'.	
3Bh (152276h)	**REG152276**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152277h)	**REG152277**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152276h'.	
3Ch (152278h)	**REG152278**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152279h)	**REG152279**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152278h'.	
3Dh (15227Ah)	**REG15227A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15227Bh)	**REG15227B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15227Ah'.	

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SDIO20P_3 Register (Bank = 1523)

SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152300h)	**REG152300**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152301h)	**REG152301**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152302h)	**REG152302**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152303h)	**REG152303**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152304h)	**REG152304**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152305h)	**REG152305**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (152306h)	**REG152306**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152307h)	**REG152307**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152306h'.	
04h (152308h)	**REG152308**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h	**REG152309**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_3 Register (Bank = 1523)

Index (Absolute)	Mnemonic	Bit	Description	
(152309h)	DMA_ADDR_15_0[15:8]	7:0	See description of '152308h'.	
05h (15230Ah)	**REG15230A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15230Dh)	**REG15230D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15230Eh)	**REG15230E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152311h ~ 152313h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152314h)	**REG152314**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (152316h)	**REG152316**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152317h)	**REG152317**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152316h'.	
0Ch (152318h)	**REG152318**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152319h)	**REG152319**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '152318h'.	
0Dh (15231Ah)	**REG15231A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15231Bh)	**REG15231B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15231Ch)	**REG15231C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15231Dh)	**REG15231D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh	**REG15231E**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15231Eh)	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152320h)	**REG152320**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152321h)	**REG152321**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152322h)	**REG152322**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152323h)	**REG152323**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152324h)	**REG152324**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152325h)	**REG152325**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (152336h)	**REG152336**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152337h)	**REG152337**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152336h'.	
1Ch (152338h)	**REG152338**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152339h)	**REG152339**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152338h'.	

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SDIO20P_3 Register (Bank = 1523)

Index (Absolute)	Mnemonic	Bit	Description	
1Dh (15233Ah)	**REG15233A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15233Bh)	**REG15233B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15233Ah'.	
1Eh (15233Ch)	**REG15233C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152358h ~ 152359h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15235Ah)	**REG15235A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (15235Ch)	**REG15235C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh	**REG15235E**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15235Eh)	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh (15235Fh)	**REG15235F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152360h)	**REG152360**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152361h)	**REG152361**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (152362h)	**REG152362**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152363h)	**REG152363**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152362h'.	
32h (152364h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152365h)	**REG152365**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152366h ~ 152367h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (152368h)	**REG152368**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152369h)	**REG152369**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152368h'.	
35h (15236Ah)	**REG15236A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (152370h)	**REG152370**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (152371h)	**REG152371**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152370h'.	
39h (152372h)	**REG152372**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152373h)	**REG152373**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152372h'.	
3Ah (152374h)	**REG152374**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152375h)	**REG152375**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152374h'.	
3Bh (152376h)	**REG152376**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152377h)	**REG152377**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152376h'.	
3Ch (152378h)	**REG152378**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152379h)	**REG152379**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152378h'.	

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SDIO20P_3 Register (Bank = 1523)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (15237Ah)	**REG15237A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15237Bh)	**REG15237B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15237Ah'.	

SDIO20P1_0 Register (Bank = 1524)

SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152400h)	**REG152400**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152401h)	**REG152401**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152402h)	**REG152402**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152403h)	**REG152403**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152404h)	**REG152404**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152405h)	**REG152405**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (152406h)	**REG152406**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152407h)	**REG152407**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152406h'.	
04h (152408h)	**REG152408**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152409h)	**REG152409**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152408h'.	
05h (15240Ah)	**REG15240A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15240Dh)	**REG15240D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15240Eh)	**REG15240E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152411h ~ 152413h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152414h)	**REG152414**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh	**REG152416**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152416h)	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152417h)	**REG152417**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152416h'.	
0Ch (152418h)	**REG152418**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152419h)	**REG152419**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '152418h'.	
0Dh (15241Ah)	**REG15241A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15241Bh)	**REG15241B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15241Ch)	**REG15241C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15241Dh)	**REG15241D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (15241Eh)	**REG15241E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152420h)	**REG152420**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152421h)	**REG152421**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152422h)	**REG152422**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152423h)	**REG152423**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152424h)	**REG152424**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152425h)	**REG152425**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh	**REG152436**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152436h)	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152437h)	**REG152437**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152436h'.	
1Ch (152438h)	**REG152438**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152439h)	**REG152439**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152438h'.	
1Dh (15243Ah)	**REG15243A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15243Bh)	**REG15243B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15243Ah'.	
1Eh (15243Ch)	**REG15243C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152458h ~ 152459h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15245Ah)	**REG15245A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh	**REG15245C**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15245Ch)	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (15245Eh)	**REG15245E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh (15245Fh)	**REG15245F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152460h)	**REG152460**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152461h)	**REG152461**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (152462h)	**REG152462**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152463h)	**REG152463**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152462h'.	
32h (152464h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152465h)	**REG152465**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152466h ~ 152467h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h	**REG152468**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152468h)	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152469h)	**REG152469**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152468h'.	
35h (15246Ah)	**REG15246A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152470h)	**REG152470**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (152471h)	**REG152471**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152470h'.	
39h (152472h)	**REG152472**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152473h)	**REG152473**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152472h'.	
3Ah	**REG152474**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P1_0 Register (Bank = 1524)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152474h)	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152475h)	**REG152475**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152474h'.	
3Bh (152476h)	**REG152476**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152477h)	**REG152477**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152476h'.	
3Ch (152478h)	**REG152478**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152479h)	**REG152479**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152478h'.	
3Dh (15247Ah)	**REG15247A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15247Bh)	**REG15247B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15247Ah'.	

SDIO20P1_1 Register (Bank = 1525)

SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152500h)	**REG152500**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152501h)	**REG152501**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152502h)	**REG152502**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152503h)	**REG152503**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152504h)	**REG152504**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152505h)	**REG152505**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (152506h)	**REG152506**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152507h)	**REG152507**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152506h'.	
04h (152508h)	**REG152508**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152509h)	**REG152509**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152508h'.	
05h (15250Ah)	**REG15250A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15250Dh)	**REG15250D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15250Eh)	**REG15250E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152511h ~ 152513h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152514h)	**REG152514**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (152516h)	**REG152516**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152517h)	**REG152517**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152516h'.	
0Ch (152518h)	**REG152518**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152519h)	**REG152519**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TR_BK_CNT[11:8]	3:0	See description of '152518h'.	
0Dh (15251Ah)	**REG15251A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15251Bh)	**REG15251B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15251Ch)	**REG15251C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15251Dh)	**REG15251D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (15251Eh)	**REG15251E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152520h)	**REG152520**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152521h)	**REG152521**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152522h)	**REG152522**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152523h)	**REG152523**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152524h)	**REG152524**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152525h)	**REG152525**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (152536h)	**REG152536**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152537h)	**REG152537**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152536h'.	
1Ch (152538h)	**REG152538**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152539h)	**REG152539**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152538h'.	
1Dh (15253Ah)	**REG15253A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15253Bh)	**REG15253B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15253Ah'.	
1Eh (15253Ch)	**REG15253C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152558h ~ 152559h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15255Ah)	**REG15255A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (15255Ch)	**REG15255C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (15255Eh)	**REG15255E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (15255Fh)	**REG15255F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152560h)	**REG152560**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152561h)	**REG152561**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h	**REG152562**	**7:0**	**Default : 0x00**	**Access : RO**

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152562h)	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152563h)	**REG152563**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152562h'.	
32h (152564h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152565h)	**REG152565**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152566h ~ 152567h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (152568h)	**REG152568**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152569h)	**REG152569**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152568h'.	
35h (15256Ah)	**REG15256A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152570h)	**REG152570**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h	**REG152571**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P1_1 Register (Bank = 1525)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152571h)	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152570h'.	
39h (152572h)	**REG152572**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152573h)	**REG152573**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152572h'.	
3Ah (152574h)	**REG152574**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152575h)	**REG152575**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152574h'.	
3Bh (152576h)	**REG152576**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152577h)	**REG152577**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152576h'.	
3Ch (152578h)	**REG152578**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152579h)	**REG152579**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152578h'.	
3Dh (15257Ah)	**REG15257A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15257Bh)	**REG15257B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15257Ah'.	

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SDIO20P1_2 Register (Bank = 1526)

SDIO20P1_2 Register (Bank = 1526)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (15261Eh)	**REG15261E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	

SDIO20P1_3 Register (Bank = 1527)

SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152700h)	**REG152700**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152701h)	**REG152701**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152702h)	**REG152702**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152703h)	**REG152703**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152704h)	**REG152704**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152705h)	**REG152705**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (152706h)	**REG152706**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152707h)	**REG152707**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152706h'.	
04h (152708h)	**REG152708**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152709h)	**REG152709**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152708h'.	
05h (15270Ah)	**REG15270A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15270Dh)	**REG15270D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15270Eh)	**REG15270E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152711h ~ 152713h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152714h)	**REG152714**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh	**REG152716**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P1_3 Register (Bank = 1527)

Index (Absolute)	Mnemonic	Bit	Description	
(152716h)	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152717h)	**REG152717**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152716h'.	
0Ch (152718h)	**REG152718**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152719h)	**REG152719**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '152718h'.	
0Dh (15271Ah)	**REG15271A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15271Bh)	**REG15271B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15271Ch)	**REG15271C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15271Dh)	**REG15271D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (15271Eh)	**REG15271E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152720h)	**REG152720**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152721h)	**REG152721**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152722h)	**REG152722**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152723h)	**REG152723**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152724h)	**REG152724**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152725h)	**REG152725**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh	**REG152736**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152736h)	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152737h)	**REG152737**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152736h'.	
1Ch (152738h)	**REG152738**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152739h)	**REG152739**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152738h'.	
1Dh (15273Ah)	**REG15273A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15273Bh)	**REG15273B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15273Ah'.	
1Eh (15273Ch)	**REG15273C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152758h ~ 152759h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15275Ah)	**REG15275A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh	**REG15275C**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15275Ch)	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (15275Eh)	**REG15275E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh (15275Fh)	**REG15275F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152760h)	**REG152760**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152761h)	**REG152761**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (152762h)	**REG152762**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152763h)	**REG152763**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152762h'.	
32h (152764h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152765h)	**REG152765**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152766h ~ 152767h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h	**REG152768**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152768h)	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152769h)	**REG152769**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152768h'.	
35h (15276Ah)	**REG15276A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152770h)	**REG152770**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (152771h)	**REG152771**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152770h'.	
39h (152772h)	**REG152772**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152773h)	**REG152773**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152772h'.	
3Ah	**REG152774**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P1_3 Register (Bank = 1527)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152774h)	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152775h)	**REG152775**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152774h'.	
3Bh (152776h)	**REG152776**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152777h)	**REG152777**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152776h'.	
3Ch (152778h)	**REG152778**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152779h)	**REG152779**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152778h'.	
3Dh (15277Ah)	**REG15277A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15277Bh)	**REG15277B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15277Ah'.	

SDIO20P2_0 Register (Bank = 1528)

SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152800h)	**REG152800**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152801h)	**REG152801**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152802h)	**REG152802**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152803h)	**REG152803**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152804h)	**REG152804**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152805h)	**REG152805**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (152806h)	**REG152806**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152807h)	**REG152807**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152806h'.	
04h (152808h)	**REG152808**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152809h)	**REG152809**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152808h'.	
05h (15280Ah)	**REG15280A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15280Dh)	**REG15280D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15280Eh)	**REG15280E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152811h ~ 152813h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152814h)	**REG152814**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (152816h)	**REG152816**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152817h)	**REG152817**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152816h'.	
0Ch (152818h)	**REG152818**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152819h)	**REG152819**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TR_BK_CNT[11:8]	3:0	See description of '152818h'.	
0Dh (15281Ah)	**REG15281A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15281Bh)	**REG15281B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15281Ch)	**REG15281C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15281Dh)	**REG15281D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (15281Eh)	**REG15281E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152820h)	**REG152820**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152821h)	**REG152821**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152822h)	**REG152822**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152823h)	**REG152823**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152824h)	**REG152824**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152825h)	**REG152825**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (152836h)	**REG152836**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152837h)	**REG152837**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152836h'.	
1Ch (152838h)	**REG152838**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152839h)	**REG152839**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152838h'.	
1Dh (15283Ah)	**REG15283A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15283Bh)	**REG15283B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15283Ah'.	
1Eh (15283Ch)	**REG15283C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152858h ~ 152859h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15285Ah)	**REG15285A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (15285Ch)	**REG15285C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (15285Eh)	**REG15285E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (15285Fh)	**REG15285F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152860h)	**REG152860**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152861h)	**REG152861**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h	**REG152862**	**7:0**	**Default : 0x00**	**Access : RO**

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152862h)	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152863h)	**REG152863**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152862h'.	
32h (152864h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152865h)	**REG152865**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152866h ~ 152867h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (152868h)	**REG152868**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152869h)	**REG152869**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152868h'.	
35h (15286Ah)	**REG15286A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152870h)	**REG152870**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h	**REG152871**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_0 Register (Bank = 1528)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152871h)	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152870h'.	
39h (152872h)	**REG152872**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152873h)	**REG152873**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152872h'.	
3Ah (152874h)	**REG152874**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152875h)	**REG152875**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152874h'.	
3Bh (152876h)	**REG152876**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152877h)	**REG152877**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152876h'.	
3Ch (152878h)	**REG152878**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152879h)	**REG152879**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152878h'.	
3Dh (15287Ah)	**REG15287A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15287Bh)	**REG15287B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15287Ah'.	

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SDIO20P2_1 Register (Bank = 1529)

SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152900h)	**REG152900**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152901h)	**REG152901**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152902h)	**REG152902**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152903h)	**REG152903**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152904h)	**REG152904**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152905h)	**REG152905**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (152906h)	**REG152906**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152907h)	**REG152907**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152906h'.	
04h (152908h)	**REG152908**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h	**REG152909**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152909h)	DMA_ADDR_15_0[15:8]	7:0	See description of '152908h'.	
05h (15290Ah)	**REG15290A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (15290Dh)	**REG15290D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (15290Eh)	**REG15290E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152911h ~ 152913h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152914h)	**REG152914**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (152916h)	**REG152916**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152917h)	**REG152917**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152916h'.	
0Ch (152918h)	**REG152918**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152919h)	**REG152919**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '152918h'.	
0Dh (15291Ah)	**REG15291A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (15291Bh)	**REG15291B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (15291Ch)	**REG15291C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (15291Dh)	**REG15291D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh	**REG15291E**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15291Eh)	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152920h)	**REG152920**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152921h)	**REG152921**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152922h)	**REG152922**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152923h)	**REG152923**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152924h)	**REG152924**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152925h)	**REG152925**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (152936h)	**REG152936**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152937h)	**REG152937**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152936h'.	
1Ch (152938h)	**REG152938**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152939h)	**REG152939**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152938h'.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (15293Ah)	**REG15293A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (15293Bh)	**REG15293B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '15293Ah'.	
1Eh (15293Ch)	**REG15293C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152958h ~ 152959h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (15295Ah)	**REG15295A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (15295Ch)	**REG15295C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh	**REG15295E**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15295Eh)	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh (15295Fh)	**REG15295F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152960h)	**REG152960**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152961h)	**REG152961**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (152962h)	**REG152962**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152963h)	**REG152963**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152962h'.	
32h (152964h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152965h)	**REG152965**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152966h ~ 152967h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (152968h)	**REG152968**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152969h)	**REG152969**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152968h'.	
35h (15296Ah)	**REG15296A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (152970h)	**REG152970**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (152971h)	**REG152971**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152970h'.	
39h (152972h)	**REG152972**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152973h)	**REG152973**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152972h'.	
3Ah (152974h)	**REG152974**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152975h)	**REG152975**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152974h'.	
3Bh (152976h)	**REG152976**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152977h)	**REG152977**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152976h'.	
3Ch (152978h)	**REG152978**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152979h)	**REG152979**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152978h'.	

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SDIO20P2_1 Register (Bank = 1529)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (15297Ah)	**REG15297A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (15297Bh)	**REG15297B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '15297Ah'.	

SDIO20P2_2 Register (Bank = 152A)

SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152A00h)	**REG152A00**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152A01h)	**REG152A01**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152A02h)	**REG152A02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152A03h)	**REG152A03**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152A04h)	**REG152A04**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152A05h)	**REG152A05**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (152A06h)	**REG152A06**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152A07h)	**REG152A07**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152A06h'.	
04h (152A08h)	**REG152A08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152A09h)	**REG152A09**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152A08h'.	
05h (152A0Ah)	**REG152A0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (152A0Dh)	**REG152A0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (152A0Eh)	**REG152A0E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152A11h ~ 152A13h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152A14h)	**REG152A14**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh	**REG152A16**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152A16h)	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152A17h)	**REG152A17**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152A16h'.	
0Ch (152A18h)	**REG152A18**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152A19h)	**REG152A19**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '152A18h'.	
0Dh (152A1Ah)	**REG152A1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (152A1Bh)	**REG152A1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (152A1Ch)	**REG152A1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (152A1Dh)	**REG152A1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (152A1Eh)	**REG152A1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152A20h)	**REG152A20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152A21h)	**REG152A21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152A22h)	**REG152A22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152A23h)	**REG152A23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152A24h)	**REG152A24**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152A25h)	**REG152A25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh	**REG152A36**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152A36h)	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152A37h)	**REG152A37**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152A36h'.	
1Ch (152A38h)	**REG152A38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152A39h)	**REG152A39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152A38h'.	
1Dh (152A3Ah)	**REG152A3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (152A3Bh)	**REG152A3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '152A3Ah'.	
1Eh (152A3Ch)	**REG152A3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152A58h ~ 152A59h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (152A5Ah)	**REG152A5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh	**REG152A5C**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152A5Ch)	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (152A5Eh)	**REG152A5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	
2Fh (152A5Fh)	**REG152A5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152A60h)	**REG152A60**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152A61h)	**REG152A61**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (152A62h)	**REG152A62**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152A63h)	**REG152A63**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152A62h'.	
32h (152A64h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152A65h)	**REG152A65**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152A66h ~ 152A67h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h	**REG152A68**	**7:0**	**Default : 0xFF**	**Access : R/W**

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152A68h)	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152A69h)	**REG152A69**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152A68h'.	
35h (152A6Ah)	**REG152A6A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152A70h)	**REG152A70**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (152A71h)	**REG152A71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152A70h'.	
39h (152A72h)	**REG152A72**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152A73h)	**REG152A73**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152A72h'.	
3Ah	**REG152A74**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_2 Register (Bank = 152A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152A74h)	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152A75h)	**REG152A75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152A74h'.	
3Bh (152A76h)	**REG152A76**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152A77h)	**REG152A77**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152A76h'.	
3Ch (152A78h)	**REG152A78**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152A79h)	**REG152A79**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152A78h'.	
3Dh (152A7Ah)	**REG152A7A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (152A7Bh)	**REG152A7B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '152A7Ah'.	

SDIO20P2_3 Register (Bank = 152B)

SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (152B00h)	**REG152B00**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (152B01h)	**REG152B01**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT	7	Boot Operation Done interrupt event.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (152B02h)	**REG152B02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (152B03h)	**REG152B03**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOOT_DONE_INT_EN	7	EMMC Boot Operation Done interrupt enable.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (152B04h)	**REG152B04**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (152B05h)	**REG152B05**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_CLK_FREE	7	Set dynamic clock miu as free run clock.	
	MIU_CLK_CTL_SW	6	Select MIU dynamic clock source. 1: By SW. 0: By HW.	
	-	5	Reserved.	
	MIU_CLK_EN_SW	4	Enable MIU dynamic clock by SW. 1: Enable. 0: Disable.	
	-	3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (152B06h)	**REG152B06**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (152B07h)	**REG152B07**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '152B06h'.	
04h (152B08h)	**REG152B08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (152B09h)	**REG152B09**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '152B08h'.	
05h (152B0Ah)	**REG152B0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
06h (152B0Dh)	**REG152B0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (152B0Eh)	**REG152B0E**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
08h ~ 09h (152B11h ~ 152B13h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah (152B14h)	**REG152B14**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (152B16h)	**REG152B16**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit : sector. SDIO & Nand unit : reg_sdio_blk_size9_0).	
0Bh (152B17h)	**REG152B17**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '152B16h'.	
0Ch (152B18h)	**REG152B18**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (152B19h)	**REG152B19**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TR_BK_CNT[11:8]	3:0	See description of '152B18h'.	
0Dh (152B1Ah)	**REG152B1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (152B1Bh)	**REG152B1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (152B1Ch)	**REG152B1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (152B1Dh)	**REG152B1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue, Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (152B1Eh)	**REG152B1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (152B20h)	**REG152B20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (152B21h)	**REG152B21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port , when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (152B22h)	**REG152B22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (152B23h)	**REG152B23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_DET_INT_NOCLK	4	SDIO interrupt source need SDIO host clk output enable, 0- need SDIO host clk output enable, 1- no need SDIO host clk output enable.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1, 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (152B24h)	**REG152B24**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (152B25h)	**REG152B25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (152B36h)	**REG152B36**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400 : 1024 bytes.	
1Bh (152B37h)	**REG152B37**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '152B36h'.	
1Ch (152B38h)	**REG152B38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (152B39h)	**REG152B39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '152B38h'.	
1Dh (152B3Ah)	**REG152B3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (152B3Bh)	**REG152B3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '152B3Ah'.	
1Eh (152B3Ch)	**REG152B3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
2Ch ~ 2Ch (152B58h ~ 152B59h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Dh (152B5Ah)	**REG152B5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIU_WDEN_PATCH_DIS	7	Disable miu wden patch.	
	-	6:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (152B5Ch)	**REG152B5C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
2Fh (152B5Eh)	**REG152B5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BOOT_FROM_EMMC	2	Enable eMMC Boot operation.	
	BOOT_END_EN	1	EMMC boot end enable.	
	BOOT_ST2_EN	0	EMMC boot stage2 enable.	

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (152B5Fh)	**REG152B5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLKOE_DELAY_EN	5	Delay sd_clkoe for timing issue.	
	FROM_TMUX	4	SD bus to/from TMUX directly.	
	SD_SDRIN_BYPASS	3	Enalbe SD Data/CMD in bypass mode.	
	SD_BYPASS_MODE	2	Enalbe SD Bypass mode.	
	SD_DDR_MODE	1	Enalbe SD DDR mode.	
	MACRO_EN	0	Enalbe flash macro interface.	
30h (152B60h)	**REG152B60**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (152B61h)	**REG152B61**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h	**REG152B62**	**7:0**	**Default : 0x00**	**Access : RO**

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152B62h)	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (152B63h)	**REG152B63**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '152B62h'.	
32h (152B64h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
32h (152B65h)	**REG152B65**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
33h ~ 33h (152B66h ~ 152B67h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (152B68h)	**REG152B68**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (152B69h)	**REG152B69**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '152B68h'.	
35h (152B6Ah)	**REG152B6A**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h (152B70h)	**REG152B70**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h	**REG152B71**	**7:0**	**Default : 0x00**	**Access : R/W**

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SDIO20P2_3 Register (Bank = 152B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(152B71h)	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152B70h'.	
39h (152B72h)	**REG152B72**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (152B73h)	**REG152B73**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152B72h'.	
3Ah (152B74h)	**REG152B74**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (152B75h)	**REG152B75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '152B74h'.	
3Bh (152B76h)	**REG152B76**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (152B77h)	**REG152B77**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '152B76h'.	
3Ch (152B78h)	**REG152B78**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (152B79h)	**REG152B79**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '152B78h'.	
3Dh (152B7Ah)	**REG152B7A**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address, MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (152B7Bh)	**REG152B7B**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '152B7Ah'.	

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UART3 Register (Bank = 1530)

UART3 Register (Bank = 1530)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (153000h)	**REG153000**	**7:0**	**Default : 0x00**	**Access : R/W**
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; Note that Writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; Note that any incoming data are lost whenFIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (153004h)	**REG153004**	**7:0**	**Default : 0x00**	**Access : R/W**
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Boud rate = (serial clock freq.) / (16 * divisor).	
04h	**REG153008**	**7:0**	**Default : 0x00**	**Access : R/W**

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UART3 Register (Bank = 1530)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153008h)	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00" - FIFO empty; "01" - 2 characters in the FIFO; "10" - FIFO 1/4 full; "11" - FIFO 1/2 full; Bit [7:6]: Receiver FIFO Interrupt trigger level. "00" - 1 character in the FIFO; "01" - FIFO 1/4 full; "10" - FIFO 1/2 full; "11" - FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt idenfy. "110" - character timeout. "011" - Receiver Line Status. "010" - Receiver Data Available. "001" - Transmitter Holding Register empty. "000" - Modem Status.	
06h (15300Ch)	**REG15300C**	**7:0**	**Default : 0x03**	**Access : R/W**
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.	
	-	6:5	Reserved.	
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.	
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.	
	LCR_STOP_BITS	2	Specify the number of stop bits. "0" - 1 stop bit; "1" - 1.5 stop bits when 5-bit character length selected and 2 bits otherwise.	
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00" - 5 bits; "01" - 6 bits; "10" - 7 bits; "11" - 8 bits.	

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UART3 Register (Bank = 1530)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (153010h)	**REG153010**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN. RTS-> CTS.	
	-	3:2	Reserved.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0" - RTS is "1"; "1" - RTS is "0".	
	-	0	Reserved.	
0Ah (153014h)	**REG153014**	**7:0**	**Default : 0x00**	**Access : RO**
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO;	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO; Gen a Transmitter Holding Register Empty interrupt.	
	-	4	Reserved.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (153018h)	**REG153018**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	-	3:1	Reserved.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1" - the "CTS" line has changed its state. Clear when reading;	

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UART3 Register (Bank = 1530)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (15301Ch)	**REG15301C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	USR_BUSY	0	UART busy.	
14h (153028h)	**REG153028**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RSTZ	0	Software reset UART; 0: enable.	

URDMA1 Register (Bank = 1531)

URDMA1 Register (Bank = 1531)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (153100h)	**REG153100**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_SW_RST	7	RX Engine software reset. 0: De-assert. 1: Assert.	
	TX_SW_RST	6	TX Engine software reset. 0: De-assert. 1: Assert.	
	RX_ENDINA	5	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	TX_ENDINA	4	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	RX_URDMA_EN	3	URDMA RX Hardware Enable. 0: Disable. 1: Enable.	
	TX_URDMA_EN	2	URDMA TX Hardware Enable. 0: Disable. 1: Enable.	
	URDMA_MODE	1	URDMA Mode selects, when mode enable, URDMA hardware will replace MCU to access UART, otherwise MCU still control UART directly. 0: Disable. 1: Enable.	

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URDMA1 Register (Bank = 1531)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SW_RST	0	URDMA software reset. 0: De-assert. 1: Assert.	
00h (153101h)	**REG153101**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	RX_BUSY	5	RX controller in BUSY state.	
	TX_BUSY	4	TX controller in BUSY state.	
	RX_OP_MODE	3	RX controller operation mode. 0: Default. 1: Stop RX DMA activity when threshold interrupt occurs, until update RX_BUF_BASE.	
	-	2:0	Reserved.	
01h (153102h)	**REG153102**	**7:0**	**Default : 0x40**	**Access : R/W**
	INTR_THRESHOLD[7:0]	7:0	Interrupt threshold, to configure interrupt MCU period. Setting how much. Data received from UART, and alert MCU, byte unit.	
01h (153103h)	**REG153103**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INTR_THRESHOLD[11:8]	3:0	See description of '153102h'.	
02h (153104h)	**REG153104**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_H[7:0]	7:0	Configure TX buffer base address[26:16] in DRAM, 8byte unit.	
02h (153105h)	**REG153105**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TX_BUF_BASE_H[10:8]	2:0	See description of '153104h'.	
03h (153106h)	**REG153106**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[7:0]	7:0	Configure TX buffer base address[15:0] in DRAM, 8byte unit.	
03h (153107h)	**REG153107**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[15:8]	7:0	See description of '153106h'.	
04h (153108h)	**REG153108**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_SIZE[7:0]	7:0	Configure TX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
04h	**REG153109**	**7:0**	**Default : 0x00**	**Access : R/W**

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URDMA1 Register (Bank = 1531)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153109h)	-	7:5	Reserved.	
	TX_BUF_SIZE[12:8]	4:0	See description of '153108h'.	
05h (15310Ah)	**REG15310A**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[7:0]	7:0	Read TX buffer read pointer from URDMA, byte unit.	
05h (15310Bh)	**REG15310B**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[15:8]	7:0	See description of '15310Ah'.	
06h (15310Ch)	**REG15310C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[7:0]	7:0	Update TX buffer write pointer to URDMA, byte unit.	
06h (15310Dh)	**REG15310D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[15:8]	7:0	See description of '15310Ch'.	
07h (15310Eh)	**REG15310E**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	TX_TIMEOUT[3:0]	3:0	Configure TX time out value, to clean TX buffer data and send to UART. 2^(TX_TIMEOUT) Cycle unit.	
08h (153110h)	**REG153110**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_H[7:0]	7:0	Configure RX buffer base address[26:16] in DRAM, 8byte unit.	
08h (153111h)	**REG153111**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RX_BUF_BASE_H[10:8]	2:0	See description of '153110h'.	
09h (153112h)	**REG153112**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[7:0]	7:0	Configure RX buffer base address[15:0] in DRAM, 8byte unit.	
09h (153113h)	**REG153113**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[15:8]	7:0	See description of '153112h'.	
0Ah (153114h)	**REG153114**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_SIZE[7:0]	7:0	Configure RX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
0Ah (153115h)	**REG153115**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RX_BUF_SIZE[12:8]	4:0	See description of '153114h'.	
0Bh	**REG153116**	**7:0**	**Default : 0x00**	**Access : RO**

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URDMA1 Register (Bank = 1531)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153116h)	RX_BUF_WPTR[7:0]	7:0	Read RX buffer write pointer from URDMA, byte unit.	
0Bh (153117h)	**REG153117**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[15:8]	7:0	See description of '153116h'.	
0Ch (153118h)	**REG153118**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	RX_TIMEOUT[3:0]	3:0	Configure RX time out value, to clean UART RX FIFO and write to DRAM. 2^(RX_TIMEOUT) Cycle unit.	
0Dh (15311Ah)	**REG15311A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RX_MCU_INTR	7	Identify rx controller to MCU interrupt event, this bit is logical OR of RX_INTR1~2 flag, and clear by RX_INTR_CLR.	
	RESERVE2	6	Reserve.	
	RX_INTR2	5	Identify Rx interrupt is cause by interrupt threshold function.	
	RX_INTR1	4	Identify Rx interrupt is cause by timeout function.	
	RESERVE1	3	Reserve.	
	RX_INTR2_EN	2	Rx interrupt threshold function enable.	
	RX_INTR1_EN	1	Rx timeout interrupt function enable.	
	RX_INTR_CLR	0	MCU clear rx control interrupt signal. Once write and auto clear.	
0Dh (15311Bh)	**REG15311B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TX_MCU_INTR	7	Identify tx controller to MCU interrupt event.	
	RESERVE3[4:0]	6:2	Reserve.	
	TX_INTR_EN	1	TX controller to MCU interrupt enable.	
	TX_INTR_CLR	0	MCU clear tx control interrupt signal. Once write and auto clear.	
0Eh (15311Ch)	**REG15311C**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[7:0]	7:0	Reserve.	
0Eh (15311Dh)	**REG15311D**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE4[15:8]	7:0	See description of '15311Ch'.	
0Fh (15311Eh)	**REG15311E**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[7:0]	7:0	Reserve.	
0Fh (15311Fh)	**REG15311F**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE5[15:8]	7:0	See description of '15311Eh'.	

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URDMA1 Register (Bank = 1531)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (153120h)	**REG153120**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	RESERVE6[4:0]	7:3	Reserve.	
	PREFCH_CLK_GATE1	2	Gated clock MINF post-write module. 0: Clock enable. 1: Clock gated.	
	PREFCH_CLK_GATE	1	Gated clock MINF pre-fetch module. 0: Clock enable. 1: Clock gated.	
	MINF_SW_RSTZ	0	MINF pre-fetch / post-write module SW reset. 0: SW reset. 1: Normal.	
10h (153121h)	**REG153121**	**7:0**	**Default : 0x00**	**Access : RO**
	POSTWR_BUSY	7	Identify MINF post write in busy state.	
	RESERVE6[11:5]	6:0	See description of '153120h'.	
11h (153122h)	**REG153122**	**7:0**	**Default : 0x46**	**Access : R/W**
	PREFCH_PATCH	7	SW patch control bit.	
	PREFCH_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	PREFCH_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	PREFCH_PRI	3	Define DRAM access priority.	
	PREFCH_RASTRD	2	MINF pre-fetch fast read enable.	
	PREFCH_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	PREFCH_CLR	0	SW clear MINF pre-fetch buffer. 0: Normal. 1: Clear.	
11h (153123h)	**REG153123**	**7:0**	**Default : 0x46**	**Access : R/W**
	POSTWR_FLUSH1_PATCH	7	SW flush path.	

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URDMA1 Register (Bank = 1531)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	POSTWR_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.
	POSEWR_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.
	POSTWR_PRI	3	Define DRAM access priority.
	POSTWR_FLUSH1	2	SW flush path.
	POSTWR_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.
	POSTWR_FLUSH	0	SW flush MINF post write buffer. 0: Normal. 1: Flush.

IMI Register (Bank = 1532)

IMI Register (Bank = 1532)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (153200h)	**REG153200**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	SET_PRIORITY	3	Set client priority when disable round robin. 0: Use round robin. 1: Set client priority.	
	ROUND_ROBIN	2	Enable round robin algorithm. 0: Disable round robin. 1: Enable round robin.	
	INIT_DONE	1	Enable imi module. 0: Disable. 1: Enable.	
	SYS_RST_CTRL0	0	Imi module software reset. 0: Reset. 1: Not reset.	
00h	**REG153201**	**7:0**	**Default : 0x00**	**Access : R/W**

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IMI Register (Bank = 1532)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153201h)	CKG_MIU[1:0]	7:6	Arbiter clock enable and inverse. [14] 1:enable 0:disable. [15] 1:inv 0: not inverse.	
	-	5:0	Reserved.	
01h (153202h)	**REG153202**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_PRIORITY[3:0]	7:4	Client1 priority range 0~7.	
	RQ0_PRIORITY[3:0]	3:0	Client0 priority range 0~7.	
01h (153203h)	**REG153203**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_PRIORITY[3:0]	7:4	Client3 priority range 0~7.	
	RQ2_PRIORITY[3:0]	3:0	Client2 priority range 0~7.	
02h (153204h)	**REG153204**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ5_PRIORITY[3:0]	7:4	Client5 priority range 0~7.	
	RQ4_PRIORITY[3:0]	3:0	Client4 priority range 0~7.	
02h (153205h)	**REG153205**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ7_PRIORITY[3:0]	7:4	Client7 priority range 0~7.	
	RQ6_PRIORITY[3:0]	3:0	Client6 priority range 0~7.	
05h (15320Ah)	**REG15320A**	**7:0**	**Default : 0x7E**	**Access : R/W**
	RQ_MASK[7:0]	7:0	[7:0] client 7~0 request mask. 1: Masked. 0: Not masked. . [15:8] reserved.	
05h (15320Bh)	**REG15320B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ_MASK[15:8]	7:0	See description of '15320Ah'.	
06h (15320Ch)	**REG15320C**	**7:0**	**Default : 0x7E**	**Access : R/W**
	RQ_HPMASK[7:0]	7:0	[7:0] client 7~0 request mask while client's high priority bit is high. 1: Masked. 0: Not masked. . [15:8] reserved.	
06h (15320Dh)	**REG15320D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ_HPMASK[15:8]	7:0	See description of '15320Ch'.	

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ASIC Register (Bank = 1536)

ASIC Register (Bank = 1536)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (153620h)	**REG153620**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_0[7:0]	7:0	Dummy register bank0.	
10h (153621h)	**REG153621**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_0[15:8]	7:0	See description of '153620h'.	
11h (153622h)	**REG153622**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_1[7:0]	7:0	Dummy register bank1.	
11h (153623h)	**REG153623**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_1[15:8]	7:0	See description of '153622h'.	
12h (153624h)	**REG153624**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_2[7:0]	7:0	Dummy register bank2.	
12h (153625h)	**REG153625**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_2[15:8]	7:0	See description of '153624h'.	
13h (153626h)	**REG153626**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_3[7:0]	7:0	Dummy register bank3.	
13h (153627h)	**REG153627**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_3[15:8]	7:0	See description of '153626h'.	
14h (153628h)	**REG153628**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_4[7:0]	7:0	Dummy register bank4.	
14h (153629h)	**REG153629**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_4[15:8]	7:0	See description of '153628h'.	
15h (15362Ah)	**REG15362A**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_5[7:0]	7:0	Dummy register bank5.	
15h (15362Bh)	**REG15362B**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_5[15:8]	7:0	See description of '15362Ah'.	
16h (15362Ch)	**REG15362C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_6[7:0]	7:0	Dummy register bank6.	
16h (15362Dh)	**REG15362D**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_6[15:8]	7:0	See description of '15362Ch'.	
17h (15362Eh)	**REG15362E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_7[7:0]	7:0	Dummy register bank7.	
17h (15362Fh)	**REG15362F**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIC_DUMMY_7[15:8]	7:0	See description of '15362Eh'.	

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ASIC Register (Bank = 1536)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Eh (1536FCh)	**REG1536FC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DEBUG_SEL[7:0]	7:0	Debug port select.	

CPU Register (Bank = 1538)

CPU Register (Bank = 1538)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (153810h)	**REG153810**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_BT_AU_MAC[3:0]	7:4	[0]: Gating; [1]: Inv; [2]: Select fast;	
	CKG_BT_AU_SRC[3:0]	3:0	[0]: Gating; [1]: Inv; [2]: Select fast;	
08h (153811h)	**REG153811**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_BT_SPI[3:0]	3:0	[0]: Gating; [1]: Inv; [2]: Select fast;	
09h (153812h)	**REG153812**	**7:0**	**Default : 0x17**	**Access : R/W**
	-	7:5	Reserved.	
	CKM_BT_AU_SRC	4	0: 26M in->130Mhz, 38.4M in->120Mhz. 1: 109Mhz.	
	-	3	Reserved.	
	GATE_32K_BT	2	Gating clk_32k_bt.	
	GATE_APB_BT	1	Gating clk_apb_bt.	
	GATE_EMI_BT	0	Gating clk_emi_bt.	
09h (153813h)	**REG153813**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	CKM_BT_AU_MAC	0	0: 26M in->130Mhz, 38.4M in->120Mhz. 1: 109Mhz.	
0Ch	**REG153818**	**7:0**	**Default : 0x10**	**Access : R/W**

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CPU Register (Bank = 1538)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153818h)	CKG_SIGP[3:0]	7:4	[0]: Gating; [1]: Inv; [2]: Select fast;	
	CKM_SIGP[3:0]	3:0	[1:0]: 0: 26M in->35.86Mhz, 38.4M in->33.1Mhz. 1: 26M in-> 26M, 38.4M in->38.4Mhz. 2: 34.9Mhz. [2]: 0: 2khz, 1: 26M in-> 26M, 38.4M in->38.4Mhz (test mode if 2khz clock is not available). [3]: 0: clk_sigp, 1: 2k hz.	
0Ch (153819h)	**REG153819**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_SIGP_DMA_WR[3:0]	7:4	[0]: Gating; [1]: Inv; [2]: Select fast;	
	CKG_SIGP_DMA_RD[3:0]	3:0	[0]: Gating; [1]: Inv; [2]: Select fast;	
0Dh (15381Ah)	**REG15381A**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKM_TCXO	7	0: From PAD. 1: From XTAL.	
	CKG_TCXO[2:0]	6:4	[0]: Gating; [1]: Inv; [2]: Select fast;	
	CKG_AFE_GPS[3:0]	3:0	[0]: Gating; [1]: Inv; [2]: Select fast;	
0Dh (15381Bh)	**REG15381B**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_RFSPI[3:0]	7:4	[0]: Gating; [1]: Inv; [2]: Select fast;	
	CKG_16HZ[3:0]	3:0	[0]: Gating; [1]: Inv; [2]: Select fast;	
0Eh (15381Ch)	**REG15381C**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	GATE_AHB_GPS	1	Gating clk_ahb_gps.	
	GATE_EMI_GPS	0	Gating clk_emi_gps.	
10h	**REG153820**	**7:0**	**Default : 0x11**	**Access : R/W**

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CPU Register (Bank = 1538)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153820h)	CKG_WLAN_BCN[3:0]	7:4	[0]: Gating; [1]: Inv; [2]: Select fast;	
	CKG_WLAN[3:0]	3:0	[0]: Gating; [1]: Inv; [2]: Select fast;	
10h (153821h)	**REG153821**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_DAC[3:0]	3:0	[0]: Gating; [1]: Inv; [2]: Select fast;	
11h (153822h)	**REG153822**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	GATE_EMI_WLAN	0	Gating clk_emi_wlan.	
22h (153844h)	**REG153844**	**7:0**	**Default : 0x37**	**Access : R/W**
	-	7:6	Reserved.	
	GATE_APB_TMR	5	Gate clk_apb_tmr.	
	GATE_SLOW_TMR	4	Gate clk_slow_tmr.	
	CKG_FAST_TMR[1:0]	3:2	[0]: Gating; [1]: Inv;	
	CKM_FAST_TMR	1	0: 32k, 1: 26M/38.4M.	
	GATE_APB_WDT	0	0: Clk_live, 1: clk_rtc.	
22h (153845h)	**REG153845**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GATE_EMI_IARB	7	Gating clk_emi_iarb.	
	GATE_EMI_EARB	6	Gating clk_emi_earb.	
	GATE_APB_AHB2APB1	5	Gate clk_apb_ahb2apb1.	
	GATE_AHB_AHB2APB1	4	Gate clk_ahb_ahb2apb1.	
	GATE_APB_AHB2APB0	3	Gate clk_apb_ahb2apb0.	
	GATE_AHB_AHB2APB0	2	Gate clk_ahb_ahb2apb0.	
	GATE_APB_ROM_PU	1	Gate clk_apb_rom_pu.	
	GATE_AHB_ROM_PU	0	Gate clk_ahb_rom_pu.	
23h (153846h)	**REG153846**	**7:0**	**Default : 0x01**	**Access : R/W**
	GATE_AHB_CRB	7	Gating clk_ahb_crb.	
	GATE_XIU_CM2RB	6	Gating clk_xiu_cm2rb.	

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CPU Register (Bank = 1538)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GATE_AHB_CM2RB	5	Gating clk_ahb_cm2rb.	
	GATE_XIU_MIPS2CM	4	Gating clk_xiu_db2cm.	
	GATE_AHB_MIPS2CM	3	Gating clk_ahb_db2cm.	
	GATE_AHB_DB2CM	2	Gating clk_ahb_db2cm.	
	GATE_DB_BUS_DB2CM	1	Gating clk_db_bus_db2cm.	
	GATE_AHB_IMC	0	Gating clk_ahb_imc.	
23h (153847h)	**REG153847**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	GATE_AHB_CM2IMI	5	Gating clk_ahb_cm2imi.	
	GATE_AHB_CM2EMI	4	Gating clk_ahb_cm2emi.	
	GATE_AHB_CM	3	Gating clk_ahb_cm.	
	GATE_AHB_R2	2	Gating clk_ahb_r2.	
	GATE_AHB_CM2W	1	Gating clk_ahb_cm2w.	
	GATE_XIU_CRB	0	Gating clk_xiu_crb.	
24h (153848h)	**REG153848**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:5	Reserved.	
	DYN_FORCE_ON	4	Force clock on.	
	DYN_DLY_AMT[3:0]	3:0	Delay amount.	
25h (15384Ah)	**REG15384A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DCG_COMBO_MEA_START[1:0]	1:0	Start DCG measure.	
26h (15384Ch)	**REG15384C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCG_COMBO_MEA_CTRL0[7:0]	7:0	DCG Ctrl: [3:0] clk_en source selection: #7 all. #6 earb. #5 iarb. #4 cpu_mreq. #3 wlan+bt+gps. #2 wlan. #1 bt. #0 gps. [7:4]: cycle selection = 2^(n + 9). [14:8]: cycle match. [15]: Max_result.	

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CPU Register (Bank = 1538)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
26h (15384Dh)	**REG15384D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCG_COMBO_MEA_CTRL0[15:8]	7:0	See description of '15384Ch'.	
27h (15384Eh)	**REG15384E**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT0[7:0]	7:0	DCG measure result.	
27h (15384Fh)	**REG15384F**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT0[15:8]	7:0	See description of '15384Eh'.	
28h (153850h)	**REG153850**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT0[23:16]	7:0	See description of '15384Eh'.	
28h (153851h)	**REG153851**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT0[31:24]	7:0	See description of '15384Eh'.	
29h (153852h)	**REG153852**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCG_COMBO_MEA_CTRL1[7:0]	7:0	DCG Ctrl: [3:0] clk_en source selection: #7 all. #6 earb. #5 iarb. #4 cpu_mreq. #3 wlan+bt+gps. #2 wlan. #1 bt. #0 gps. [7:4]: cycle selection = 2^(n + 9). [14:8]: cycle match. [15]: Max_result.	
29h (153853h)	**REG153853**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCG_COMBO_MEA_CTRL1[15:8]	7:0	See description of '153852h'.	
2Ah (153854h)	**REG153854**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT1[7:0]	7:0	DCG measure result.	
2Ah (153855h)	**REG153855**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT1[15:8]	7:0	See description of '153854h'.	
2Bh (153856h)	**REG153856**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT1[23:16]	7:0	See description of '153854h'.	
2Bh (153857h)	**REG153857**	**7:0**	**Default : 0x00**	**Access : RO**
	DCG_COMBO_MEA_RESULT1[31:24]	7:0	See description of '153854h'.	
2Dh	**REG15385A**	**7:0**	**Default : 0x00**	**Access : R/W**

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CPU Register (Bank = 1538)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15385Ah)	-	7:3	Reserved.	
	GATE_TEST_R2	2	Gating clk_test_r2.	
	GATE_AHB_INT	1	Gating clk_ahb_int.	
	GATE_CPU_R2	0	Gating clk_cpu_r2.	
30h (153860h)	**REG153860**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	WATCHDOG_TIME_HALT	5	1/0= watchdog clock gating.	
	TIMERS_TIME_HALT	4	1/0= timer clock gating.	
	AHB2APB1_WRITE_BUFFER_ON	3	1/0= write buffer on/off.	
	AHB2APB1_READ_BUFFER_ON	2	1/0= read buffer on/off.	
	AHB2APB0_WRITE_BUFFER_ON	1	1/0= write buffer on/off.	
	AHB2APB0_READ_BUFFER_ON	0	1/0= read buffer on/off.	
31h (153862h)	**REG153862**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	SWRSTN_ROM_PU	3	Rom pu reset, low active.	
	SWRSTN_WATCHDOG	2	Watchdog reset, low active.	
	SWRSTN_FAST_TIMERS	1	Fast timer reset, low active.	
	SWRSTN_SLOW_TIMERS	0	Slow timer reset, low active.	
32h (153864h)	**REG153864**	**7:0**	**Default : 0x10**	**Access : R/W**
	APB_CLK_DIV_CFG[3:0]	7:4		
	-	3:2	Reserved.	
	CLK_APB_UPDATE_REQ_CFG	1	Update cpu0 derived clock div configuer.	
	AHB_DIV_DISABLE	0	0: Clk_apb=clk_ahb/2. 1: Clk_apb=clk_ahb.	
33h (153866h)	**REG153866**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROMBIST_WIDTH[3:0]	7:4	Byte number of a word; 4'h3 : 4 bytes.	
	-	3:2	Reserved.	
	ROMBIST_PD	1	Rom power down control.	
	ROMBIST_START	0		
34h (153868h)	**REG153868**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROMBIST_WORD[7:0]	7:0	Rom length (word number).	
34h (153869h)	**REG153869**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROMBIST_WORD[15:8]	7:0	See description of '153868h'.	

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CPU Register (Bank = 1538)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
35h (15386Ah)	**REG15386A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ROMBIST_DONE	0	Rom bist test done.	
36h (15386Ch)	**REG15386C**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CUR[7:0]	7:0	Rom bist current address.	
36h (15386Dh)	**REG15386D**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CUR[15:8]	7:0	See description of '15386Ch'.	
37h (15386Eh)	**REG15386E**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[7:0]	7:0	Rom bist signature.	
37h (15386Fh)	**REG15386F**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[15:8]	7:0	See description of '15386Eh'.	
38h (153870h)	**REG153870**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[23:16]	7:0	See description of '15386Eh'.	
38h (153871h)	**REG153871**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[31:24]	7:0	See description of '15386Eh'.	
39h (153872h)	**REG153872**	**7:0**	**Default : 0x01**	**Access : R/W**
	AHB_HPROT_PR[3:0]	7:4		
	-	3:2	Reserved.	
	AHB_INCR_WORDS[1:0]	1:0		
39h (153873h)	**REG153873**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RX_RST_ERR_WLAN	3	Wlan am_bridge_tx rst.	
	RX_RST_ERR_CPU	2	Cpu am_bridge_tx rst.	
	R2_INT_B14_SEL	1	Mux selection for bit14 of r2 interrupt source. 0: Emi_int. 1: Combo_bt_xtal_en_in.	
	R2_INT_B12_SEL	0	Mux selection for bit13 of r2 interrupt source. 0: Iarb_int. 1: Combo_bt_xtal_en_in.	
3Ah (153874h)	**REG153874**	**7:0**	**Default : 0x00**	**Access : RO**
	MREQ_STATUS[7:0]	7:0	Miu request status.	
3Ah (153875h)	**REG153875**	**7:0**	**Default : 0x00**	**Access : RO**
	MREQ_STATUS[15:8]	7:0	See description of '153874h'.	
40h	**REG153880**	**7:0**	**Default : 0x00**	**Access : R/W**

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CPU Register (Bank = 1538)

Index (Absolute)	Mnemonic	Bit	Description	
(153880h)	CPU_DUMMY_0[7:0]	7:0	Dummy register bank0.	
40h (153881h)	**REG153881**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_0[15:8]	7:0	See description of '153880h'.	
41h (153882h)	**REG153882**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_1[7:0]	7:0	Dummy register bank1.	
41h (153883h)	**REG153883**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_1[15:8]	7:0	See description of '153882h'.	
42h (153884h)	**REG153884**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_2[7:0]	7:0	Dummy register bank2.	
42h (153885h)	**REG153885**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_2[15:8]	7:0	See description of '153884h'.	
43h (153886h)	**REG153886**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_3[7:0]	7:0	Dummy register bank3.	
43h (153887h)	**REG153887**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_3[15:8]	7:0	See description of '153886h'.	
44h (153888h)	**REG153888**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_4[7:0]	7:0	Dummy register bank4.	
44h (153889h)	**REG153889**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_4[15:8]	7:0	See description of '153888h'.	
45h (15388Ah)	**REG15388A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_5[7:0]	7:0	Dummy register bank5.	
45h (15388Bh)	**REG15388B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_5[15:8]	7:0	See description of '15388Ah'.	
46h (15388Ch)	**REG15388C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_6[7:0]	7:0	Dummy register bank6.	
46h (15388Dh)	**REG15388D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_6[15:8]	7:0	See description of '15388Ch'.	
47h (15388Eh)	**REG15388E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_7[7:0]	7:0	Dummy register bank7.	
47h (15388Fh)	**REG15388F**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_DUMMY_7[15:8]	7:0	See description of '15388Eh'.	
7Eh (1538FCh)	**REG1538FC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DEBUG_SEL[7:0]	7:0	Debug port select.	

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VP6 Register (Bank = 1539)

VP6 Register (Bank = 1539)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (153900h)	**REG153900**	**7:0**	**Default : 0x00**	**Access : RO**
	REV_ID[7:0]	7:0	Revision ID. Version 1.1.	
00h (153901h)	**REG153901**	**7:0**	**Default : 0x00**	**Access : RO**
	REV_ID[15:8]	7:0	See description of '153900h'.	
01h (153902h)	**REG153902**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	-	7:5	Reserved.	
	DIS_MIU_RDY	4	1: Disable miu rdy. 0: Miu access normally.	
	-	3	Reserved.	
	HK_SWRST_FINISH	2	1: Hardware finish reset procedure. 0: Hardware is performing reset procedure.	
	-	1	Reserved.	
	HK_SWRST	0	Set this register to 1 will reset all hardware engine..	
01h (153903h)	**REG153903**	**7:0**	**Default : 0x00**	**Access : R/W**
	VP6_APB_SEL	7	1: MIPS. 0: VD_32BMCU.	
	-	6:0	Reserved.	
0Bh (153916h)	**REG153916**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX0_L[7:0]	7:0	Hi message box 0 low word.	
0Bh (153917h)	**REG153917**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX0_L[15:8]	7:0	See description of '153916h'.	
0Ch (153918h)	**REG153918**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX0_H[7:0]	7:0	Hi message box 0 low word.	
0Ch (153919h)	**REG153919**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX0_H[15:8]	7:0	See description of '153918h'.	
0Dh (15391Ah)	**REG15391A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX1_L[7:0]	7:0	Hi message box 1 low word.	
0Dh (15391Bh)	**REG15391B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX1_L[15:8]	7:0	See description of '15391Ah'.	
0Eh (15391Ch)	**REG15391C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX1_H[7:0]	7:0	Hi message box 1 low word.	

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VP6 Register (Bank = 1539)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (15391Dh)	**REG15391D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_MBOX1_H[15:8]	7:0	See description of '15391Ch'.	
0Fh (15391Eh)	**REG15391E**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	HI_MBOX0_SET	0	Hi message box 0 set.	
0Fh (15391Fh)	**REG15391F**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:2	Reserved.	
	HI_INT_SET	1	House keeping set interrupt to risc.	
	HI_MBOX1_SET	0	Hi message box 1 set.	
10h (153920h)	**REG153920**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	-	7	Reserved.	
	RISC_INT_MSK	6	Risc interrupt mask.	
	-	5:3	Reserved.	
	RISC_INT_CLR	2	Risc interrupt clear.	
	RISC_MBOX1_CLR	1	Risc message box 1 clear.	
	RISC_MBOX0_CLR	0	Risc message box 0 clear.	
10h (153921h)	**REG153921**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RISC_INT_FORCE	2	Risc interrupt force.	
	-	1:0	Reserved.	
11h (153922h)	**REG153922**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RISC_MBOX1_RDY	4	Risc message box 1 ready.	
	-	3:1	Reserved.	
	RISC_MBOX0_RDY	0	Risc message box 0 ready.	
11h (153923h)	**REG153923**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	RISC_INT_VALID	0	Risc interrupt ready.	
12h (153924h)	**REG153924**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	HI_MBOX0_RDY	0	Hi message box 0 ready.	
12h (153925h)	**REG153925**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	

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VP6 Register (Bank = 1539)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HI_INT_STATUS	1	House keeping interrupt status.	
	HI_MBOX1_RDY	0	Hi message box 1 ready.	
13h (153926h)	**REG153926**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX0_L[7:0]	7:0	Risc message box 0.	
13h (153927h)	**REG153927**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX0_L[15:8]	7:0	See description of '153926h'.	
14h (153928h)	**REG153928**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX0_H[7:0]	7:0	Risc message box 0.	
14h (153929h)	**REG153929**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX0_H[15:8]	7:0	See description of '153928h'.	
15h (15392Ah)	**REG15392A**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX1_L[7:0]	7:0	Risc message box 1.	
15h (15392Bh)	**REG15392B**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX1_L[15:8]	7:0	See description of '15392Ah'.	
16h (15392Ch)	**REG15392C**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX1_H[7:0]	7:0	Risc message box 1.	
16h (15392Dh)	**REG15392D**	**7:0**	**Default : 0x00**	**Access : RO**
	RISC_MBOX1_H[15:8]	7:0	See description of '15392Ch'.	
1Ah (153934h)	**REG153934**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_DUMMY_0[7:0]	7:0	Dummy cell.	
1Ah (153935h)	**REG153935**	**7:0**	**Default : 0x00**	**Access : R/W**
	HI_DUMMY_0[15:8]	7:0	See description of '153934h'.	

INTR_CTRL2 Register (Bank = 153B)

INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (153B00h)	**REG153B00**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst0; 0/1 : not force/force.	
00h (153B01h)	**REG153B01**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_15_0_[15:8]	7:0	See description of '153B00h'.	
01h	**REG153B02**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153B02h)	HST0_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst0; 0/1 : not force/force.	
01h (153B03h)	**REG153B03**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_31_16_[15:8]	7:0	See description of '153B02h'.	
02h (153B04h)	**REG153B04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst0; 0/1 : not force/force.	
02h (153B05h)	**REG153B05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_FORCE_47_32_[15:8]	7:0	See description of '153B04h'.	
03h (153B06h)	**REG153B06**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst0; 0/1 : not force/force.	
03h (153B07h)	**REG153B07**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_FORCE_63_48_[15:8]	7:0	See description of '153B06h'.	
04h (153B08h)	**REG153B08**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst0; 0/1: not mask/mask.	
04h (153B09h)	**REG153B09**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_15_0_[15:8]	7:0	See description of '153B08h'.	
05h (153B0Ah)	**REG153B0A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst0; 0/1: not mask/mask.	
05h (153B0Bh)	**REG153B0B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_31_16_[15:8]	7:0	See description of '153B0Ah'.	
06h (153B0Ch)	**REG153B0C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst0; 0/1: not mask/mask.	
06h (153B0Dh)	**REG153B0D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_47_32_[15:8]	7:0	See description of '153B0Ch'.	
07h (153B0Eh)	**REG153B0E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst0; 0/1: not mask/mask.	
07h (153B0Fh)	**REG153B0F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_FIQ_MASK_63_48_[15:8]	7:0	See description of '153B0Eh'.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (153B10h)	**REG153B10**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
08h (153B11h)	**REG153B11**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '153B10h'.	
09h (153B12h)	**REG153B12**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst0; 0/1: not reverse/reverse.	
09h (153B13h)	**REG153B13**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '153B12h'.	
0Ah (153B14h)	**REG153B14**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst0; 0/1: not reverse/reverse.	
0Ah (153B15h)	**REG153B15**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '153B14h'.	
0Bh (153B16h)	**REG153B16**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst0; 0/1: not reverse/reverse.	
0Bh (153B17h)	**REG153B17**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '153B16h'.	
0Ch (153B18h)	**REG153B18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst0; Write 1 to clear fiq interrupt[15:0] of hst0.	
0Ch (153B19h)	**REG153B19**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_15_0_[15:8]	7:0	See description of '153B18h'.	
0Dh (153B1Ah)	**REG153B1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst0; Write 1 to clear fiq interrupt[31:16] of hst0.	
0Dh (153B1Bh)	**REG153B1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_31_16_[15:8]	7:0	See description of '153B1Ah'.	
0Eh (153B1Ch)	**REG153B1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst0; Write 1 to clear fiq interrupt[47:32] of hst0.	
0Eh	**REG153B1D**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153B1Dh)	HST0_FIQ_STATUS_47_32_[15:8]	7:0	See description of '153B1Ch'.	
0Fh (153B1Eh)	**REG153B1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst0; Write 1 to clear fiq interrupt[63:48] of hst0.	
0Fh (153B1Fh)	**REG153B1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_FIQ_STATUS_63_48_[15:8]	7:0	See description of '153B1Eh'.	
10h (153B20h)	**REG153B20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst0; 0/1 : not force/force.	
10h (153B21h)	**REG153B21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_15_0_[15:8]	7:0	See description of '153B20h'.	
11h (153B22h)	**REG153B22**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst0; 0/1 : not force/force.	
11h (153B23h)	**REG153B23**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_31_16_[15:8]	7:0	See description of '153B22h'.	
12h (153B24h)	**REG153B24**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst0; 0/1 : not force/force.	
12h (153B25h)	**REG153B25**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_FORCE_47_32_[15:8]	7:0	See description of '153B24h'.	
13h (153B26h)	**REG153B26**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst0; 0/1 : not force/force.	
13h (153B27h)	**REG153B27**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_FORCE_63_48_[15:8]	7:0	See description of '153B26h'.	
14h (153B28h)	**REG153B28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst0; 0/1: not mask/mask.	
14h (153B29h)	**REG153B29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_15_0_[15:8]	7:0	See description of '153B28h'.	
15h (153B2Ah)	**REG153B2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst0; 0/1: not mask/mask.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (153B2Bh)	**REG153B2B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_31_16_[15:8]	7:0	See description of '153B2Ah'.	
16h (153B2Ch)	**REG153B2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst0; 0/1: not mask/mask.	
16h (153B2Dh)	**REG153B2D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_47_32_[15:8]	7:0	See description of '153B2Ch'.	
17h (153B2Eh)	**REG153B2E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst0; 0/1: not mask/mask.	
17h (153B2Fh)	**REG153B2F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST0_IRQ_MASK_63_48_[15:8]	7:0	See description of '153B2Eh'.	
18h (153B30h)	**REG153B30**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
18h (153B31h)	**REG153B31**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '153B30h'.	
19h (153B32h)	**REG153B32**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst0; 0/1: not reverse/reverse.	
19h (153B33h)	**REG153B33**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '153B32h'.	
1Ah (153B34h)	**REG153B34**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst0; 0/1: not reverse/reverse.	
1Ah (153B35h)	**REG153B35**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '153B34h'.	
1Bh (153B36h)	**REG153B36**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst0; 0/1: not reverse/reverse.	
1Bh (153B37h)	**REG153B37**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST0_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '153B36h'.	
1Ch (153B38h)	**REG153B38**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst0;	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (153B39h)	**REG153B39**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_15_0_[15:8]	7:0	See description of '153B38h'.	
1Dh (153B3Ah)	**REG153B3A**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst0;	
1Dh (153B3Bh)	**REG153B3B**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_31_16_[15:8]	7:0	See description of '153B3Ah'.	
1Eh (153B3Ch)	**REG153B3C**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst0;	
1Eh (153B3Dh)	**REG153B3D**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_47_32_[15:8]	7:0	See description of '153B3Ch'.	
1Fh (153B3Eh)	**REG153B3E**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst0;	
1Fh (153B3Fh)	**REG153B3F**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_63_48_[15:8]	7:0	See description of '153B3Eh'.	
20h (153B40h)	**REG153B40**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst1; 0/1 : not force/force.	
20h (153B41h)	**REG153B41**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_15_0_[15:8]	7:0	See description of '153B40h'.	
21h (153B42h)	**REG153B42**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst1; 0/1 : not force/force.	
21h (153B43h)	**REG153B43**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_31_16_[15:8]	7:0	See description of '153B42h'.	
22h (153B44h)	**REG153B44**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst1; 0/1 : not force/force.	
22h (153B45h)	**REG153B45**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_FORCE_47_32_[15:8]	7:0	See description of '153B44h'.	
23h (153B46h)	**REG153B46**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst1; 0/1 : not force/force.	
23h (153B47h)	**REG153B47**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_FORCE_63_48_[15:8]	7:0	See description of '153B46h'.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (153B48h)	**REG153B48**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst1; 0/1: not mask/mask.	
24h (153B49h)	**REG153B49**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_15_0_[15:8]	7:0	See description of '153B48h'.	
25h (153B4Ah)	**REG153B4A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst1; 0/1: not mask/mask.	
25h (153B4Bh)	**REG153B4B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_31_16_[15:8]	7:0	See description of '153B4Ah'.	
26h (153B4Ch)	**REG153B4C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst1; 0/1: not mask/mask.	
26h (153B4Dh)	**REG153B4D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_47_32_[15:8]	7:0	See description of '153B4Ch'.	
27h (153B4Eh)	**REG153B4E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst1; 0/1: not mask/mask.	
27h (153B4Fh)	**REG153B4F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_FIQ_MASK_63_48_[15:8]	7:0	See description of '153B4Eh'.	
28h (153B50h)	**REG153B50**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst1; 0/1: not reverse/reverse.	
28h (153B51h)	**REG153B51**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '153B50h'.	
29h (153B52h)	**REG153B52**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst1; 0/1: not reverse/reverse.	
29h (153B53h)	**REG153B53**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '153B52h'.	
2Ah (153B54h)	**REG153B54**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst1; 0/1: not reverse/reverse.	
2Ah	**REG153B55**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153B55h)	HST1_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '153B54h'.	
2Bh (153B56h)	**REG153B56**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst1; 0/1: not reverse/reverse.	
2Bh (153B57h)	**REG153B57**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '153B56h'.	
2Ch (153B58h)	**REG153B58**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst1; Write 1 to clear fiq interrupt[15:0] of hst1.	
2Ch (153B59h)	**REG153B59**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_15_0_[15:8]	7:0	See description of '153B58h'.	
2Dh (153B5Ah)	**REG153B5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst1; Write 1 to clear fiq interrupt[31:16] of hst1.	
2Dh (153B5Bh)	**REG153B5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_31_16_[15:8]	7:0	See description of '153B5Ah'.	
2Eh (153B5Ch)	**REG153B5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst1; Write 1 to clear fiq interrupt[47:32] of hst1.	
2Eh (153B5Dh)	**REG153B5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_47_32_[15:8]	7:0	See description of '153B5Ch'.	
2Fh (153B5Eh)	**REG153B5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst1; Write 1 to clear fiq interrupt[63:48] of hst1.	
2Fh (153B5Fh)	**REG153B5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_FIQ_STATUS_63_48_[15:8]	7:0	See description of '153B5Eh'.	
30h (153B60h)	**REG153B60**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst1; 0/1 : not force/force.	
30h (153B61h)	**REG153B61**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_15_0_[15:8]	7:0	See description of '153B60h'.	
31h (153B62h)	**REG153B62**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst1; 0/1 : not force/force.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
31h (153B63h)	**REG153B63**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_31_16_[15:8]	7:0	See description of '153B62h'.	
32h (153B64h)	**REG153B64**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst1; 0/1 : not force/force.	
32h (153B65h)	**REG153B65**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_FORCE_47_32_[15:8]	7:0	See description of '153B64h'.	
33h (153B66h)	**REG153B66**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst1; 0/1 : not force/force.	
33h (153B67h)	**REG153B67**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_FORCE_63_48_[15:8]	7:0	See description of '153B66h'.	
34h (153B68h)	**REG153B68**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst1; 0/1: not mask/mask.	
34h (153B69h)	**REG153B69**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_15_0_[15:8]	7:0	See description of '153B68h'.	
35h (153B6Ah)	**REG153B6A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst1; 0/1: not mask/mask.	
35h (153B6Bh)	**REG153B6B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_31_16_[15:8]	7:0	See description of '153B6Ah'.	
36h (153B6Ch)	**REG153B6C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst1; 0/1: not mask/mask.	
36h (153B6Dh)	**REG153B6D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_47_32_[15:8]	7:0	See description of '153B6Ch'.	
37h (153B6Eh)	**REG153B6E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst1; 0/1: not mask/mask.	
37h (153B6Fh)	**REG153B6F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST1_IRQ_MASK_63_48_[15:8]	7:0	See description of '153B6Eh'.	
38h	**REG153B70**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153B70h)	HST1_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst1; 0/1: not reverse/reverse.	
38h (153B71h)	**REG153B71**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '153B70h'.	
39h (153B72h)	**REG153B72**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst1; 0/1: not reverse/reverse.	
39h (153B73h)	**REG153B73**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '153B72h'.	
3Ah (153B74h)	**REG153B74**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst1; 0/1: not reverse/reverse.	
3Ah (153B75h)	**REG153B75**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '153B74h'.	
3Bh (153B76h)	**REG153B76**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst1; 0/1: not reverse/reverse.	
3Bh (153B77h)	**REG153B77**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST1_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '153B76h'.	
3Ch (153B78h)	**REG153B78**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst1;	
3Ch (153B79h)	**REG153B79**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_15_0_[15:8]	7:0	See description of '153B78h'.	
3Dh (153B7Ah)	**REG153B7A**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst1;	
3Dh (153B7Bh)	**REG153B7B**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_31_16_[15:8]	7:0	See description of '153B7Ah'.	
3Eh (153B7Ch)	**REG153B7C**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst1;	
3Eh (153B7Dh)	**REG153B7D**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_47_32_[15:8]	7:0	See description of '153B7Ch'.	
3Fh (153B7Eh)	**REG153B7E**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst1;	
3Fh	**REG153B7F**	**7:0**	**Default : 0x00**	**Access : RO**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153B7Fh)	HST1_IRQ_STATUS_63_48_[15:8]	7:0	See description of '153B7Eh'.	
40h (153B80h)	**REG153B80**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst2; 0/1 : not force/force.	
40h (153B81h)	**REG153B81**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_15_0_[15:8]	7:0	See description of '153B80h'.	
41h (153B82h)	**REG153B82**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst2; 0/1 : not force/force.	
41h (153B83h)	**REG153B83**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_31_16_[15:8]	7:0	See description of '153B82h'.	
42h (153B84h)	**REG153B84**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst2; 0/1 : not force/force.	
42h (153B85h)	**REG153B85**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_FORCE_47_32_[15:8]	7:0	See description of '153B84h'.	
43h (153B86h)	**REG153B86**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst2; 0/1 : not force/force.	
43h (153B87h)	**REG153B87**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_FORCE_63_48_[15:8]	7:0	See description of '153B86h'.	
44h (153B88h)	**REG153B88**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst2; 0/1: not mask/mask.	
44h (153B89h)	**REG153B89**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_15_0_[15:8]	7:0	See description of '153B88h'.	
45h (153B8Ah)	**REG153B8A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst2; 0/1: not mask/mask.	
45h (153B8Bh)	**REG153B8B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_31_16_[15:8]	7:0	See description of '153B8Ah'.	
46h (153B8Ch)	**REG153B8C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst2; 0/1: not mask/mask.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (153B8Dh)	**REG153B8D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_47_32_[15:8]	7:0	See description of '153B8Ch'.	
47h (153B8Eh)	**REG153B8E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst2; 0/1: not mask/mask.	
47h (153B8Fh)	**REG153B8F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_FIQ_MASK_63_48_[15:8]	7:0	See description of '153B8Eh'.	
48h (153B90h)	**REG153B90**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst2; 0/1: not reverse/reverse.	
48h (153B91h)	**REG153B91**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '153B90h'.	
49h (153B92h)	**REG153B92**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst2; 0/1: not reverse/reverse.	
49h (153B93h)	**REG153B93**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '153B92h'.	
4Ah (153B94h)	**REG153B94**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst2; 0/1: not reverse/reverse.	
4Ah (153B95h)	**REG153B95**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '153B94h'.	
4Bh (153B96h)	**REG153B96**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst2; 0/1: not reverse/reverse.	
4Bh (153B97h)	**REG153B97**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '153B96h'.	
4Ch (153B98h)	**REG153B98**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst2; Write 1 to clear fiq interrupt[15:0] of hst2.	
4Ch (153B99h)	**REG153B99**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_15_0_[15:8]	7:0	See description of '153B98h'.	
4Dh	**REG153B9A**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153B9Ah)	HST2_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst2; Write 1 to clear fiq interrupt[31:16] of hst2.	
4Dh (153B9Bh)	**REG153B9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_31_16_[15:8]	7:0	See description of '153B9Ah'.	
4Eh (153B9Ch)	**REG153B9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst2; Write 1 to clear fiq interrupt[47:32] of hst2.	
4Eh (153B9Dh)	**REG153B9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_47_32_[15:8]	7:0	See description of '153B9Ch'.	
4Fh (153B9Eh)	**REG153B9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst2; Write 1 to clear fiq interrupt[63:48] of hst2.	
4Fh (153B9Fh)	**REG153B9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_FIQ_STATUS_63_48_[15:8]	7:0	See description of '153B9Eh'.	
50h (153BA0h)	**REG153BA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst2; 0/1 : not force/force.	
50h (153BA1h)	**REG153BA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_15_0_[15:8]	7:0	See description of '153BA0h'.	
51h (153BA2h)	**REG153BA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst2; 0/1 : not force/force.	
51h (153BA3h)	**REG153BA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_31_16_[15:8]	7:0	See description of '153BA2h'.	
52h (153BA4h)	**REG153BA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst2; 0/1 : not force/force.	
52h (153BA5h)	**REG153BA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_FORCE_47_32_[15:8]	7:0	See description of '153BA4h'.	
53h (153BA6h)	**REG153BA6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst2; 0/1 : not force/force.	
53h (153BA7h)	**REG153BA7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_FORCE_63_48_[15:8]	7:0	See description of '153BA6h'.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
54h (153BA8h)	**REG153BA8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst2; 0/1: not mask/mask.	
54h (153BA9h)	**REG153BA9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_15_0_[15:8]	7:0	See description of '153BA8h'.	
55h (153BAAh)	**REG153BAA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst2; 0/1: not mask/mask.	
55h (153BABh)	**REG153BAB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_31_16_[15:8]	7:0	See description of '153BAAh'.	
56h (153BACh)	**REG153BAC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst2; 0/1: not mask/mask.	
56h (153BADh)	**REG153BAD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_47_32_[15:8]	7:0	See description of '153BACh'.	
57h (153BAEh)	**REG153BAE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst2; 0/1: not mask/mask.	
57h (153BAFh)	**REG153BAF**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST2_IRQ_MASK_63_48_[15:8]	7:0	See description of '153BAEh'.	
58h (153BB0h)	**REG153BB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst2; 0/1: not reverse/reverse.	
58h (153BB1h)	**REG153BB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '153BB0h'.	
59h (153BB2h)	**REG153BB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst2; 0/1: not reverse/reverse.	
59h (153BB3h)	**REG153BB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '153BB2h'.	
5Ah (153BB4h)	**REG153BB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst2; 0/1: not reverse/reverse.	
5Ah	**REG153BB5**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153BB5h)	HST2_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '153BB4h'.	
5Bh (153BB6h)	**REG153BB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst2; 0/1: not reverse/reverse.	
5Bh (153BB7h)	**REG153BB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST2_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '153BB6h'.	
5Ch (153BB8h)	**REG153BB8**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst2;	
5Ch (153BB9h)	**REG153BB9**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_15_0_[15:8]	7:0	See description of '153BB8h'.	
5Dh (153BBAh)	**REG153BBA**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst2;	
5Dh (153BBBh)	**REG153BBB**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_31_16_[15:8]	7:0	See description of '153BBAh'.	
5Eh (153BBCh)	**REG153BBC**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst2;	
5Eh (153BBDh)	**REG153BBD**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_47_32_[15:8]	7:0	See description of '153BBCh'.	
5Fh (153BBEh)	**REG153BBE**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst2;	
5Fh (153BBFh)	**REG153BBF**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_63_48_[15:8]	7:0	See description of '153BBEh'.	
60h (153BC0h)	**REG153BC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst3; 0/1 : not force/force.	
60h (153BC1h)	**REG153BC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_15_0_[15:8]	7:0	See description of '153BC0h'.	
61h (153BC2h)	**REG153BC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst3; 0/1 : not force/force.	
61h (153BC3h)	**REG153BC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_31_16_[15:8]	7:0	See description of '153BC2h'.	
62h	**REG153BC4**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153BC4h)	HST3_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst3; 0/1 : not force/force.	
62h (153BC5h)	**REG153BC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_FORCE_47_32_[15:8]	7:0	See description of '153BC4h'.	
63h (153BC6h)	**REG153BC6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63:48] to hst3; 0/1 : not force/force.	
63h (153BC7h)	**REG153BC7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_FORCE_63_48_[15:8]	7:0	See description of '153BC6h'.	
64h (153BC8h)	**REG153BC8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst3; 0/1: not mask/mask.	
64h (153BC9h)	**REG153BC9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_15_0_[15:8]	7:0	See description of '153BC8h'.	
65h (153BCAh)	**REG153BCA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst3; 0/1: not mask/mask.	
65h (153BCBh)	**REG153BCB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_31_16_[15:8]	7:0	See description of '153BCAh'.	
66h (153BCCh)	**REG153BCC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst3; 0/1: not mask/mask.	
66h (153BCDh)	**REG153BCD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_47_32_[15:8]	7:0	See description of '153BCCh'.	
67h (153BCEh)	**REG153BCE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63:48] for hst3; 0/1: not mask/mask.	
67h (153BCFh)	**REG153BCF**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_FIQ_MASK_63_48_[15:8]	7:0	See description of '153BCEh'.	
68h (153BD0h)	**REG153BD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst3; 0/1: not reverse/reverse.	
68h (153BD1h)	**REG153BD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '153BD0h'.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
69h (153BD2h)	**REG153BD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst3; 0/1: not reverse/reverse.	
69h (153BD3h)	**REG153BD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '153BD2h'.	
6Ah (153BD4h)	**REG153BD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst3; 0/1: not reverse/reverse.	
6Ah (153BD5h)	**REG153BD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '153BD4h'.	
6Bh (153BD6h)	**REG153BD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63:48] polarity for hst3; 0/1: not reverse/reverse.	
6Bh (153BD7h)	**REG153BD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '153BD6h'.	
6Ch (153BD8h)	**REG153BD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst3; Write 1 to clear fiq interrupt[15:0] of hst3.	
6Ch (153BD9h)	**REG153BD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_15_0_[15:8]	7:0	See description of '153BD8h'.	
6Dh (153BDAh)	**REG153BDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst3; Write 1 to clear fiq interrupt[31:16] of hst3.	
6Dh (153BDBh)	**REG153BDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_31_16_[15:8]	7:0	See description of '153BDAh'.	
6Eh (153BDCh)	**REG153BDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst3; Write 1 to clear fiq interrupt[47:32] of hst3.	
6Eh (153BDDh)	**REG153BDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_47_32_[15:8]	7:0	See description of '153BDCh'.	
6Fh (153BDEh)	**REG153BDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63:48] for hst3; Write 1 to clear fiq interrupt[63:48] of hst3.	
6Fh	**REG153BDF**	**7:0**	**Default : 0x00**	**Access : R/W**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153BDFh)	HST3_FIQ_STATUS_63_48_[15:8]	7:0	See description of '153BDEh'.	
70h (153BE0h)	**REG153BE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst3; 0/1 : not force/force.	
70h (153BE1h)	**REG153BE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_15_0_[15:8]	7:0	See description of '153BE0h'.	
71h (153BE2h)	**REG153BE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst3; 0/1 : not force/force.	
71h (153BE3h)	**REG153BE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_31_16_[15:8]	7:0	See description of '153BE2h'.	
72h (153BE4h)	**REG153BE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst3; 0/1 : not force/force.	
72h (153BE5h)	**REG153BE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_FORCE_47_32_[15:8]	7:0	See description of '153BE4h'.	
73h (153BE6h)	**REG153BE6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63:48] to hst3; 0/1 : not force/force.	
73h (153BE7h)	**REG153BE7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_FORCE_63_48_[15:8]	7:0	See description of '153BE6h'.	
74h (153BE8h)	**REG153BE8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst3; 0/1: not mask/mask.	
74h (153BE9h)	**REG153BE9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_15_0_[15:8]	7:0	See description of '153BE8h'.	
75h (153BEAh)	**REG153BEA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst3; 0/1: not mask/mask.	
75h (153BEBh)	**REG153BEB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_31_16_[15:8]	7:0	See description of '153BEAh'.	
76h (153BECh)	**REG153BEC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst3; 0/1: not mask/mask.	

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
76h (153BEDh)	**REG153BED**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_47_32_[15:8]	7:0	See description of '153BECh'.	
77h (153BEEh)	**REG153BEE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63:48] for hst3; 0/1: not mask/mask.	
77h (153BEFh)	**REG153BEF**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HST3_IRQ_MASK_63_48_[15:8]	7:0	See description of '153BEEh'.	
78h (153BF0h)	**REG153BF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst3; 0/1: not reverse/reverse.	
78h (153BF1h)	**REG153BF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '153BF0h'.	
79h (153BF2h)	**REG153BF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst3; 0/1: not reverse/reverse.	
79h (153BF3h)	**REG153BF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '153BF2h'.	
7Ah (153BF4h)	**REG153BF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst3; 0/1: not reverse/reverse.	
7Ah (153BF5h)	**REG153BF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '153BF4h'.	
7Bh (153BF6h)	**REG153BF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63:48] polarity for hst3; 0/1: not reverse/reverse.	
7Bh (153BF7h)	**REG153BF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HST3_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '153BF6h'.	
7Ch (153BF8h)	**REG153BF8**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst3;	
7Ch (153BF9h)	**REG153BF9**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_15_0_[15:8]	7:0	See description of '153BF8h'.	
7Dh (153BFAh)	**REG153BFA**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst3;	
7Dh	**REG153BFB**	**7:0**	**Default : 0x00**	**Access : RO**

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INTR_CTRL2 Register (Bank = 153B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153BFBh)	HST3_IRQ_STATUS_31_16_[15:8]	7:0	See description of '153BFAh'.	
7Eh (153BFCh)	**REG153BFC**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst3;	
7Eh (153BFDh)	**REG153BFD**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_47_32_[15:8]	7:0	See description of '153BFCh'.	
7Fh (153BFEh)	**REG153BFE**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63:48] for hst3;	
7Fh (153BFFh)	**REG153BFF**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_63_48_[15:8]	7:0	See description of '153BFEh'.	

IDAC Register (Bank = 153E)

IDAC Register (Bank = 153E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (153E00h)	**REG153E00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_IDAC_REF	4	Enable IDAC Ref.	
	-	3:1	Reserved.	
	EN_IDAC_SDX	0	Enable X DAC.	
00h (153E01h)	**REG153E01**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_REF_IDAC_GAINSD	7	Enable reference register SD DAC gain control.	
	GCR_IDAC_GAINSD[6:0]	6:0	SD DAC gain control.	
01h (153E02h)	**REG153E02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DAT_CLK_DLY[3:0]	7:4	Delay settings of SD DAC clock.	
	-	3:1	Reserved.	
	SD_DAT_CLK_INV	0	Invert clock to SD DAC.	
02h (153E04h)	**REG153E04**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	SD_DAC_RAMP_MD[1:0]	5:4	DAC pattern mode: 00: Force DAC to minimum value (10'b0). 01: Force DAC to maximum value (10'h3FF). 10: Force DAC to register setting value. 11: Output ramp pattern to DAC.	

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IDAC Register (Bank = 153E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SD_DAC_TEST_SEL[1:0]	3:2	Test input select of DAC: 00: ADC test bus. 01: External test vector. 10: DVBC test bus. 11: Internal BIST pattern.	
	SD_DAC_OUT_SEL[1:0]	1:0	Source of DAC output: 00: HD Gen output. 01: VE output (CVBS+S-Video). 10: Test Mode. 11: VE output (Y/Pb/Pr).	
02h (153E05h)	**REG153E05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DAC_SWAP_SEL[2:0]	2:0	Swap three output SD DAC. 001: XCY. 010: YXC. 100: CYX. 101: YCX. 110: CXY. others: XYC.	
03h (153E06h)	**REG153E06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	EN_IDAC_B	2	Enable HD B DAC.	
	EN_IDAC_G	1	Enable HD G DAC.	
	EN_IDAC_R	0	Enable HD R DAC.	
03h (153E07h)	**REG153E07**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_REF_IDAC_GAINR	7	Enable reference register HD R DAC gain control.	
	GCR_IDAC_GAINR[6:0]	6:0	HD R DAC gain control.	
04h (153E08h)	**REG153E08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HD_DAT_CLK_DLY[3:0]	7:4	Delay settings of HD DAC clock.	
	-	3:1	Reserved.	
	HD_DAT_CLK_INV	0	Invert clock to HD DAC.	
04h (153E09h)	**REG153E09**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_OUT_SEL[1:0]	7:6	Debug output select.	
	-	5:1	Reserved.	
	IDAC_SEL_REXT	0	Select external resistor.	

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IDAC Register (Bank = 153E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (153E0Ah)	**REG153E0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	HD_DAC_RAMP_MD[1:0]	5:4	DAC pattern mode: 00: Force DAC to minimum value (10'b0). 01: Force DAC to maximum value (10'h3FF). 10: Force DAC to register setting value. 11: Output ramp pattern to DAC.	
	HD_DAC_TEST_SEL[1:0]	3:2	Test input select of DAC: 00: ADC test bus. 01: External test vector. 10: DVBC test bus. 11: Internal BIST pattern.	
	HD_DAC_OUT_SEL[1:0]	1:0	Source of DAC output: 00: HD Gen output. 01: VE output (CVBS+S-Video). 10: Test Mode. 11: VE output (Y/Pb/Pr).	
05h (153E0Bh)	**REG153E0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HD_DAC_SWAP_SEL[2:0]	2:0	Swap three output HD DAC. 001: RBG. 010: GRB. 100: BGR. 101: GBR. 110: BRG. others: RGB.	
06h (153E0Ch)	**REG153E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DAC_LEVEL_TEST[7:0]	7:0	Force DAC test value.	
06h (153E0Dh)	**REG153E0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DAC_LEVEL_TEST[11:8]	3:0	See description of '153E0Ch'.	
07h (153E0Eh)	**REG153E0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DAC_RAMP_HOLD_CYC[7:0]	7:0	Ramp hold period for test.	
07h (153E0Fh)	**REG153E0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DAC_RAMP_STEP[7:0]	7:0	Ramp step.	
08h	**REG153E11**	**7:0**	**Default : 0x00**	**Access : R/W**

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IDAC Register (Bank = 153E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153E11h)	IQUART_SD	7	SD DAC quart current mode.	
	IQUART_HD	6	HD DAC quart current mode.	
	IHALF_SD	5	SD DAC half current mode.	
	IHALF_HD	4	HD DAC half current mode.	
	-	3	Reserved.	
	MODE_SD	2	Maximum Output Voltage. 0: 1.3V. 1: 1V.	
	MODE_HD	1	Maximum Output Voltage. 0: 1.3V. 1: 1V.	
	-	0	Reserved.	
09h (153E12h)	**REG153E12**	**7:0**	**Default : 0x3F**	**Access : R/W**
	DET_IN_PRD[7:0]	7:0	Detect in period.	
09h (153E13h)	**REG153E13**	**7:0**	**Default : 0x3F**	**Access : R/W**
	DET_OUT_PRD[7:0]	7:0	Detect out period.	
0Ah (153E14h)	**REG153E14**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DAC_X_DET_EN	4	Enable Channel X plug detection.	
	-	3:2	Reserved.	
	SD_DAC_DET_MODE[1:0]	1:0	1: Detect plug in. 2: Detect plug out.	
0Bh (153E16h)	**REG153E16**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HD_DAC_B_DET_EN	6	Enable Channel B plug detection.	
	HD_DAC_G_DET_EN	5	Enable Channel G plug detection.	
	HD_DAC_R_DET_EN	4	Enable Channel R plug detection.	
	-	3:2	Reserved.	
	HD_DAC_DET_MODE[1:0]	1:0	1: Detect plug in. 2: Detect plug out.	
0Ch (153E18h)	**REG153E18**	**7:0**	**Default : 0x00**	**Access : RO**
	SD_CMP_OUT_CNT[1:0]	7:6	Compare result.	
	-	5:1	Reserved.	
	DAC_CMP_OUT	0	Analog compare result.	

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IDAC Register (Bank = 153E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (153E19h)	**REG153E19**	**7:0**	**Default : 0x00**	**Access : RO**
	SD_CMP_OUT_CNT[9:2]	7:0	See description of '153E18h'.	
0Dh (153E1Ah)	**REG153E1A**	**7:0**	**Default : 0x00**	**Access : RO**
	HD_CMP_OUT_CNT[1:0]	7:6	Compare result.	
	-	5:4	Reserved.	
	DAC_CMP_MUX[3:0]	3:0	Analog comapre channel.	
0Dh (153E1Bh)	**REG153E1B**	**7:0**	**Default : 0x00**	**Access : RO**
	HD_CMP_OUT_CNT[9:2]	7:0	See description of '153E1Ah'.	
0Eh (153E1Ch)	**REG153E1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HSYNC_DLY_SEL[3:0]	3:0	Select delay cycle of digital hsync falling.	
0Eh (153E1Dh)	**REG153E1D**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	CMP_OUT_DLY_SEL[3:0]	3:0	Select delay cycle of analog compare result.	
0Fh (153E1Eh)	**REG153E1E**	**7:0**	**Default : 0x7F**	**Access : R/W**
	DET_IN_SETUP_CYC[7:0]	7:0	Detect in setup cycles (x8).	
10h (153E20h)	**REG153E20**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_IDAC[7:0]	7:0	Reserve for idac_atop.	
10h (153E21h)	**REG153E21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TEST_IDAC[9:8]	1:0	See description of '153E20h'.	
11h (153E22h)	**REG153E22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FORCE_DET_EN	7	Force enable dac plug detection enable.	
	-	6:2	Reserved.	
	GCR_LEV[1:0]	1:0	Output level for internal 2.5V regulator. 00: 2.4V. 01: 2.3V. 10: 2.5V. 11: 2.6V.	
11h (153E23h)	**REG153E23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

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IDAC Register (Bank = 153E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GCR_LEV_PLUGDET[2:0]	2:0	Threshold level for plug-in/out detection. 000: 0.5V. 001: 0.3V. 010: 0.35V. 011: 0.4V. 100: 0.45V. 101: 0.55V. 110: 0.6V. 111: 0.65V.	
12h (153E24h)	**REG153E24**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_REF_IDAC_GAING	7	Enable reference register HD G DAC gain control.	
	GCR_IDAC_GAING[6:0]	6:0	HD G DAC gain control.	
12h (153E25h)	**REG153E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_REF_IDAC_GAINB	7	Enable reference register HD BDAC gain control.	
	GCR_IDAC_GAINB[6:0]	6:0	HD B DAC gain control.	
13h (153E26h)	**REG153E26**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DAC_DET_DAT[7:0]	7:0	SD compare level.	
13h (153E27h)	**REG153E27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SD_DAC_DET_DAT[11:8]	3:0	See description of '153E26h'.	
14h (153E28h)	**REG153E28**	**7:0**	**Default : 0x00**	**Access : R/W**
	HD_DAC_DET_DAT[7:0]	7:0	HD compare level.	
14h (153E29h)	**REG153E29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HD_DAC_DET_DAT[11:8]	3:0	See description of '153E28h'.	

INTR_CPUINT2 Register (Bank = 153F)

INTR_CPUINT2 Register (Bank = 153F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (153F40h)	**REG153F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST0TO3_INT	2	Host0 to host3 interrupt.	
	HST0TO2_INT	1	Host0 to host2 interrupt.	

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INTR_CPUINT2 Register (Bank = 153F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HST0TO1_INT	0	Host0 to host1 interrupt.	
22h (153F44h)	**REG153F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST1TO3_INT	2	Host1 to host3 interrupt.	
	HST1TO2_INT	1	Host1 to host2 interrupt.	
	HST1TO0_INT	0	Host1 to host0 interrupt.	
24h (153F48h)	**REG153F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST2TO3_INT	2	Host2 to host3 interrupt.	
	HST2TO1_INT	1	Host2 to host1 interrupt.	
	HST2TO0_INT	0	Host2 to host0 interrupt.	
26h (153F4Ch)	**REG153F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HST3TO2_INT	2	Host3 to host2 interrupt.	
	HST3TO1_INT	1	Host3 to host1 interrupt.	
	HST3TO0_INT	0	Host3 to host0 interrupt.	
28h (153F50h)	**REG153F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host0 fiq final status[7:0]). Bit1 => OR (host0 fiq final status[15:8]). ..... Bit7 => OR (host0 fiq final status[63:56]).	
28h (153F51h)	**REG153F51**	**7:0**	**Default : 0x00**	**Access : RO**
	HST0_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host0 irq final status[7:0]). Bit1 => OR (host0 irq final status[15:8]). ..... Bit7 => OR (host0 irq final status[63:56]).	
29h (153F52h)	**REG153F52**	**7:0**	**Default : 0x00**	**Access : RO**
	HST1_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host1 fiq final status[7:0]). Bit1 => OR (host1 fiq final status[15:8]). ..... Bit7 => OR (host1 fiq final status[63:56]).	
29h	**REG153F53**	**7:0**	**Default : 0x00**	**Access : RO**

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INTR_CPUINT2 Register (Bank = 153F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(153F53h)	HST1_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host1 irq final status[7:0]). Bit1 => OR (host1 irq final status[15:8]). ..... Bit7 => OR (host1 irq final status[63:56]).	
2Ah (153F54h)	**REG153F54**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host2 fiq final status[7:0]). Bit1 => OR (host2 fiq final status[15:8]). ..... Bit7 => OR (host2 fiq final status[63:56]).	
2Ah (153F55h)	**REG153F55**	**7:0**	**Default : 0x00**	**Access : RO**
	HST2_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host2 irq final status[7:0]). Bit1 => OR (host2 irq final status[15:8]). ..... Bit7 => OR (host2 irq final status[63:56]).	
2Bh (153F56h)	**REG153F56**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_FIQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host3 fiq final status[7:0]). Bit1 => OR (host3 fiq final status[15:8]). ..... Bit7 => OR (host3 fiq final status[63:56]).	
2Bh (153F57h)	**REG153F57**	**7:0**	**Default : 0x00**	**Access : RO**
	HST3_IRQ_STATUS_GROUP[7:0]	7:0	Bit0 => OR (host3 irq final status[7:0]). Bit1 => OR (host3 irq final status[15:8]). ..... Bit7 => OR (host3 irq final status[63:56]).	

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VD REGISTER TABLE

MCU Register (Bank = 10)

MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1000h)	**REG1000**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_START_ADDR_1[7:0]	7:0	SRAM_A Start Address[23:16].	
00h (1001h)	**REG1001**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_START_ADDR_1[15:8]	7:0	See description of '1000h'.	
01h (1002h)	**REG1002**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_END_ADDR_1[7:0]	7:0	SRAM_A End Address[23:16].	
01h (1003h)	**REG1003**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_END_ADDR_1[15:8]	7:0	See description of '1002h'.	
02h (1004h)	**REG1004**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAMA_START_ADDR_0[7:0]	7:0	SRAM_A End Address[15:0],bit[7:0] don't care.	
02h (1005h)	**REG1005**	**7:0**	**Default : 0xF8**	**Access : R/W**
	SRAMA_START_ADDR_0[15:8]	7:0	See description of '1004h'.	
03h (1006h)	**REG1006**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SRAMA_END_ADDR_0[7:0]	7:0	SRAM_A End Address[15:0],bit[7:0] don't care.	
03h (1007h)	**REG1007**	**7:0**	**Default : 0xFB**	**Access : R/W**
	SRAMA_END_ADDR_0[15:8]	7:0	See description of '1006h'.	
04h (1008h)	**REG1008**	**7:0**	**Default : 0x01**	**Access : R/W**
	DRAM_START_ADDR_1[7:0]	7:0	DRAM Start Address[23:16].	
04h (1009h)	**REG1009**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_START_ADDR_1[15:8]	7:0	See description of '1008h'.	
05h (100Ah)	**REG100A**	**7:0**	**Default : 0x0F**	**Access : R/W**
	DRAM_END_ADDR_1[7:0]	7:0	DRAM End Address[23:16].	
05h (100Bh)	**REG100B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_END_ADDR_1[15:8]	7:0	See description of '100Ah'.	
06h (100Ch)	**REG100C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_START_ADDR_0[7:0]	7:0	DRAM Start Address[15:0],bit[7:0] don't care.	
06h (100Dh)	**REG100D**	**7:0**	**Default : 0x80**	**Access : R/W**
	DRAM_START_ADDR_0[15:8]	7:0	See description of '100Ch'.	
07h	**REG100E**	**7:0**	**Default : 0xFF**	**Access : R/W**

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MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
(100Eh)	DRAM_END_ADDR_0[7:0]	7:0	DRAM End Address[15:0],bit[7:0] don't care.	
07h (100Fh)	**REG100F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DRAM_END_ADDR_0[15:8]	7:0	See description of '100Eh'.	
08h (1010h)	**REG1010**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[7:0]	7:0	SPI Start Address[23:16].	
08h (1011h)	**REG1011**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[15:8]	7:0	See description of '1010h'.	
09h (1012h)	**REG1012**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[7:0]	7:0	SPI End Address[23:16].	
09h (1013h)	**REG1013**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[15:8]	7:0	See description of '1012h'.	
0Ah (1014h)	**REG1014**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[7:0]	7:0	SPI Start Address[15:0],bit[7:0] don't care.	
0Ah (1015h)	**REG1015**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[15:8]	7:0	See description of '1014h'.	
0Bh (1016h)	**REG1016**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[7:0]	7:0	SPI End Address[15:0],bit[7:0] don't care.	
0Bh (1017h)	**REG1017**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[15:8]	7:0	See description of '1016h'.	
0Ch (1018h)	**REG1018**	**7:0**	**Default : 0x02**	**Access : R/W**
	MCU_BANK_USE_XFR	7	Use xfr to switch bank.	
	TEST_SEL[2:0]	6:4	Test bus selection.	
	ICACHE_RSTZ	3	Icache enable.	
	DRAM_EN	2	DRAM enable.	
	SPI_EN	1	SPI enable.	
	SRAMA_EN	0	SRAM_A enable.	
0Ch (1019h)	**REG1019**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU_BANK_XFR[7:0]	7:0	Xfr BANK(64KB).	
0Dh (101Ah)	**REG101A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TWA[7:0]	7:0	TWA for RIU Bridge.	
0Dh (101Bh)	**REG101B**	**7:0**	**Default : 0x01**	**Access : R/W**
	TAW[7:0]	7:0	TAW for RIU Bridge.	
20h	**REG1040**	**7:0**	**Default : 0x00**	**Access : R/W**

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1040h)	P0_OV[7:0]	7:0	P0 overide by P0_REG. 0: Disable. 1: Enable.	
20h (1041h)	**REG1041**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_REG[7:0]	7:0	Data to overide P0.	
21h (1042h)	**REG1042**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OV[7:0]	7:0	P1 overide by P1_REG. 0: Disable. 1: Enable.	
21h (1043h)	**REG1043**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_REG[7:0]	7:0	Data to overide P1.	
22h (1044h)	**REG1044**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OV[7:0]	7:0	P2 overide by P2_REG. 0: Disable. 1: Enable.	
22h (1045h)	**REG1045**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_REG[7:0]	7:0	Data to overide P2.	
23h (1046h)	**REG1046**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OV[7:0]	7:0	P3 overide by P3_REG. 0: Disable. 1: Enable.	
23h (1047h)	**REG1047**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_REG[7:0]	7:0	Data to overide P3.	
24h (1048h)	**REG1048**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_CTRL[7:0]	7:0	MCU Port 0 Output Enable Control.	
25h (104Ah)	**REG104A**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OE[7:0]	7:0	MCU Port 0 output enable.	
26h (104Ch)	**REG104C**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_IN[7:0]	7:0	MCU Port 0 output enable from output data.	
27h (104Eh)	**REG104E**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_CTRL[7:0]	7:0	MCU Port 1 Output Enable Control.	
28h (1050h)	**REG1050**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OE[7:0]	7:0	MCU Port 1 output enable.	
29h	**REG1052**	**7:0**	**Default : 0x00**	**Access : R/W**

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MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
(1052h)	P1_IN[7:0]	7:0	MCU Port 1 output enable from output data.	
2Ah (1054h)	**REG1054**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_CTRL[7:0]	7:0	MCU Port 2 Output Enable Control.	
2Bh (1056h)	**REG1056**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OE[7:0]	7:0	MCU Port 2 output enable.	
2Ch (1058h)	**REG1058**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_IN[7:0]	7:0	MCU Port 2 output enable from output data.	
2Dh (105Ah)	**REG105A**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_CTRL[7:0]	7:0	MCU Port 3 Output Enable Control.	
2Eh (105Ch)	**REG105C**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OE[7:0]	7:0	MCU Port 3 output enable.	
2Fh (105Eh)	**REG105E**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.	
40h (1080h)	**REG1080**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESET_CPU0[7:0]	7:0	Reset cpu0.	
40h (1081h)	**REG1081**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RESET_CPU0[15:8]	7:0	See description of '1080h'.	
41h (1082h)	**REG1082**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESET_CPU1[7:0]	7:0	Reset cpu1.	
41h (1083h)	**REG1083**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RESET_CPU1[15:8]	7:0	See description of '1082h'.	
42h (1084h)	**REG1084**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU0[7:0]	7:0	Sw reset cpu0(8051).	
42h (1085h)	**REG1085**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU0[15:8]	7:0	See description of '1084h'.	
43h (1086h)	**REG1086**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU1[7:0]	7:0	Sw reset cpu1(aeon).	
43h (1087h)	**REG1087**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU1[15:8]	7:0	See description of '1086h'.	
60h (10C0h)	**REG10C0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	BUFFER_MUX	7	Use 512 bytes as menuload buffer. 0: X51 xdata SRAM. 1: Menuload SRAM.	

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MENULOAD_DONE	6	Menuload done, will be cleared when menuload enabled.	
	MENULOAD_BUSY	5	Menuload busy, will be cleared when menuload done.	
	-	4:2	Reserved.	
	MENULOAD_CTRL_MODE[1:0]	1:0	Menuload trigger src select.	
60h (10C1h)	**REG10C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	ENABLE_MENULOAD_SRAM	7	Enable 512bytes menuload sram. 1: X51 xdata SRAM. 0: Xdata2miu.	
	-	6:0	Reserved.	
61h (10C2h)	**REG10C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MENULOAD_NUMBER[7:0]	7:0	Menuload numbers.	
62h (10C4h)	**REG10C4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	MENULOAD_ABORTED_ONCE	0	Menuload was aborted once.	
63h (10C6h)	**REG10C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SYNC_TRIG2_SEL	2	Select negated sync.	
	SYNC_TRIG1_SEL	1	Select negated sync.	
	SYNC_TRIG0_SEL	0	Select negated sync.	
64h (10C8h)	**REG10C8**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	MENULOAD_REALTIME_TRIG	0	Menuload realtime trigger one shot.	
65h (10CAh)	**REG10CA**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	MENULOAD_ABORT	0	Menuload abort one shot.	
66h (10CCh)	**REG10CC**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	MENULOAD_ENABLE	0	Menuload enable one shot.	
67h (10CEh)	**REG10CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MENULOAD_RIU_MODE	0	1: Download data to 512bytes SRAM thru riu, Aeon CPU can use it. 0: Download data to 512bytes SRAM thru xdata mapping.	
68h	**REG10D0**	**7:0**	**Default : 0x00**	**Access : WO**

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MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10D0h)	-	7:1	Reserved.	
	CLR_ADR	0	Clear "reg_menuload_addr" as "zero".	
70h (10E0h)	**REG10E0**	**7:0**	**Default : 0x14**	**Access : R/W**
	XB_ERAM_LB[7:0]	7:0	Eram map hk xdata low bondary(unit: 1k), suggested: 0x14.	
70h (10E1h)	**REG10E1**	**7:0**	**Default : 0x14**	**Access : R/W**
	XB_ERAM_HB[7:0]	7:0	Eram map hk xdata high bondary(unit: 1k), suggested: 0x14.	
72h (10E4h)	**REG10E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	XD2ERAM_ADRH[7:0]	7:0	Eram base address (unit: 1k, 0x000-0x3FF).	
73h (10E6h)	**REG10E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XD2ERAM_HK_MCU_PSRAM_EN	3	Enable eram mapping for hk mcu program SRAM.	
	XD2ERAM_PM_EN	2	Enable eram mapping for pm SRAM.	
	XD2ERAM_CACHE_EN	1	Enable eram mapping for 51 cache SRAM.	
	XD2ERAM_VD_MCU_EN	0	Enable eram mapping for vd mcu SRAM.	
7Ch (10F8h)	**REG10F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SPI_OFFSET_EN	0	Enable spi_offset_addr.	
7Ch (10F9h)	**REG10F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_OFFSET_ADDR[7:0]	7:0	SPI_OFFSET_ADDR[7:0].	
7Dh (10FAh)	**REG10FA**	**7:0**	**Default : 0x00**	**Access : RO**
	PROGRAM_BANK[7:0]	7:0		
7Dh (10FBh)	**REG10FB**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_BANK[7:0]	7:0		
7Eh (10FCh)	**REG10FC**	**7:0**	**Default : 0x00**	**Access : RO**
	PC_ADDR_L[7:0]	7:0	HK mcu program counter [15:0].	
7Eh (10FDh)	**REG10FD**	**7:0**	**Default : 0x00**	**Access : RO**
	PC_ADDR_L[15:8]	7:0	See description of '10FCh'.	
7Fh (10FEh)	**REG10FE**	**7:0**	**Default : 0x00**	**Access : RO**
	PC_ADDR_H[7:0]	7:0	HK mcu program counter [23:16].	
7Fh (10FFh)	**REG10FF**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA[7:0]	7:0	Return instruction to HK MCU.	

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IRQ Register (Bank = 1B)

IRQ Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1B00h)	**REG1B00**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[7:0]	7:0	Mask for fiq, bit[31:0]. 1: Mask. 0: Not mask.	
00h (1B01h)	**REG1B01**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[15:8]	7:0	See description of '1B00h'.	
01h (1B02h)	**REG1B02**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[23:16]	7:0	See description of '1B00h'.	
01h (1B03h)	**REG1B03**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[31:24]	7:0	See description of '1B00h'.	
02h (1B04h)	**REG1B04**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[7:0]	7:0	Force for fiq, bit[31:0]. 1: Force. 0: Not force.	
02h (1B05h)	**REG1B05**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[15:8]	7:0	See description of '1B04h'.	
03h (1B06h)	**REG1B06**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[23:16]	7:0	See description of '1B04h'.	
03h (1B07h)	**REG1B07**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[31:24]	7:0	See description of '1B04h'.	
04h (1B08h)	**REG1B08**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[7:0]	7:0	Clear for fiq, bit[31:0]. 1: Clear. 0: Not clear.	
04h (1B09h)	**REG1B09**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[15:8]	7:0	See description of '1B08h'.	
05h (1B0Ah)	**REG1B0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[23:16]	7:0	See description of '1B08h'.	
05h (1B0Bh)	**REG1B0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[31:24]	7:0	See description of '1B08h'.	
06h (1B0Ch)	**REG1B0C**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[7:0]	7:0	FIQ_RAW_STATUS, bit[31:0]. Interrupt source status for fiq.	

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IRQ Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (1B0Dh)	**REG1B0D**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[15:8]	7:0	See description of '1B0Ch'.	
07h (1B0Eh)	**REG1B0E**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[23:16]	7:0	See description of '1B0Ch'.	
07h (1B0Fh)	**REG1B0F**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[31:24]	7:0	See description of '1B0Ch'.	
08h (1B10h)	**REG1B10**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[7:0]	7:0	FIQ_FINAL_STATUS, bit[31:0]. Finial interrupt status for fiq.	
08h (1B11h)	**REG1B11**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[15:8]	7:0	See description of '1B10h'.	
09h (1B12h)	**REG1B12**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[23:16]	7:0	See description of '1B10h'.	
09h (1B13h)	**REG1B13**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[31:24]	7:0	See description of '1B10h'.	
0Ah (1B14h)	**REG1B14**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[7:0]	7:0	Sel H or L trigger, bit[31:0]. Inverse source polarity for fiq.	
0Ah (1B15h)	**REG1B15**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '1B14h'.	
0Bh (1B16h)	**REG1B16**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '1B14h'.	
0Bh (1B17h)	**REG1B17**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '1B14h'.	
0Ch (1B18h)	**REG1B18**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[7:0]	7:0	Mask for irq, bit[31:0]. 1: Mask. 0: Not mask.	
0Ch (1B19h)	**REG1B19**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[15:8]	7:0	See description of '1B18h'.	
0Dh (1B1Ah)	**REG1B1A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[23:16]	7:0	See description of '1B18h'.	
0Dh (1B1Bh)	**REG1B1B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[31:24]	7:0	See description of '1B18h'.	

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IRQ Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (1B1Ch)	**REG1B1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[7:0]	7:0	Force for irq, bit[31:0]. 1: Force. 0: Not force.	
0Eh (1B1Dh)	**REG1B1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[15:8]	7:0	See description of '1B1Ch'.	
0Fh (1B1Eh)	**REG1B1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[23:16]	7:0	See description of '1B1Ch'.	
0Fh (1B1Fh)	**REG1B1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[31:24]	7:0	See description of '1B1Ch'.	
10h (1B20h)	**REG1B20**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[7:0]	7:0	Sel H or L trigger, bit[31:0]. Inverse source polarity for irq.	
10h (1B21h)	**REG1B21**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '1B20h'.	
11h (1B22h)	**REG1B22**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '1B20h'.	
11h (1B23h)	**REG1B23**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '1B20h'.	
12h (1B24h)	**REG1B24**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[7:0]	7:0	IRQ_RAW_STATUS, bit[31:0]. Interrupt source status for irq.	
12h (1B25h)	**REG1B25**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[15:8]	7:0	See description of '1B24h'.	
13h (1B26h)	**REG1B26**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[23:16]	7:0	See description of '1B24h'.	
13h (1B27h)	**REG1B27**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[31:24]	7:0	See description of '1B24h'.	
14h (1B28h)	**REG1B28**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ_FINAL_STATUS, bit[31:0]. Finial interrupt status for irq.	
14h (1B29h)	**REG1B29**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[15:8]	7:0	See description of '1B28h'.	
15h	**REG1B2A**	**7:0**	**Default : 0x00**	**Access : RO**

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IRQ Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1B2Ah)	IRQ_FINAL_STATUS[23:16]	7:0	See description of '1B28h'.	
15h (1B2Bh)	**REG1B2B**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[31:24]	7:0	See description of '1B28h'.	
20h (1B40h)	**REG1B40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_FIQ_MASK[7:0]	7:0	Mask for fiq, bit[31:0]. 1: Mask. 0: Not mask.	
20h (1B41h)	**REG1B41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_FIQ_MASK[15:8]	7:0	See description of '1B40h'.	
21h (1B42h)	**REG1B42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_FIQ_MASK[23:16]	7:0	See description of '1B40h'.	
21h (1B43h)	**REG1B43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_FIQ_MASK[31:24]	7:0	See description of '1B40h'.	
22h (1B44h)	**REG1B44**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_FORCE[7:0]	7:0	Force for fiq, bit[31:0]. 1: Force. 0: Not force.	
22h (1B45h)	**REG1B45**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_FORCE[15:8]	7:0	See description of '1B44h'.	
23h (1B46h)	**REG1B46**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_FORCE[23:16]	7:0	See description of '1B44h'.	
23h (1B47h)	**REG1B47**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_FORCE[31:24]	7:0	See description of '1B44h'.	
24h (1B48h)	**REG1B48**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_CLR[7:0]	7:0	Clear for fiq, bit[31:0]. 1: Clear. 0: Not clear.	
24h (1B49h)	**REG1B49**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_CLR[15:8]	7:0	See description of '1B48h'.	
25h (1B4Ah)	**REG1B4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_CLR[23:16]	7:0	See description of '1B48h'.	
25h (1B4Bh)	**REG1B4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_CLR[31:24]	7:0	See description of '1B48h'.	
26h	**REG1B4C**	**7:0**	**Default : 0x00**	**Access : RO**

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IRQ Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1B4Ch)	AEON_FIQ_RAW_STATUS[7:0]	7:0	Fiq_raw_status, bit[31:0]. Interrupt source status for fiq.	
26h (1B4Dh)	**REG1B4D**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_FIQ_RAW_STATUS[15:8]	7:0	See description of '1B4Ch'.	
27h (1B4Eh)	**REG1B4E**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_FIQ_RAW_STATUS[23:16]	7:0	See description of '1B4Ch'.	
27h (1B4Fh)	**REG1B4F**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_FIQ_RAW_STATUS[31:24]	7:0	See description of '1B4Ch'.	
28h (1B50h)	**REG1B50**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_FIQ_FINAL_STATUS[7:0]	7:0	Fiq_final_status, bit[31:0]. Finial interrupt status for fiq.	
28h (1B51h)	**REG1B51**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_FIQ_FINAL_STATUS[15:8]	7:0	See description of '1B50h'.	
29h (1B52h)	**REG1B52**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_FIQ_FINAL_STATUS[23:16]	7:0	See description of '1B50h'.	
29h (1B53h)	**REG1B53**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_FIQ_FINAL_STATUS[31:24]	7:0	See description of '1B50h'.	
2Ah (1B54h)	**REG1B54**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_SEL_HL_TRIGGER[7:0]	7:0	Sel H or L trigger, bit[31:0]. Inverse source polarity for fiq.	
2Ah (1B55h)	**REG1B55**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '1B54h'.	
2Bh (1B56h)	**REG1B56**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '1B54h'.	
2Bh (1B57h)	**REG1B57**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_FIQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '1B54h'.	
2Ch (1B58h)	**REG1B58**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_IRQ_MASK[7:0]	7:0	Mask for irq, bit[31:0]. 1: Mask. 0: Not mask.	
2Ch (1B59h)	**REG1B59**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_IRQ_MASK[15:8]	7:0	See description of '1B58h'.	
2Dh (1B5Ah)	**REG1B5A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_IRQ_MASK[23:16]	7:0	See description of '1B58h'.	

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IRQ Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Dh (1B5Bh)	**REG1B5B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AEON_C_IRQ_MASK[31:24]	7:0	See description of '1B58h'.	
2Eh (1B5Ch)	**REG1B5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_FORCE[7:0]	7:0	Force for irq, bit[31:0]. 1: Force. 0: Not force.	
2Eh (1B5Dh)	**REG1B5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_FORCE[15:8]	7:0	See description of '1B5Ch'.	
2Fh (1B5Eh)	**REG1B5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_FORCE[23:16]	7:0	See description of '1B5Ch'.	
2Fh (1B5Fh)	**REG1B5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_FORCE[31:24]	7:0	See description of '1B5Ch'.	
30h (1B60h)	**REG1B60**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_SEL_HL_TRIGGER[7:0]	7:0	Sel H or L trigger, bit[31:0]. Inverse source polarity for irq.	
30h (1B61h)	**REG1B61**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '1B60h'.	
31h (1B62h)	**REG1B62**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '1B60h'.	
31h (1B63h)	**REG1B63**	**7:0**	**Default : 0x00**	**Access : R/W**
	AEON_C_IRQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '1B60h'.	
32h (1B64h)	**REG1B64**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_IRQ_RAW_STATUS[7:0]	7:0	Irq_raw_status, bit[31:0]. Interrupt source status for irq.	
32h (1B65h)	**REG1B65**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_IRQ_RAW_STATUS[15:8]	7:0	See description of '1B64h'.	
33h (1B66h)	**REG1B66**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_IRQ_RAW_STATUS[23:16]	7:0	See description of '1B64h'.	
33h (1B67h)	**REG1B67**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_IRQ_RAW_STATUS[31:24]	7:0	See description of '1B64h'.	
34h (1B68h)	**REG1B68**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_IRQ_FINAL_STATUS[7:0]	7:0	Irq_final_status, bit[31:0]. Finial interrupt status for irq.	
34h	**REG1B69**	**7:0**	**Default : 0x00**	**Access : RO**

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IRQ Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1B69h)	AEON_IRQ_FINAL_STATUS[15:8]	7:0	See description of '1B68h'.	
35h (1B6Ah)	**REG1B6A**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_IRQ_FINAL_STATUS[23:16]	7:0	See description of '1B68h'.	
35h (1B6Bh)	**REG1B6B**	**7:0**	**Default : 0x00**	**Access : RO**
	AEON_IRQ_FINAL_STATUS[31:24]	7:0	See description of '1B68h'.	
3Eh (1B7Ch)	**REG1B7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CPU0_2_CPU2_IRQ	1	51 to aeon1 interrupt.	
	CPU0_2_CPU1_IRQ	0	51 to aeon0 interrupt.	
3Fh (1B7Eh)	**REG1B7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CPU1_2_CPU2_IRQ	1	Aeon0 to aeon1 interrupt.	
	CPU1_2_CPU0_IRQ	0	Aeon0 to 51 interrupt.	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
07/23/12		Ÿ Created first version.

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